

## 2.5 V/3.3 V 1:5 Differential ECL/PECL/HSTL/LVDS Clock Driver

The MC100ES6014 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the  $V_{BB}$  output is used). HSTL and LVDS inputs can be used when the ES6014 is operating under PECL conditions.

The ES6014 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into  $50\ \Omega$  even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ( $\overline{EN}$ ) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100ES6014, as with most other ECL devices, can be operated from a positive  $V_{CC}$  supply in PECL mode. This allows the ES6014 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single ended CLK input pin operation is limited to a  $V_{CC} \geq 3.0$  V in PECL mode, or  $V_{EE} \leq -3.0$  V in ECL mode. Designers can take advantage of the ES6014's performance to distribute low skew clocks across the backplane or the board.

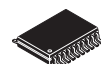
### Features

- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode:  $V_{CC} = 2.375$  V to 3.8 V with  $V_{EE} = 0$  V
- ECL Mode:  $V_{CC} = 0$  V with  $V_{EE} = -2.375$  V to  $-3.8$  V
- LVDS and HSTL Input Compatible
- Open Input Default State
- 20-Lead Pb-Free Package Available

## MC100ES6014



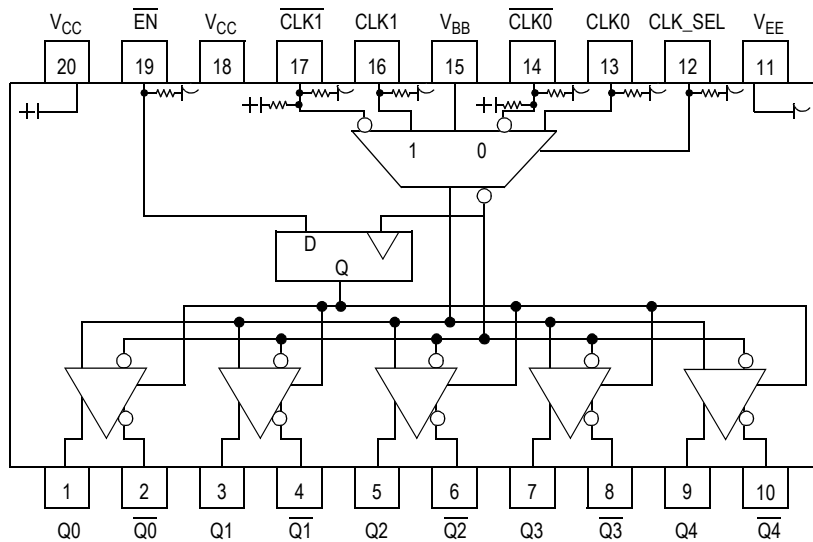
**DT SUFFIX**  
**20-LEAD TSSOP PACKAGE**  
**CASE 948E-03**



**EJ SUFFIX**  
**20-LEAD TSSOP PACKAGE**  
**Pb-FREE PACKAGE**  
**CASE 948E-03**

### ORDERING INFORMATION

Device	Package
MC100ES6014DT	TSSOP-20
MC100ES6014DTR2	TSSOP-20
MC100ES6014EJ	TSSOP-20 (Pb-Free)
MC100ES6014EJR2	TSSOP-20 (Pb-Free)



Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 20-Lead Pinout (Top View) and Logic Diagram**

**Table 1. Pin Description**

Pin	Function
CLK0*, $\overline{\text{CLK0}}$ **	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{\text{CLK1}}$ **	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{\text{Q0:4}}$	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
$\overline{\text{EN}}$ *	ECL Sync Enable
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

\* Pins will default LOW when left open.

\*\* Pins will default to  $V_{CC}/2$  when left open.

**Table 2. Function Table**

CLK0	CLK1	CLK_SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\* On next negative transition of CLK0 or CLK1

**Table 3. General specifications**

Characteristics		Value
Internal Input Pulldown Resistor		75 k $\Omega$
Internal Input Pullup Resistor		75 k $\Omega$
ESD Protection	Human Body Model	> 2000 V
	Machine Model	> 200 V
	Charged Device Model	> 1500 V
Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP	140°C/W
	500 LFPM, 20 TSSOP	100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

**Table 4. Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Characteristic	Conditions	Rating	Units
V <sub>SUPPLY</sub>	Power Supply Voltage	Difference between V <sub>CC</sub> & V <sub>EE</sub>	3.9	V
V <sub>IN</sub>	Input Voltage	V <sub>CC</sub> - V <sub>EE</sub> ≤ 3.6 V	V <sub>CC</sub> + 0.3 V <sub>EE</sub> - 0.3	V
I <sub>OUT</sub>	Output Current	Continuous Surge	50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source Current		±0.5	°C
T <sub>A</sub>	Operating Temperature Range		-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5. DC Characteristics (V<sub>CC</sub> = 0 V, V<sub>EE</sub> = -2.5 V ± 5% or V<sub>CC</sub> = 2.5 V ± 5%, V<sub>EE</sub> = 0 V)**

Symbol	Characteristics	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		30	60		30	60	mA
V <sub>OH</sub>	Output HIGH Voltage <sup>(1)</sup>	V <sub>CC</sub> -1250	V <sub>CC</sub> -990	V <sub>CC</sub> -800	V <sub>CC</sub> -1200	V <sub>CC</sub> -960	V <sub>CC</sub> -750	mV
V <sub>OL</sub>	Output LOW Voltage <sup>(1)</sup>	V <sub>CC</sub> -2000	V <sub>CC</sub> -1550	V <sub>CC</sub> -1150	V <sub>CC</sub> -1925	V <sub>CC</sub> -1630	V <sub>CC</sub> -1200	mV
V <sub>outPP</sub>	Output Peak-to-Peak Voltage	200			200			mV
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	mV
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	mV
V <sub>BB</sub>	Output Reference Voltage I <sub>BB</sub> = 200 μA	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	mV
V <sub>PP</sub>	Differential Input Voltage <sup>(2)</sup>	0.12		1.3	0.12		1.3	mV
V <sub>CMR</sub>	Differential Cross Point Voltage <sup>(3)</sup>	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.0	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.0	mV
I <sub>IN</sub>	Input Current			±150			±150	μA

1. Output termination voltage V<sub>TT</sub> = 0 V for V<sub>CC</sub> = 2.5 V operation is supported but the power consumption of the device will increase.
2. V<sub>PP</sub> (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V<sub>CMR</sub> (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V<sub>CMR</sub> (DC) range and the input swing lies within the V<sub>PP</sub> (DC) specification.

**Table 6. DC Characteristics (V<sub>CC</sub> = 0 V, V<sub>EE</sub> = -3.8 V to -3.135 V or V<sub>CC</sub> = 3.135 V to 3.8 V, V<sub>EE</sub> = 0 V)**

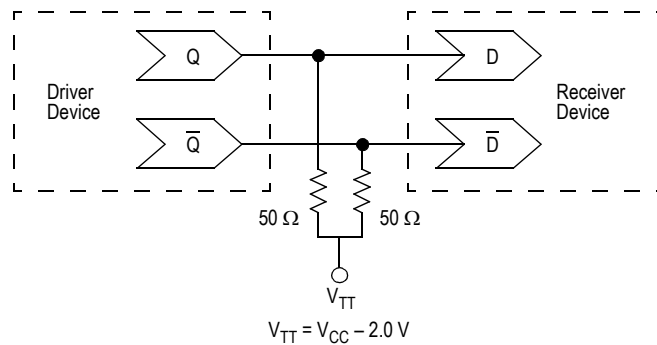
Symbol	Characteristics	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		30	60		30	60	mA
V <sub>OH</sub>	Output HIGH Voltage <sup>(1)</sup>	V <sub>CC</sub> -1150	V <sub>CC</sub> -1020	V <sub>CC</sub> -800	V <sub>CC</sub> -1200	V <sub>CC</sub> -970	V <sub>CC</sub> -750	mV
V <sub>OL</sub>	Output LOW Voltage <sup>(1)</sup>	V <sub>CC</sub> -1950	V <sub>CC</sub> -1620	V <sub>CC</sub> -1250	V <sub>CC</sub> -2000	V <sub>CC</sub> -1680	V <sub>CC</sub> -1300	mV
V <sub>outPP</sub>	Output Peak-to-Peak Voltage	200			200			mV
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	mV
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	mV
V <sub>BB</sub>	Output Reference Voltage I <sub>BB</sub> = 200 μA	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	mV
V <sub>PP</sub>	Differential Input Voltage <sup>(2)</sup>	0.12		1.3	0.12		1.3	V
V <sub>CMR</sub>	Differential Cross Point Voltage <sup>(3)</sup>	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.1	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.1	V
I <sub>IN</sub>	Input Current			±150			±150	μA

1. Output termination voltage V<sub>TT</sub> = 0 V for V<sub>CC</sub> = 2.5 V operation is supported but the power consumption of the device will increase.
2. V<sub>PP</sub> (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V<sub>CMR</sub> (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V<sub>CMR</sub> (DC) range and the input swing lies within the V<sub>PP</sub> (DC) specification.

**Table 7. AC Characteristics** ( $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-3.135\text{ V}$  or  $V_{CC} = 3.135\text{ V}$  to  $3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$ )<sup>(1)</sup>

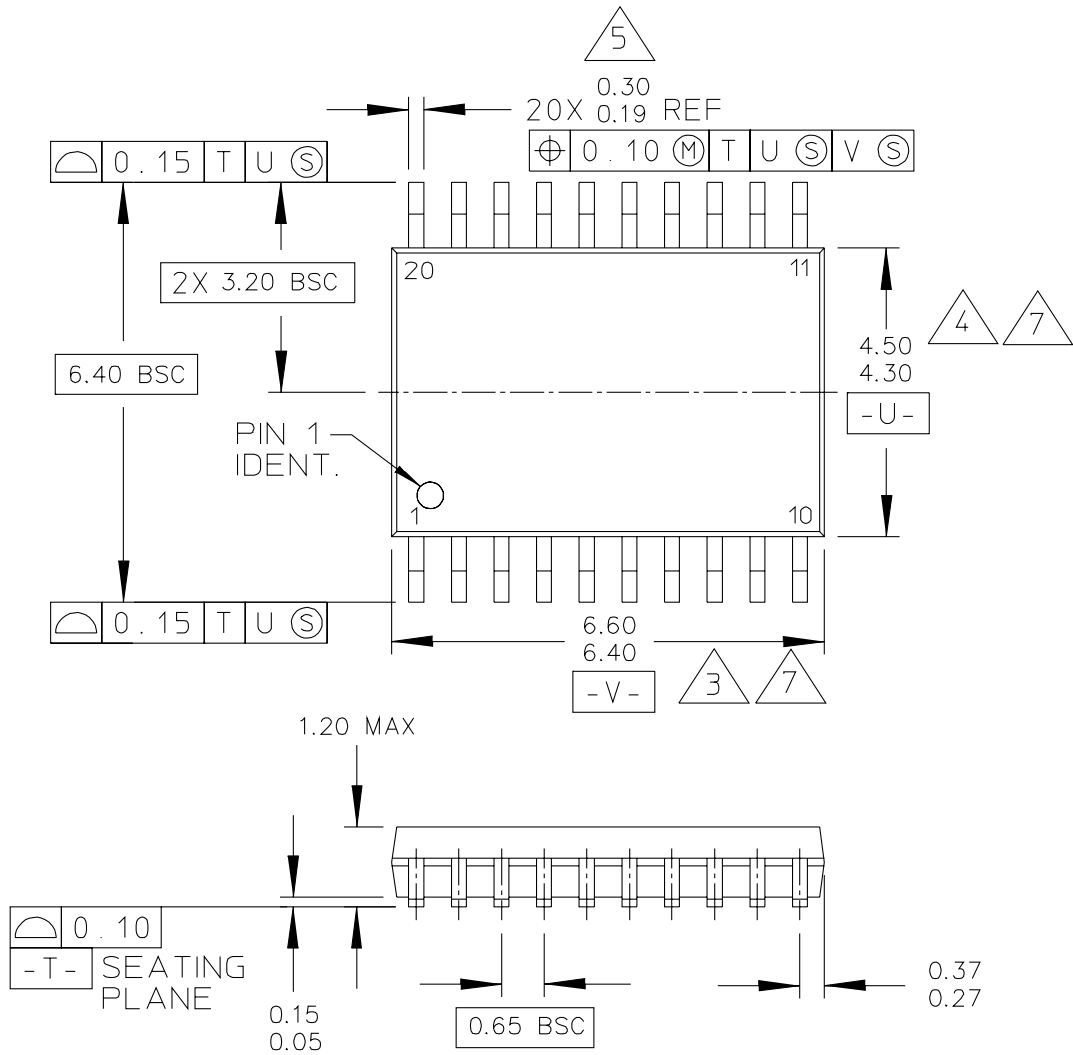
Symbol	Characteristics	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Output Frequency	2			2			2			GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay (Differential) CLK to Q, $\bar{Q}$	300	355	425	300	375	475	300	400	525	ps
$t_{SKEW}$	Within Device Skew <sup>(2)</sup> Device-to-Device Skew <sup>(2)</sup>		23	45 125		23	45 175		23	45 225	ps ps
$t_{JITTER}$	Cycle-to-Cycle Jitter RMS ( $1\sigma$ )			1			1			1	ps
$V_{PP}$	Input Peak-to-Peak Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
$V_{CMR}$	Differential Cross Point Voltage	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	V
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	70		225	70		250	70		275	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC}-2.0\text{ V}$ .
2. Skew is measured between outputs under identical transitions.



**Figure 2. Typical Termination for Output Driver and Device Evaluation**

# PACKAGE DIMENSIONS



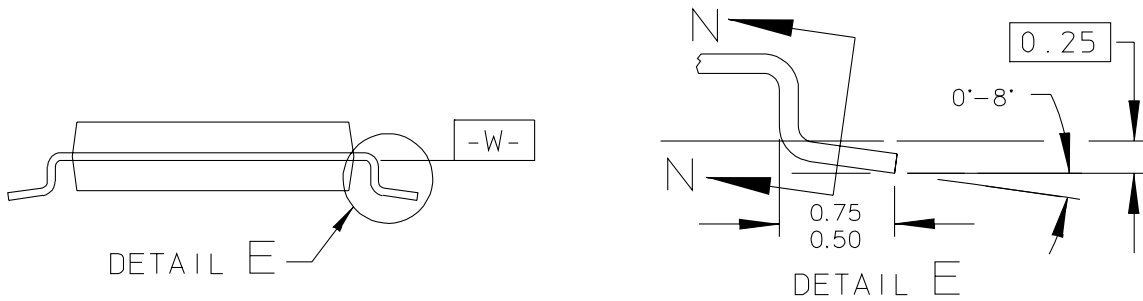
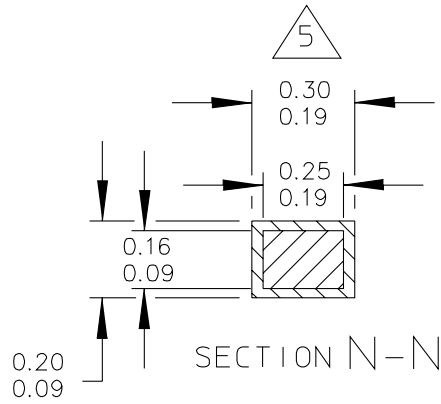
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: B	
	CASE NUMBER: 948E-03	09 MAR 2005	
	STANDARD: JEDEC		

PAGE 1 OF 3

**CASE 948E-03  
ISSUE B  
20-LEAD TSSOP PACKAGE**

MC100ES6014

## PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: B
	CASE NUMBER: 948E-03	09 MAR 2005
	STANDARD: JEDEC	

PAGE 2 OF 3

**CASE 948E-03**  
**ISSUE B**  
**20-LEAD TSSOP PACKAGE**

## PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: B	
	CASE NUMBER: 948E-03	09 MAR 2005	
	STANDARD: JEDEC		

PAGE 3 OF 3

**CASE 948E-03  
ISSUE B  
20-LEAD TSSOP PACKAGE**

**MC100ES6014**

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005. All rights reserved.

