SECTION 6
Neuron CHIP ELECTRICAL AND MECHANICAL SPECIFICATIONS

6.1 INTRODUCTION

The Neuron Chip processor family consists of two device types: MC143150 and MC143120. Within these device types are different versions, each with its own electrical and mechanical specifications. The MC143150B1FU1 and MC143120B1/E2 operate up to 10 MHz over the full industrial temperature range of – 40 to + 85°C, including writes to EEPROM down to – 40°C. Refer to Appendix C in this data book for more information on external memory interfacing.

When deciding at what speed to operate the MC143150, the cost of the external memory will be an important consideration. There is a cost difference between a 200 ns memory (EPROM access time required at 5 MHz) and a 120 ns memory (10 MHz access time) which is rated over the full industrial temperature range, particularly in surface mount packages.

For multiple memory configurations (external EPROM, EEPROM, flash, and/or SRAM), additional cost savings due to slower memory map decode logic, and lower cost of the memory, can be realized at 5 MHz operation. Power consumption will be 30 – 40% lower at 5 MHz than at 10 MHz. Issues such as required data rate and I/O response time must be considered.

Running the Neuron Chip at a higher clock rate decreases the processing time. Proper prioritizing of "when" statements in the application program and use of timer counter objects can help to minimize latency.

Refer to Section D.2 regarding handling precautions and moisture sensitivity of the various Neuron devices.

NOTE: The MC143150FU, MC143150FU1, and MC143150B1FU devices have been discontinued. **The MC143150B1FU1 is recommended for new designs.**

6.2 ELECTRICAL SPECIFICATIONS

6.2.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range (Referenced to V_{SS})	V_{DD}	– 0.3 to 7.0 V	V
Input Voltage Range (Referenced to V_{SS})	V_{in}	– 0.3 to V_{DD} + 0.3	V
Maximum Drain Current	I_{DD}	200	mA
Maximum Source Current	I_{SS}	300	mA
Maximum Power Dissipation	P_D	800	mW
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

6.2.2 Recommended Operating Conditions

(Voltages referenced to V_{SS}, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
TTL Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
TTL High-Level Input Voltage	V_{IH}	2.0	V_{DD}	V
CMOS Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
CMOS High-Level Input Voltage	V_{IH}	V_{DD} – 0.8	V_{DD}	V
Operating Free-Air Temperature	T_A	–40*	+ 85	°C

* Writes to EEPROM are guaranteed down to –40°C for all Neuron Chip devices.

6

6.2.3 Electrical Characteristics (V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}				V
IO0 – IO10, D0 – D7, CP0, CP3, CP4, $\overline{\text{SERVICE}}$		—	—	0.8	
CP0, CP1 (Differential) (See Section 6.2.5)		—	—	Programmable	
Reset				0.3 V_{DD}	
Input High Voltage	V_{IH}				V
IO0 – IO10, D0 – D7, CP0, CP3, CP4, service pin		2.0	—	—	
CP0, CP1 (Differential) (See Section 6.2.5)		Programmable	—	—	
Reset				V_{DD} – 0.7	
Low-Level Output Voltage	V_{OL}				V
Standard Outputs (I_{OL} = 1.4 mA) (Note 1)		—	—	0.4	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL}= 20 mA)		—	—	0.8	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL}= 10 mA)		—	—	0.4	
Maximum Sink (CP2, CP3) (I_{OL}= 40 mA)		—	—	1.0	
Maximum Sink (CP2, CP3) (I_{OL}= 15 mA)		—	—	0.4	
High-Level Output Voltage	V_{OH}				V
Standard Outputs (I_{OH} = –1.4 mA) (Note 1)		V_{DD} – 0.4	—	—	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$ (I_{OH} = – 1.4 mA)		V_{DD} – 0.4	—	—	
Maximum Source (CP2, CP3) (I_{OH} = – 40 mA)		V_{DD} – 1.0	—	—	
Maximum Source (CP2, CP3) (I_{OH} = – 15 mA)		V_{DD} – 0.4	—	—	
Hysteresis (Excluding CLK1, $\overline{\text{RESET}}$)	V_{hys}	175	—	—	mV
Input Current (Excluding pullups) (V_{SS} to V_{DD}) (Note 2)	I_{in}	– 10	—	10	µA

MC143150B1FU1

Pullup Source Current (V_{out} = 0 V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	µA
Operating Mode Supply Current (Notes 3, 4)					mA
10 MHz Clock		—	15	25	
5 MHz Clock		—	8	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	2.4	4.2	
0.625 MHz Clock		—	1.5	2.5	
Sleep Mode Supply Current (Notes 3, 4)		—	15	100	µA

MC143120B1

Pullup Source Current (V_{out} = 0 V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	µA
Operating Mode Supply Current (Notes 3, 4, and 5)					mA
10 MHz Clock		—	14	25	
5 MHz Clock		—	7.5	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	3.2	4.2	
0.625 MHz Clock		—	1.6	2.5	
Sleep Mode Supply Current (Note 3,4)		—	9	100	µA

MC143120E2

Pullup Source Current (V_{out} = 0 V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	µA
Operating Mode Supply Current (Notes 3, 5)					mA
10 MHz Clock		—	16	N/A	
5 MHz Clock		—	8		
2.5 MHz Clock		—	5.0		
1.25 MHz Clock		—	3.5		
0.625 MHz Clock		—	1.8		
Sleep Mode Supply Current (Notes 3, 5)		—	9	100	µA

NOTES:

1. Standard outputs are A0 – A15, D0 – D7, IO4 – IO10, CP0, CP1, CP4, $\overline{\text{E}}$, and R/$\overline{\text{W}}$. ($\overline{\text{RESET}}$ is a CMOS open drain input/output. CLK2 must have ≤ 15 pF.)
2. IO4 – IO7 and $\overline{\text{SERVICE}}$ have configurable pullups. $\overline{\text{RESET}}$ has a permanent pullup.
3. Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2 V or ≥ (V_{DD} – 0.2 V), configurable pullups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 µA typical and 600 µA maximum when enabled. It is enabled on either of the following conditions:
   - Neuron Chip in Operating mode **and** Comm Port in Differential mode.
   - Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wakeup not masked.
4. Typical values are at midpoint of voltage range and 25°C only.

Reset Trip Point (V_{DD})

Part Number	Min	Typ	Max	Unit
MC143150B1FU1	2.1	3.3	4.4	V
MC143120B1	2.1	3.3	4.4	V
MC143120E2 (See Note)	3.8	4.1	4.4	V

NOTE: On-chip LVI circuit.

6.2.4 External Memory Interface Timing — MC143150B1FU1, V_{DD} ± 10%

(V_{DD} = 4.5 to 5.5 V, T_A = – 40 to+ 85°C)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	200	3200	ns
PW_{EH}	Pulse Width, $\overline{E}$ High (Note 2)	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, $\overline{E}$ Low	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, $\overline{E}$ High to Address Valid	—	50	ns
t_{AH}	Address Hold Time after $\overline{E}$ High	10	—	ns
t_{RD}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Read	—	45	ns
t_{RH}	R/$\overline{W}$ Hold Time Read after $\overline{E}$ High	5	—	ns
t_{WR}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Write	—	45	ns
t_{WH}	R/$\overline{W}$ Hold Time Write after $\overline{E}$ High	5	—	ns
t_{DSR}	Read Data Setup Time to $\overline{E}$ High	20	—	ns
t_{DHR}	Data Hold Time Read after $\overline{E}$ High	0	—	ns
t_{DHW}	Data Hold Time Write after $\overline{E}$ High (Note 3, 4)	20	—	ns
t_{DDW}	Delay, $\overline{E}$ Low to Data Valid	—	60	ns
t_{DHZ}	Data Three State Hold Time after $\overline{E}$ Low (Note 5)	0	—	ns
t_{DDZ}	Delay, $\overline{E}$ High to Data Three-State (Note 4)	—	60	ns
t_{acc}	External Memory Access Time ($t_{acc} = t_{cyc} - t_{AD} - t_{DSR}$)	130	—	ns

NOTES:

1. t_{cyc} = 2•1/f, where f is the input clock (CLK1) frequency (10, 5, 2.5, 1.25, or 0.625 MHz). Refer to Clocking System for more details on the CLK1 input clock, including the accuracy requirements (in ppm) and duty cycle requirements.
2. Refer to Figure 6–3, Test Point Levels for $\overline{E}$ Pulse Width Measurements, for detailed measurement information.
3. The data hold parameter, t_{DHW}, is measured to the disable levels shown in Figure 6–7, Test Point Levels for Driven to Three-State Time Measurements, rather than to the traditional data invalid levels.
4. Refer to Figure 6–6, Signal Loading for Driven to Three-State Time Measurements, and Figure 6–7, Test Point Levels for Driven to Three-State Time Measurements, for detailed measurement information.
5. The three-state condition is when the device is not actively driving data. Refer to Figure 6–2, Signal Loading for Timing Specifications Unless Otherwise Specified, and Figure 6–5, Test Point Levels for Three-State to Driven Time Measurements, for detailed measurement information.

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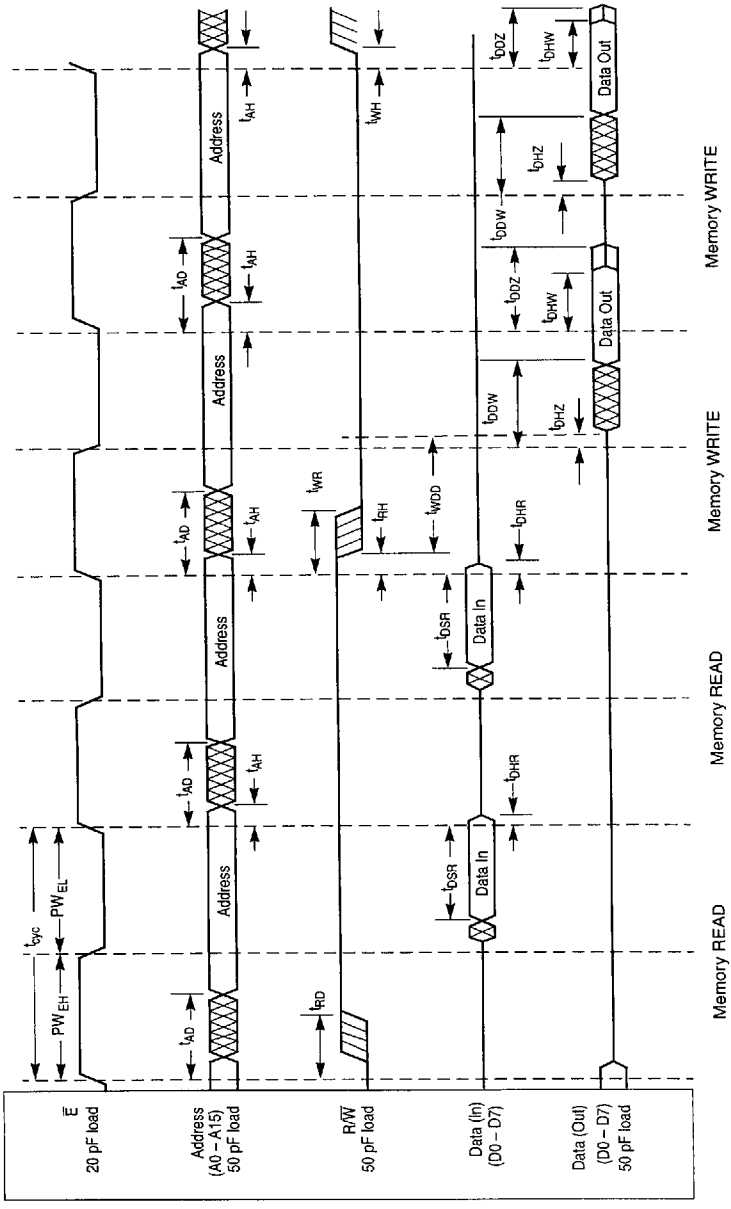

Figure 6–1. External Memory Interface Timing Diagram

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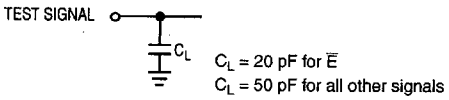


Figure 6–2. Signal Loading for Timing Specifications Unless Otherwise Specified

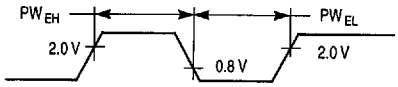
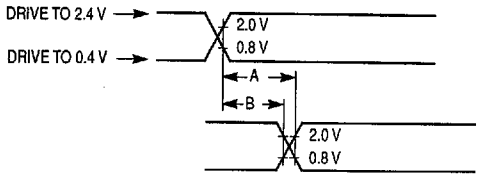


Figure 6–3. Test Point Levels for $\overline{E}$ Pulse Width Measurements



A — Signal valid to signal valid specification (maximum or minimum)
B — Signal valid to signal invalid specification (maximum or minimum)

Figure 6–4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified

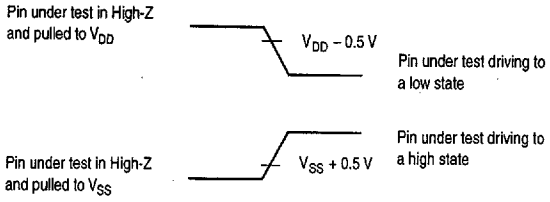


Figure 6–5. Test Point Levels for Three-State-to-Driven Time Measurements

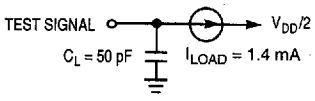
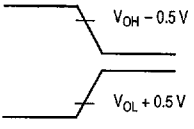


Figure 6–6. Signal Loading for Driven-to-Three-State Time Measurements



V_{OH} – Measured high output drive level
V_{OL} – Measured low output drive level

Figure 6–7. Test Point Levels for Driven-to-Three-State Time Measurements

6.2.5 Communications Port Programmable Hysteresis Values

(Expressed as differential peak to peak voltages in terms of V_{DD})

Hysteresis*	V_{hys} Min	V_{hys} Typ	V_{hys} Max
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.040 V_{DD}	0.054 V_{DD}	0.068 V_{DD}
2	0.061 V_{DD}	0.081 V_{DD}	0.101 V_{DD}
3	0.081 V_{DD}	0.108 V_{DD}	0.135 V_{DD}
4	0.101 V_{DD}	0.135 V_{DD}	0.169 V_{DD}
5	0.121 V_{DD}	0.162 V_{DD}	0.203 V_{DD}
6	0.142 V_{DD}	0.189 V_{DD}	0.236 V_{DD}
7	0.162 V_{DD}	0.216 V_{DD}	0.270 V_{DD}

* Hysteresis values are under the conditions that the input signal swing is 200 mV greater than the programmed value.

6.2.6 Communications Port Programmable Glitch Filter Values*

[Receiver (end-to-end) filter values expressed as transient pulse suppression times]

Filter (F)	Min	Typ	Max	Unit
0	10	75	140	ns
1	120	410	700	ns
2	240	800	1350	ns
3	480	1500	2600	ns

* Must be disabled if data rate is 1.25 Mbps.

6.2.7 Receiver* (End-to-End) Absolute Asymmetry

(Worst case across hysteresis)

Filter (F)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	35	ns
1	150	ns
2	250	ns
3	400	ns

* Receiver input, $V_D = V_{CP0} - V_{CP1}$, at least 200 mV greater than hysteresis levels. See Figure 6–4.

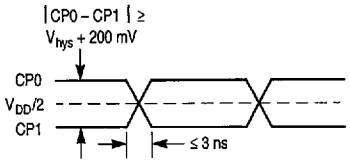


Figure 6–8. Receiver Input Waveform

6.2.8 Differential Receiver (End-to-End) Absolute Symmetry

Filter (F)	Hysteresis (H)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	0	24	ns

NOTES:

1. CP0 and CP1 inputs each 0.60 Vp–p, 1.25 MHz sine wave 180° out of phase with each other as shown in Figure 6–9.
   $V_{DD} = 5.00\ V \pm 5\%$
2. t_{PLH}: Time from input switching states from low to high to output switching states
   t_{PHL}: Time from input switching states from high to low to output switching states

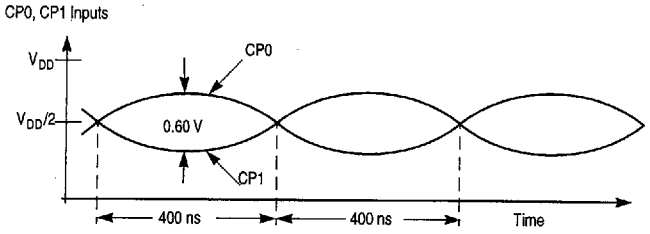


Figure 6–9. Communications Port Signal Input for Table 6.2.8

6.2.9 Differential Transceiver Electrical Characteristics

Characteristic	Min	Max
Receiver Common Mode Voltage Range to maintain hysteresis as specified in Table 4–4*	1.2 V	$V_{DD} - 2.2\ V$
Receiver Common Mode Range to operate with unspecified hysteresis	0.9 V	$V_{DD} - 1.75\ V$
Input Offset Voltage	$-0.05\ V_{hys} - 35\ mV$	$0.05\ V_{hys} + 35\ mV$
Propagation Delay ($F = 0$, $V_{ID} = V_{hys}/2 + 200\ mV$)	—	230 ns
Input Resistance	5 MΩ	—
Wake-Up Time	—	10 µs

* Common mode voltage is defined as the average value of the waveform at each input at the time switching occurs.

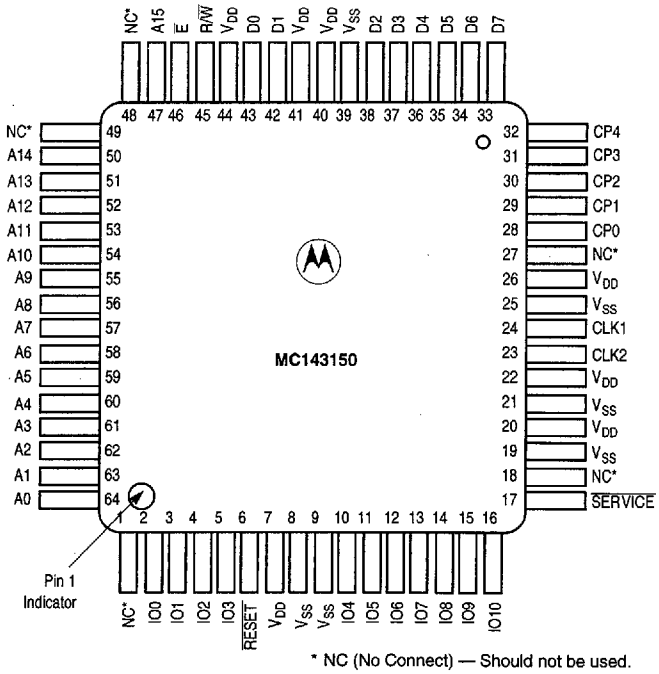
6.3 MECHANICAL SPECIFICATIONS

6.3.1 Pin Descriptions

Pin Name	I/O	Pin Function	MC143150 Pin Number	MC143120xx DW Suffix Pin Number	MC143120xx FB Suffix Pin Number
CLK1	Input	Oscillator connection or external clock input.	24	15	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. One Load.	23	14	14
$\overline{\text{RESET}}$	I/O (Built-In Pullup)	Reset pin (active low).	6	1	40
$\overline{\text{SERVICE}}$	I/O (Built-In Configurable Pullup)	Service pin. Indicator output during operation.	17	8	5
IO0 – IO3	I/O	Large current-sink capacity (20 mA). General I/O port.	2, 3, 4, 5	7, 6, 5, 4	2, 3, 4, 43
IO4 – IO7	I/O (Built-In Configurable Pullup)	General I/O port. One of IO4 to IO7 can be specified as No. 1 timer/counter input with IO0 as output. IO4 can be used as the No. 2 timer/counter input with IO1 as output.	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8 – IO10	I/O	General I/O port. Can be used for serial communication with other devices.	14, 15, 16	27, 26, 24	27, 30, 31
D0 – D7	I/O	Memory data bus.	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
R/$\overline{\text{W}}$	Output	Read/write control output port for external memory.	45	N/A	N/A
$\overline{\text{E}}$	Output	Control output port for external memory.	46	N/A	N/A
A15 – A0	Output	Address output port.	47, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64	N/A	N/A
V_{DD}	Input	Power input (5 V nom). All V_{DD} pins must be connected together externally.	7, 20, 22, 26, 40, 41, 44	2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41
V_{SS}	Input	Power input (0 V, GND). All V_{SS} pins must be connected together externally.	8, 9,19, 21, 25, 39	9, 10, 13, 16, 23, 31	7, 8, 13, 16, 26, 37
CP0 – CP4	Communication Network Interface	Bidirectional port that supports communications protocols by specifying mode.	28, 29, 30, 31, 32	19, 20, 17, 21, 22	20, 21, 18, 24, 25
NC	N/A	No internal connection. Leave open. CAUTION: Pin 18 of the MC143150 MUST NOT have any external connection.	1, 18, 27, 48, 49	N/A	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

6.3.2 MC143150 Pin Assignment

MC143150
64-LEAD QUAD FLAT-PACK

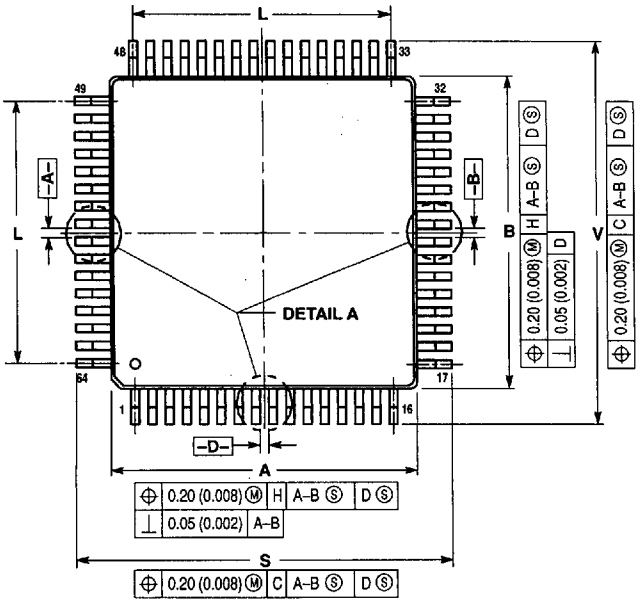


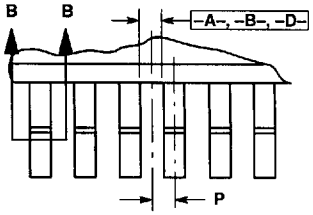
* NC (No Connect) — Should not be used.
These pins may be used for internal testing.

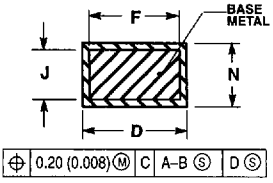
The larger dimple at the bottom left of the marking indicates pin 1.

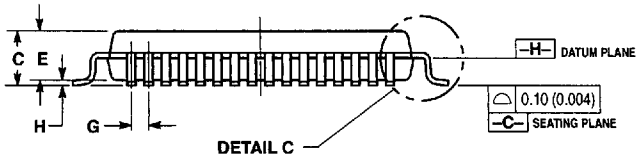
6.3.3 MC143150 Package Dimensions

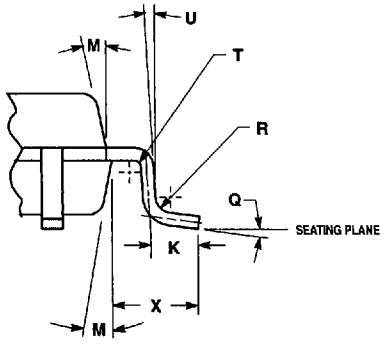
64-LEAD PQFP
CASE 840C-04









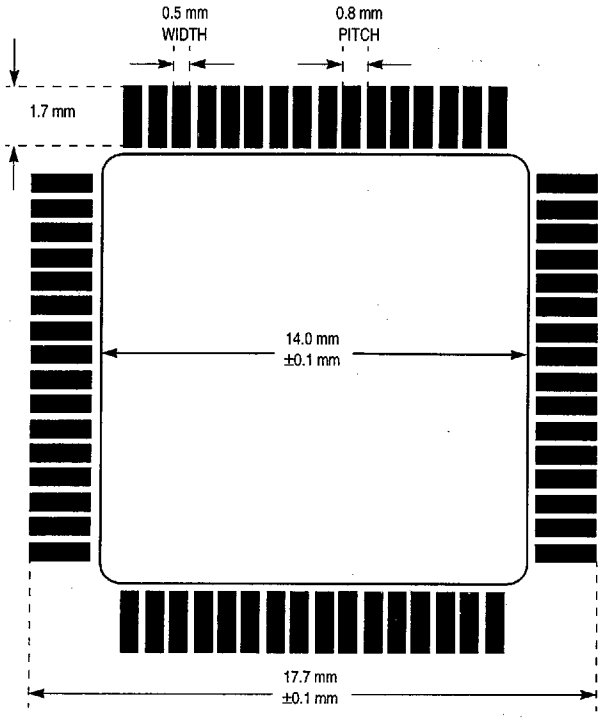


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.53 (0.021). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. DIMENSION K IS TO BE MEASURED FROM THE THEORETICAL INTERSECTION OF LEAD FOOT AND LEG CENTERLINES.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.07	2.46	0.081	0.097
D	0.30	0.45	0.012	0.018
E	2.00	2.40	0.079	0.094
F	0.30	—	0.012	—
G	0.80 BSC		0.031 BSC	
H	0.067	0.250	0.003	0.010
J	0.130	0.230	0.005	0.090
K	0.50	0.66	0.020	0.026
L	12.00 REF		0.472 REF	
M	5°	10°	5°	10°
N	0.130	0.170	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	2°	8°	2°	8°
R	0.13	0.30	0.005	0.012
S	16.20	16.60	0.638	0.654
T	0.20 REF		0.008 REF	
U	0°	—	0°	—
V	16.20	16.60	0.638	0.654
X	1.10	1.30	0.043	0.051

6.3.4 MC143150 Pad Layout

MC143150
64-LEAD QUAD FLAT PACK



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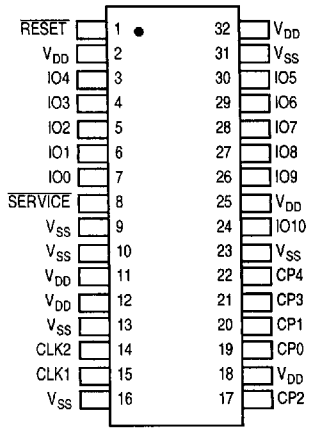
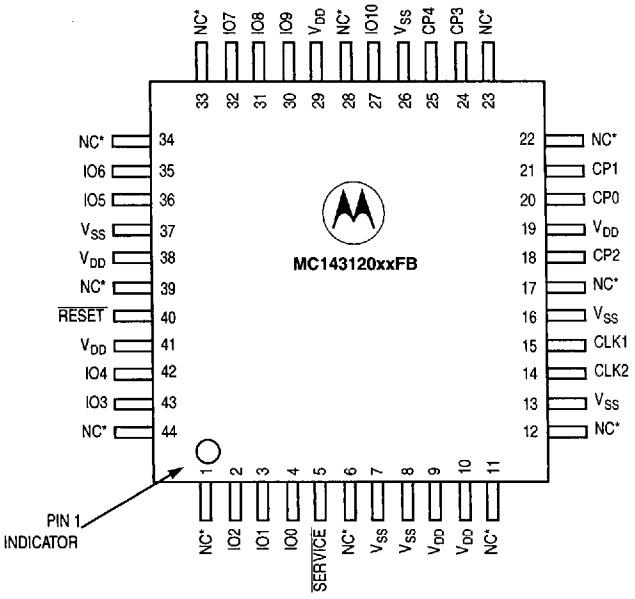
6.3.5 MC143120 Pin Assignments

32-LEAD SOG



44-LEAD QFP

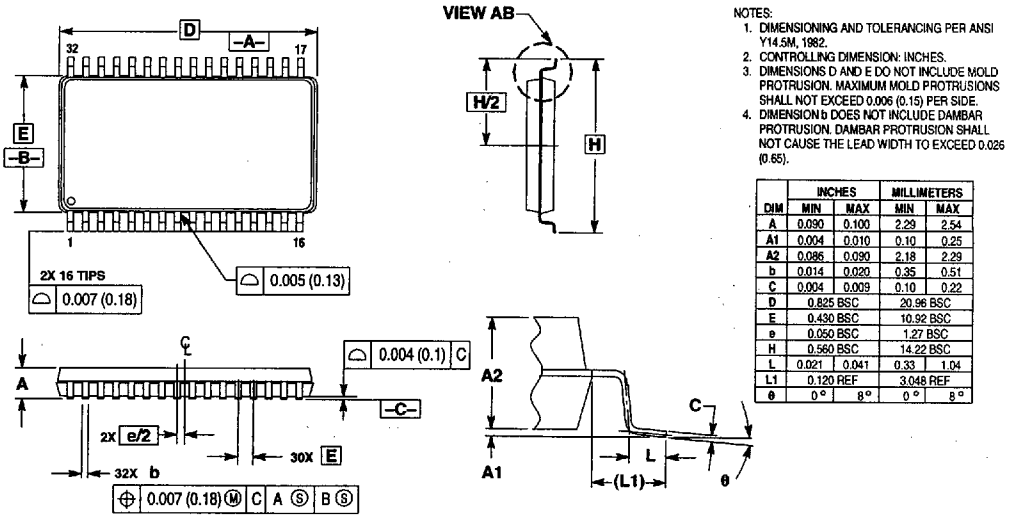


* NC (No Connect) — Should not be used.
These pins may be used for internal testing.

6

6.3.6 MC143120 Package Dimensions

DW SUFFIX
SOG PACKAGE
CASE 1116-01

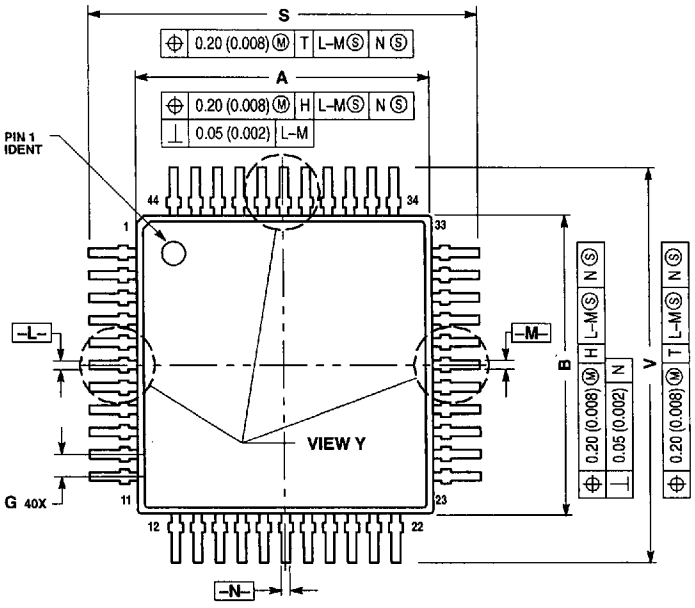


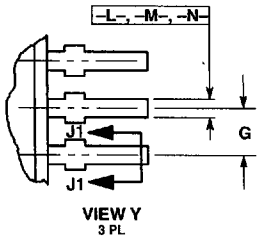
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSIONS SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.026 (0.65).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.090	0.100	2.29	2.54
A1	0.004	0.010	0.10	0.25
A2	0.086	0.090	2.18	2.29
b	0.014	0.020	0.35	0.51
C	0.004	0.009	0.10	0.22
D	0.825 BSC		20.96 BSC	
E	0.430 BSC		10.92 BSC	
e	0.050 BSC		1.27 BSC	
H	0.560 BSC		14.22 BSC	
L	0.021	0.041	0.33	1.04
L1	0.120 REF		3.048 REF	
θ	0°	8°	0°	8°

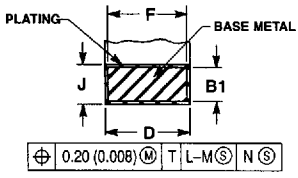
6

FB SUFFIX
PQFP PACKAGE
CASE 824E-02



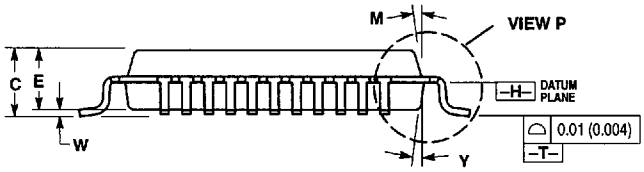


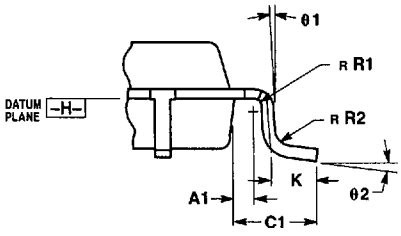
VIEW Y
3 PL



SECTION J1–J1
44 PL

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).





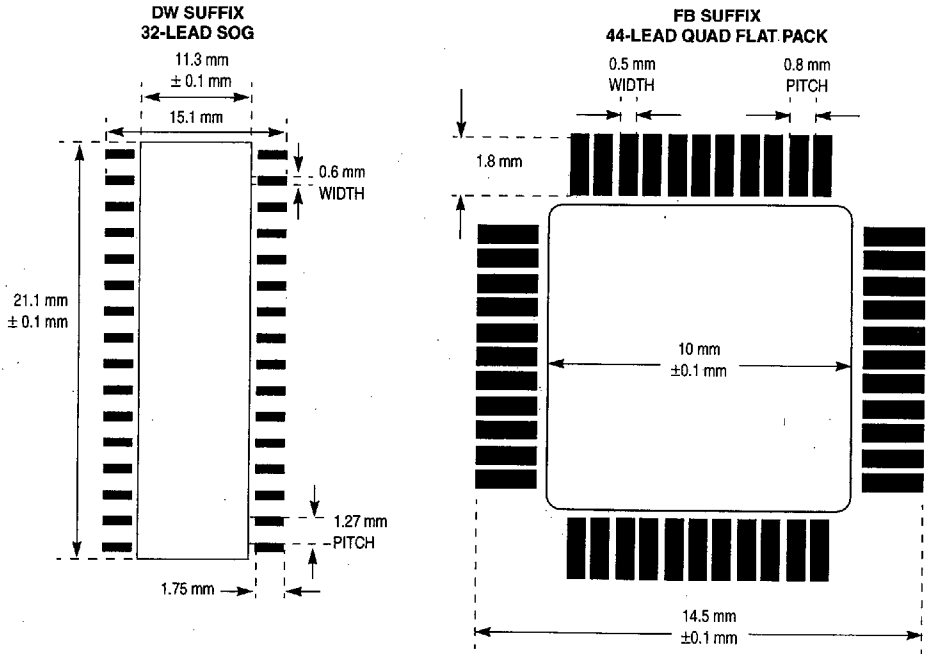
VIEW P

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.00	2.21	0.079	0.087
D	0.30	0.45	0.0118	0.0177
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
M	5°	10°	5°	10°
S	12.95	13.45	0.510	0.530
V	12.95	13.45	0.510	0.530
W	0.000	0.210	0.000	0.008
Y	5°	10°	5°	10°
A1	0.450 REF		0.018 REF	
B1	0.130	0.170	0.005	0.007
C1	1.600 REF		0.063 REF	
R1	0.130	0.300	0.005	0.012
R2	0.130	0.300	0.005	0.012
θ1	5°	10°	5°	10°
θ2	0°	7°	0°	7°

6

6.3.7 MC143120 Pad Layout

MC143120 PAD LAYOUTS



6

6.3.8 Sockets for Neuron Chips

NOTE: Motorola can not recommend one supplier over another and in no way suggests that these are the only suppliers.

Integrated Circuit	Manufacturer	Part Number
MC143120 32-Pin SOG (DW Suffix)	Yamaichi	IC51-0322-667-2
MC143120 44-Pin PQFP (FB Suffix)	Enplas	FPQ-44-0.8-16
MC143150B1FU1 64-Pin QFP	Enplas	FPQ-64-0.8-02

6.3.9 Test Clips

Below is a listing of Pamona IC test clips and their part numbers.

Device	Type	Pamona Part Number
MC143120 32-Pin SOG (DW Suffix)	SOIC	6107
MC143120 44-Pin PQFP (FB Suffix)	PLCC	5281
MC143150B1FU1 64-Pin QFP	QFP	5888-2