MN673282A

Image-Processing IC for Digital Still Cameras

■ Overview

The MN673282A is an image-processing IC with JPEG function for digital still cameras. The MN673282A supports the analog video outputs provided by the RGB checker board pattern color filter CCD area image sensors such as the Panasonic MN39571 (which features an interlaced scanning technique and 2.31 million pixels) and MN39742 (which features an interlaced scanning technique and 1.33 million pixels).

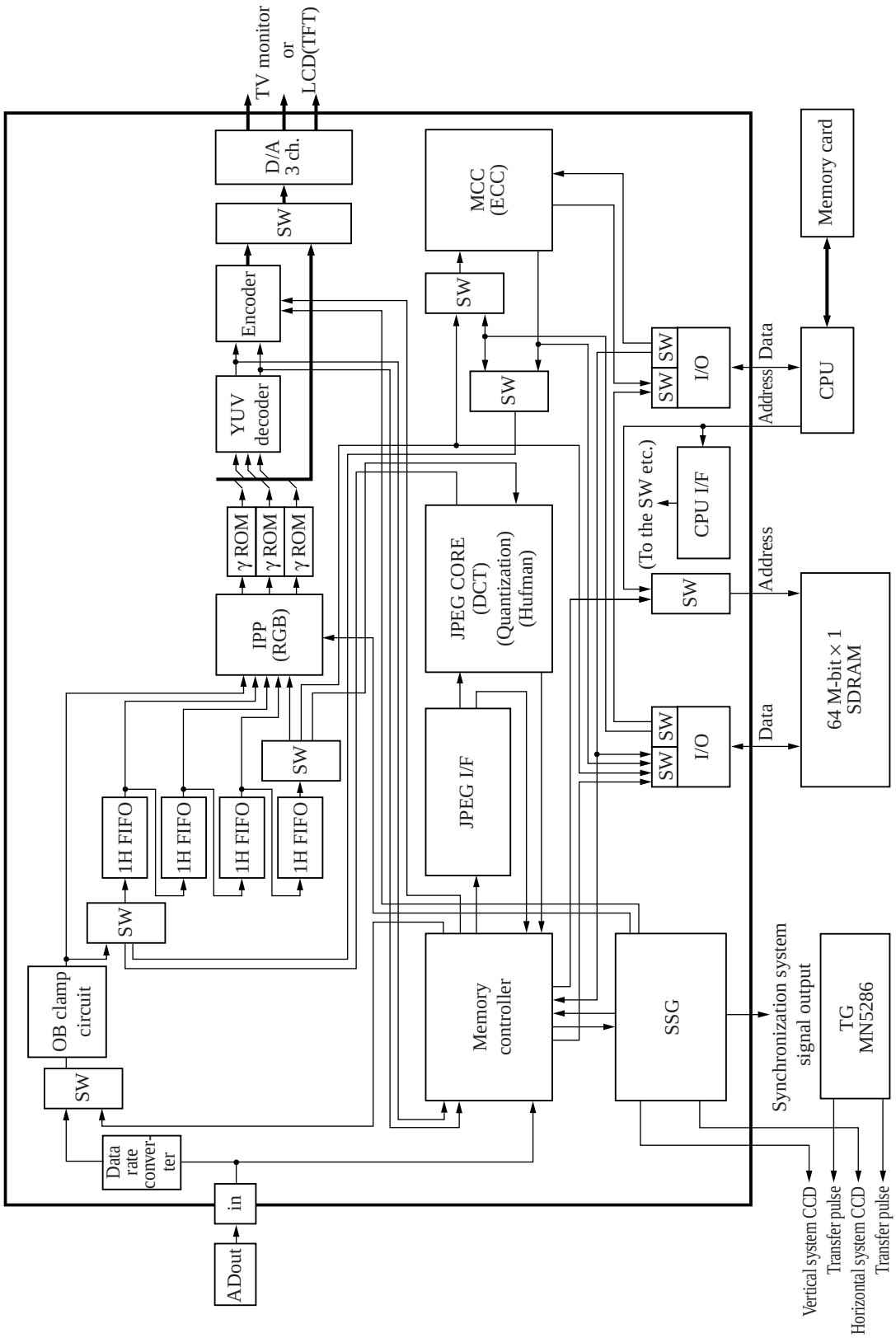
■ Features

- Supports both NTSC and PAL with a single 49.5 MHz oscillator.
- Real-time monitoring with an image refresh rate of 30 Hz (25 Hz for PAL)
- Integrates all functions from analog-to-digital signal input to JPEG input and output, and a monitor output, on a single chip. Supports JPEG compression and expansion.
- Implements the highest image quality in its class with new Matsushita-developed image-processing technologies.
- Maximum speed of under 1 second for all processing from full-resolution imaging through JPEG compression (Slightly over 800 ms, not including storing the data to the recording media.)
- Fine mode function that reduces the amount of data to 1/4 that for full resolution.
- Supports panorama mode with an aspect ratio of 1:3 (V:H)
- Provides a teleconferencing mode that can extract and store an arbitrary VGA resolution subset of the full resolution image.
- Thumbnail signal generation and processing function

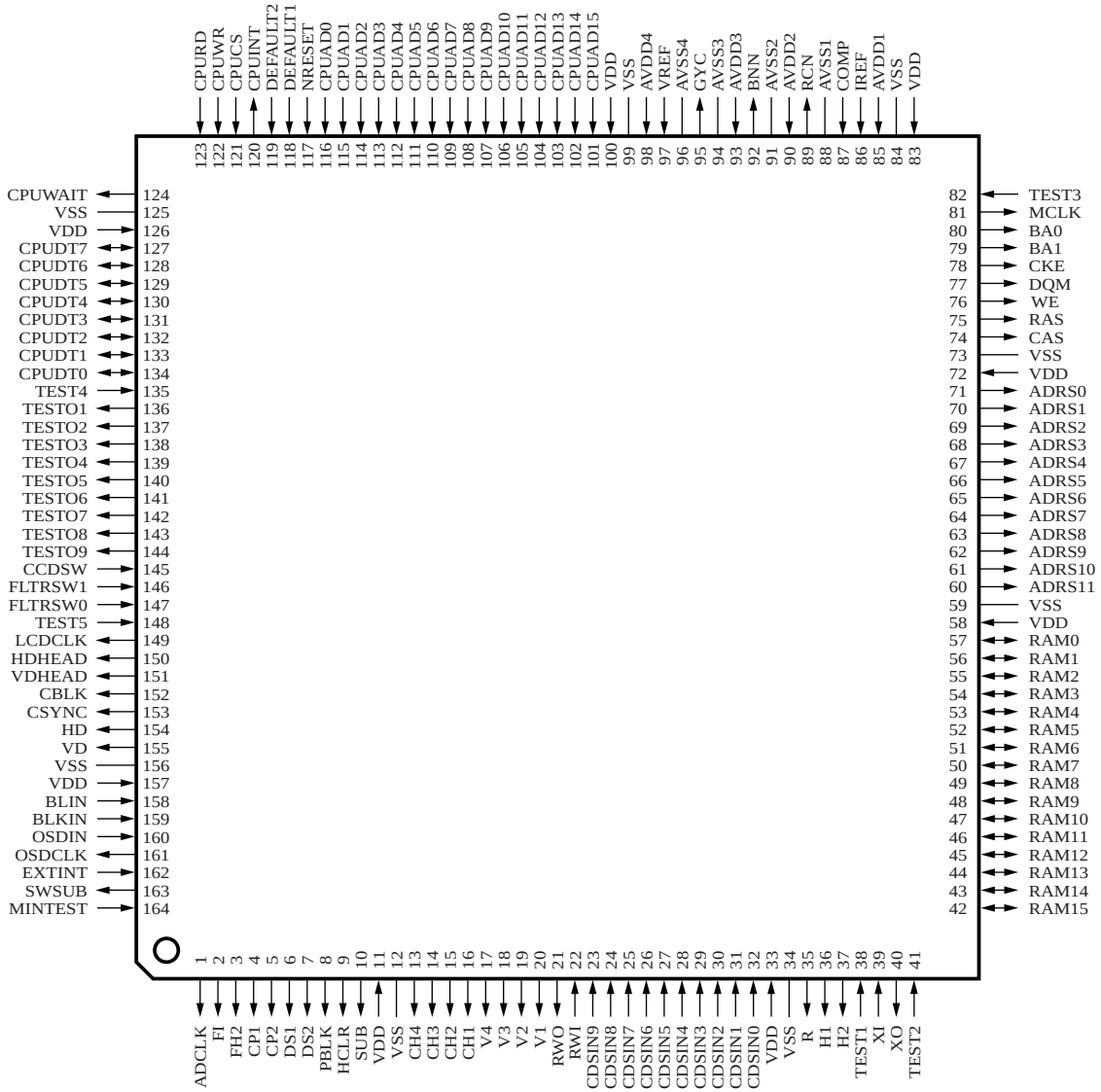
■ Applications

- Digital still cameras, cameras for use in FA and OA applications

■ Block Diagram



■ Pin Arrangement



(TOP VIEW)

■ Pin Descriptions

Pin No.	Pin Name	I/O	Function	Descriptions	
1	ADCLK	O	A/D converter clock	Clock used for the A/D converter. 24.75 MHz clock synchronized with HDHEAD (front side)	
2	FI	O	Field index	Low for odd fields, high for even fields, and synchronized with interlaced scanning CCD.	
3	FH2	O	Line index	Outputs a low for the GR line signal and high for the BG line signal in the CDS data input.	
4	CP1	O	Optical black clamp	Clamps the optical black level of the CCD output input to the CDS chip.	
5	CP2	O	Clamp pulse	Output immediately after the stop of CCD horizontal transfer. This signal is normally not needed.	
6	DS1	O	CDS pulse 1	Clamps the optical black level of the CCD output. Input to the CDS chip.	
7	DS2	O	CDS pulse 2	Clamps the signal component of the CCD output and inputs that level to the CDS chip.	
8	PBLK	O	Pre-blanking pulse	Blanking signal used for preprocessing for the horizontal return period.	
9	HCLR	O	CCD horizontal transfer stop period	Outputs a high level during the horizontal CCD transfer stop period.	
10	SUB	O	Electronic shutter CCDSUB pulse	Sweeps out unnecessary charge from the CCD substrate during electronic shutter operation.	
11	VDD	I	Digital system power supply (3.3 V)		
12	VSS	I	Digital system ground		
13	CH4	O	Test output	Open	
14	CH3	O	DCLK (external TG interface)	Mode setting clock output	
15	CH2	O	DATA (external TG interface)	Mode setting data output	
16	CH1	O	CS (external TG interface)	Chip select	
17	V4	O	Test outputs	Open	
18	V3	O			
19	V2	O			
20	V1	O			
21	RWO	O	Test outputs	Open	
22	RWI	I	Test inputs	Connect to ground.	
23	CDSIN9	I	CDS data inputs	CDS data input (MSB).	CDS sampling is applied to the CCD output and those levels are A/D converted with 10-bit resolution.
24	CDSIN8	I		CDS data input (bit 9).	
25	CDSIN7	I		CDS data input (bit 8).	
26	CDSIN6	I		CDS data input (bit 7).	
27	CDSIN5	I		CDS data input (bit 6).	

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Function	Descriptions	
28	CDSIN4	I	CDS data inputs	CDS data input (bit 5).	CDS sampling is applied to the CCD output and those levels are A/D converted with 10-bit resolution.
29	CDSIN3	I		CDS data input (bit 4).	
30	CDSIN2	I		CDS data input (bit 3).	
31	CDSIN1	I		CDS data input (bit 2).	
32	CDSIN0	I		CDS data input (LSB).	
33	VDD	I	Digital system power supply (3.3 V)		
34	VSS	I	Digital system ground		
35	R	O	Test output	Open	
36	H1	O	Test output	Open	
37	H2	O			
38	TEST1	I	Test input	Must be held low during normal operation.	
39	XI	I	Crystal oscillator element input	Input	
40	XO	O	and output	Output	
41	TEST2	I	Test input	Must be held low during normal operation.	
42	RAM15	I/O	SDRAM data I/O	[MSB]	
43	RAM14	I/O		Bit 15	
44	RAM13	I/O		Bit 14	
45	RAM12	I/O		Bit 13	
46	RAM11	I/O		Bit 12	
47	RAM10	I/O		Bit 11	
48	RAM9	I/O		Bit 10	
49	RAM8	I/O		Bit 9	
50	RAM7	I/O		Bit 8	
51	RAM6	I/O		Bit 7	
52	RAM5	I/O		Bit 6	
53	RAM4	I/O		Bit 5	
54	RAM3	I/O		Bit 4	
55	RAM2	I/O		Bit 3	
56	RAM1	I/O		Bit 2	
57	RAM0	I/O		[LSB]	
58	VDD	I	Digital system power supply (3.3 V)		
59	VSS	I	Digital system ground		

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Function	Descriptions
60	ADRS11	O	SDRAM address outputs	[MSB]
61	ADRS10	O		Bit 11
62	ADRS9	O		Bit 10
63	ADRS8	O		Bit 9
64	ADRS7	O		Bit 8
65	ADRS6	O		Bit 7
66	ADRS5	O		Bit 6
67	ADRS4	O		Bit 5
68	ADRS3	O		Bit 4
69	ADRS2	O		Bit 3
70	ADRS1	O		Bit 2
71	ADRS0	O		[LSB]
72	VDD	I	Digital system power supply (3.3 V)	
73	VSS	I	Digital system ground	
74	CAS	O	SDRAM control outputs	RAMCOL address-enable signal
75	RAS	O		RAMROW address-enable signal
76	WE	O		RAM write-enable signal
77	DQM	O		RAM data mask: for monitoring
78	CKE	O		RAM clock enable
79	BA1	O		RAM bank selection
80	BA0	O		
81	MCLK	O	Master clock output1	
82	TEST3	I	Test input	Must be held low during normal operation.
83	VDD	I	Digital system power supply (3.3 V)	
84	VSS	I	Digital system ground	
85	AVDD1	I	Analog system power supply (3.3 V)	If possible, a separate power supply system should be used.
86	IREF	I	D/A converter control input	D/A converter current-reference input
87	COMP	I	D/A converter control input	D/A converter comparator-voltage input
88	AVSS1	I	Analog system ground	If possible, a separate power supply system should be used.
89	RCN	O	Analog signal output	Outputs the R signal in RGB mode, the color difference signal (C) in component mode, and is unused in video output mode.
90	AVDD2	I	Analog system power supply (3.3 V)	If possible, a separate power supply system should be used.
91	AVSS2	I	Analog system ground	If possible, a separate power supply system should be used.
92	BNN	O	Analog signal output	Outputs the B signal in RGB mode, the luminance signal (Y) in component mode, and the V signal in video mode.
93	AVDD3	I	Analog system power supply (3.3 V)	If possible, a separate power supply system should be used.
94	AVSS3	I	Analog system ground	If possible, a separate power supply system should be used.

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Function	Descriptions
95	GYC	O	Analog signal output	Outputs the G signal in RGB mode, the luminance signal (Y) in component mode, and the V signal in video mode.
96	AVSS4	I	Analog system ground	If possible, a separate power supply system should be used.
97	VREF	I	D/A converter control input	D/A converter reference-voltage input
98	AVDD4	I	Analog system power supply (3.3 V)	If possible, a separate power supply system should be used.
99	VSS	I	Digital system ground	
100	VDD	I	Digital system power supply (3.3 V)	
101	CPUAD15	I	CPU interface	CPU address bus (MSB)
102	CPUAD14	I		CPU address bus (bit 15)
103	CPUAD13	I		CPU address bus (bit 14)
104	CPUAD12	I		CPU address bus (bit 13)
105	CPUAD11	I		CPU address bus (bit 12)
106	CPUAD10	I		CPU address bus (bit 11)
107	CPUAD9	I		CPU address bus (bit 10)
108	CPUAD8	I		CPU address bus (bit 9)
109	CPUAD7	I		CPU address bus (bit 8)
110	CPUAD6	I		CPU address bus (bit 7)
111	CPUAD5	I		CPU address bus (bit 6)
112	CPUAD4	I		CPU address bus (bit 5)
113	CPUAD3	I		CPU address bus (bit 4)
114	CPUAD2	I		CPU address bus (bit 3)
115	CPUAD1	I		CPU address bus (bit 2)
116	CPUAD0	I		CPU address bus (MSB)
117	NRESET	I	Hardware reset	Low active input
118	DEFAULT1	I	Default pin 1	Must be held low during normal operation.
119	DEFAULT2	I	Default pin 2	Must be held low during normal operation.
120	CPUINT	O	CPU interface	CPU interrupt signal output
121	CPUCS	I		Chip select
122	CPUWR	I		CPU data-bus write signal input
123	CPURD	I		CPU data-bus read signal input
124	CPUWAIT	O		DRAM refresh flag
125	VSS	I	Digital system ground	
126	VDD	I	Digital system power supply (3.3 V)	
127	CPUDT7	I/O	CPU interface	CPU data bus (MSB)
128	CPUDT6	I/O		CPU data bus (bit 7)
129	CPUDT5	I/O		CPU data bus (bit 6)
130	CPUDT4	I/O		CPU data bus (bit 5)

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Function	Descriptions
131	CPUDT3	I/O	CPU interface	CPU address bus (bit 4)
132	CPUDT2	I/O		CPU address bus (bit 3)
133	CPUDT1	I/O		CPU address bus (bit 2)
134	CPUDT0	I/O		CPU address bus (LSB)
135	TEST4	I	Test input	Must be held low during normal operation.
136	TESTO1	O	Test output	Open
137	TESTO2	O		
138	TESTO3	O		
139	TESTO4	O		
140	TESTO5	O		
141	TESTO6	O		
142	TESTO7	O		
143	TESTO8	O		
144	TESTO9	O		
145	CCDSW	I	CCD switch	Must be held low during normal operation.
146	FLTRSW1	I	CCD color filter phase adjustment switch	Must be held low during normal operation.
147	FLTRSW0	I		
148	TEST5	I	Test input	Must be held low during normal operation.
149	LCDCLK	O	LCD clock	Outputs the master clock (49.5 MHz) divided by 4. 12.375 MHz
150	HDHEAD	O	Frame horizontal synchronizing signal	CCD (TG) horizontal synchronizing signal (This differs from a TV horizontal synchronizing signal.)
151	VDHEAD	O	Frame vertical synchronizing signal	CCD (TG) vertical synchronizing signal (This differs from a TV vertical synchronizing signal.)
152	CBLK	O	Composite blanking	Composite (horizontal and vertical) blanking signal that conforms to the NTSC and PAL standards.
153	CSYNC	O	Composite synchronization signal	Composite (horizontal and vertical) synchronization signal that conforms to the NTSC and PAL standards.
154	HD	O	Horizontal synchronizing signal (TV)	Horizontal synchronizing signal that conforms to the NTSC and PAL standards.
155	VD	O	Vertical synchronizing signal (TV)	Vertical synchronizing signal that conforms to the NTSC and PAL standards.
156	VSS	I	Digital system ground	
157	VDD	I	Digital system power supply (3.3 V)	
158	BLIN	I	OSD interface	Blue background-mode setting
159	BLKIN	I		OSD blanking signal input
160	OSDIN	I		OSD signal input
161	OSDCLK	O		Clock for the OSD IC Outputs the master clock (49.5 MHz) divided by 8.

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Function	Descriptions
162	EXTINT	I	External TG switching	Must be held high during normal operation.
163	SWSUB	O	Drive mode discrimination pulse	Unused. This pin should be left open.
164	MINTEST	I	Test input	Must be held low during normal operation.

■ Electrical Characteristics

1. Absolute Maximum Ratings

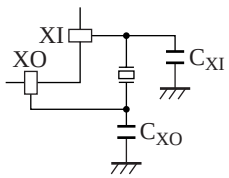
Parameter	Symbol	Rating	Unit
Supply voltage(digital)	DV_{DD}	– 0.3 to +4.6	V
Supply voltage(analog)	AV_{DD}	– 0.3 to +4.6	V
Input pins voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output pins voltage	V_O	– 0.3 to V_{DD}+0.3	V
Output current (2 mA pins)	I_O	±6	mA
Output current (4 mA pins)		±12	
Output current (16 mA pins)		±48	
Power dissipation	P_D	1 050	mW
Operating temperature	T_{opr}	–20 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. All of the DVDD, AVDD, DVSS,and AVSS pins must be directly connected externally to the power supply or ground, respectively.

2. Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage(digital)	DV_{DD}		3.0	3.3	3.6	V
Supply voltage(analog)	AV_{DD}		3.0	3.3	3.6	V
Ambient temperature	T_a		0	—	70	°C
Oscillator frequency	f_{OSC}	Xtal = 49.5 MHz	—	49.5	—	MHz
Recommended external	C_{XI}	V_{DD} = 3.3 V	—	22	—	pF
capacitor values *	C_{XO}	A feedback resistor is built in.	—	22	—	



Note) *: The oscillator characteristics depend on the type of the oscillator element used, external capacitors, and other factors. Consult the manufacturer of the oscillator element used to determine the oscillator circuit component values.

■ Electrical Characteristics (continued)

3. DC Characteristics at $DV_{DD} = AV_{DD} = 3.0$ V to 3.6 V, $DV_{SS} = AV_{SS} = 0$ V, $f_{OSC} = 49.5$ MHz, $T_a = 0°C$ to $70°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating supply current	I_{DD}	$V_I = V_{DD}$ or V_{SS} $V_{DD} = 3.3$ V, with the output pins open.	—	190	285	mA
Input pins 1: CMOS level pins RWI, BLIN, TEST1 to TEST5, BLKIN, CCDSW, CDSIN0 to CDSIN9, CPUAD0 to CPUAD15, CPUCS, CPURD, CPUWR, OSDIN, EXTINT, FLTRSW0, FLTRSW1, NRESET, DEFAULT1, DEFAULT2						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	—	±5	µA
Input pins 2: CMOS level pins with pull-down resistor MINTEST						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
Output pins 1: Push-pull outputs (2 mA pins) V1 to V4, BA0, BA1, CH1 to CH4, CP1, CP2, FH2, FI, WE, CAS, CKE, DQM, RAS, RWO, SUB, ADRS0 to ADRS11, CBLK, HCLR, PBLK, CSYNC, SWSUB, TESTO1 to TESTO9, CPUINT, HDHEAD						
High-level output voltage	V_{OH}	$I_{OH} = -2.0$ mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = +2.0$ mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output pins 2: Push-pull outputs (4 mA pins) DS1, DS2, HD, VD, MCLK, ADCLK, LCDCLK, OSDCLK, VDHEAD						
High-level output voltage	V_{OH}	$I_{OH} = -4.0$ mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = +4.0$ mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output pins 3: Push-pull outputs (16 mA pins) H1, H2, R						
High-level output voltage	V_{OH}	$I_{OH} = -16.0$ mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = +16.0$ mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V

■ Electrical Characteristics (continued)

3. DC Characteristics at $DV_{DD} = AV_{DD} = 3.0$ V to 3.6 V, $DV_{SS} = AV_{SS} = 0$ V, $f_{OSC} = 49.5$ MHz, $T_a = 0°C$ to $70°C$ (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output pins 4: Three-state outputs (2 mA pins) CPUWAIT						
High-level output voltage	V_{OH}	$I_{OH} = -2.0$ mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = +2.0$ mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage	I_{LO}	V_O = High-impedance state $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}	—	—	±5	µA
I/O pins: CMOS level pins RAM0 to 15, CPUDT0 to CPUDT7						
Low-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
High-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
High-level output voltage	V_{OH}	$I_{OH} = -4.0$ mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = +4.0$ mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage	I_{LO}	V_O = High-impedance state $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}	—	±5	µA	
Oscillator pins XI, XO						
Standard oscillator frequency	f_{OSC}	$V_{DD} = 3.3$ V, using an external crystal	—	49.5	—	MHz
Internal feedback resistance	R_f	XI = V_{DD} or V_{SS} $V_{DD} = 3.3$ V	1.5	3.0	6.0	kΩ
High-level output current	I_{OH}	$V_{DD} = 3.3$ V, XI = XO = V_{SS}	30	60	120	mA
Low-level output current	I_{OL}	$V_{DD} = 3.3$ V, XI = XO = V_{DD}	30	60	120	mA

4. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input pin 1 XI						
Clock period	t_{cyc}	See figure 1.	—	20.2	—	ns
Clock duty factor	d_{clk}	See figure 1.	45	50	55	%
Input pins 2 CDSIN0 to CDSIN9, CPUAD0 to CPUAD15, CPUCS, CPURD, CPUWR, NRESET						
Input setup time	t_{su}	See figure 1.	5	—	—	ns
Input hold time	t_{hd}	See figure 1.	10	—	—	ns

■ Electrical Characteristics (continued)

3. AC Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output pins BA0, BA1, CH1 to CH3, CP1, FH2, FI, CAS, RAS, DS1, DS2, CBLK, HCLR, PBLK, CSYNC, CPUINT, HDHEAD, VDHEAD, HD, VD, ADRS0 to ADRS11, WE, CKE, CPUWAIT						
Output delay time	t_{od}	With a 70 pF load, and a 50% output level. See figure 1.	—	—	32	ns
Input/Output pins RAM0 to RAM15, CPUDT0 to CPUDT7						
Input setup time	t_{su}	See figure 1.	5	—	—	ns
Input hold time	t_{hd}	See figure 1.	10	—	—	ns
Output delay time	t_{od}	With a 70 pF load, and a 50% output level. See figure 1.	—	—	32	ns

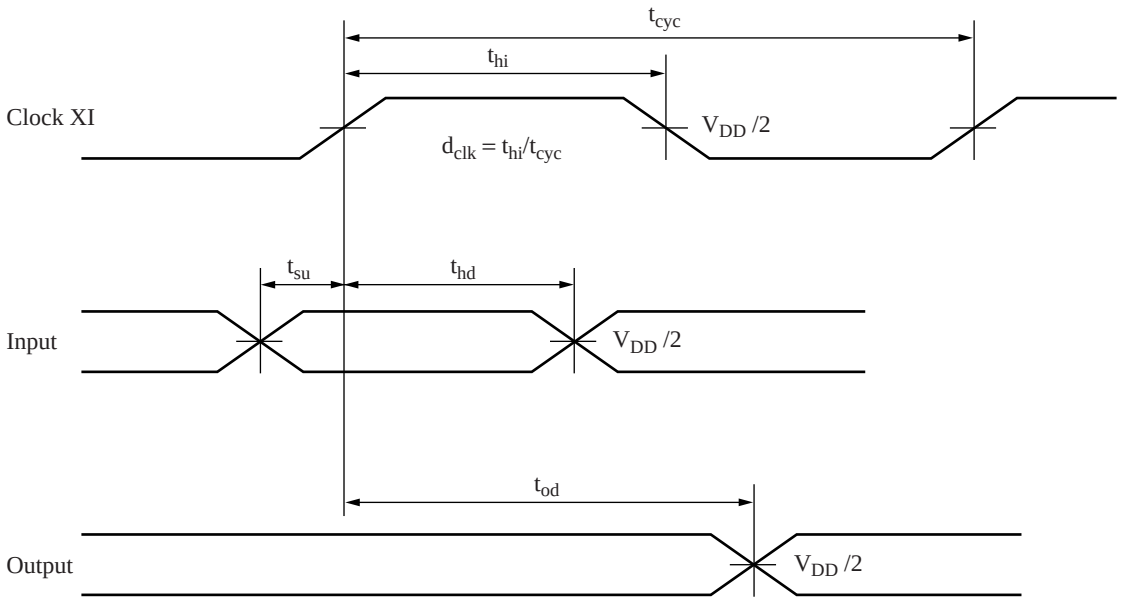


Figure 1. I/O Timing

■ Electrical Characteristics (continued)

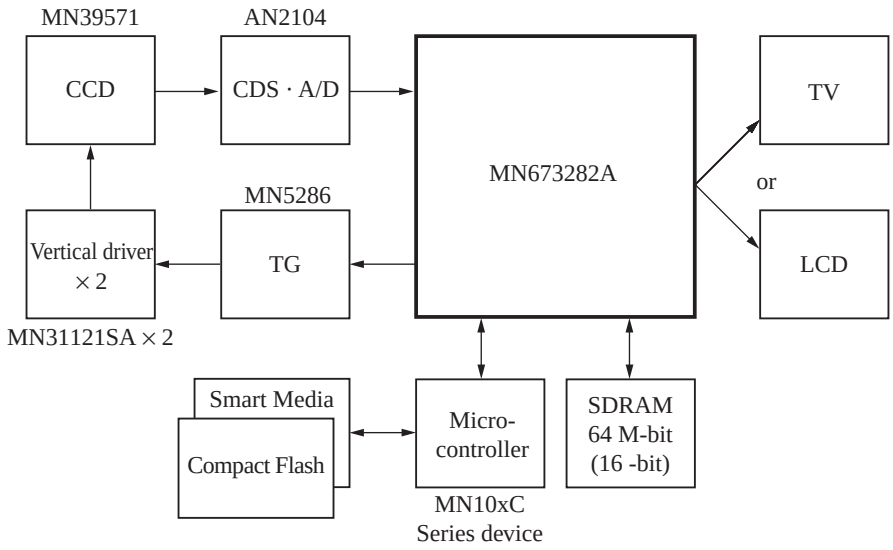
5. D/A Converter at $DV_{DD} = AV_{DD} = 3.3$ V, $DV_{SS} = AV_{SS} = 0$ V, $T_a = 0°C$ to $70°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Recommended D/A Converter Operating Conditions Analog input pins: IREF, VREF, COMP Analog output pins: RCN, BNN, GYC						
Reference voltage	V_{REF}		—	1.235	—	V
External phase compensation capacitor	C_{COMP}	Inserted between the COMP and AVDD pins.	—	1.0	—	µF
External output resistor	R_L	Inserted between the analog output and VSS pins.	—	200	—	Ω
External-bias current setting resistor	R_{IREF}	Inserted between the IREF and VSS pins.	—	31.6	—	kΩ
D/A converter characteristics						
Resolution	RES	$f_{clk} = 20.0$ MHz, $V_{DD} = 3.3$ V,	—	—	10	bit
Linearity error	INLE	$R_L = 200$ Ω, $R_{IREF} = 31.6$ kΩ,	—	±1.5	±2.5	LSB
Differential linearity error	DNLE	$V_{REF} = 1.235$ V	—	±1.0	±2.0	LSB
Full-scale output current	I_{FS}		4.5	5.0	5.5	mA
Full-scale output voltage setting range *	V_O		0.6	—	1.1	V

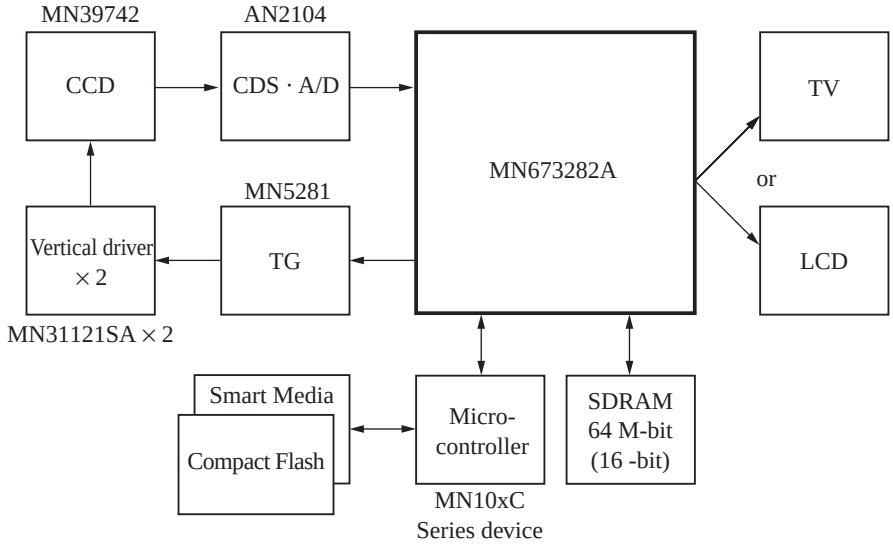
Note) * : This is the range over which output as a D/A converter is possible. Note that INLE, DNLE, and other characteristics are not guaranteed over this range.

■ Application Circuit Example

• Interlaced 2.31 megapixel CCD camera system structure

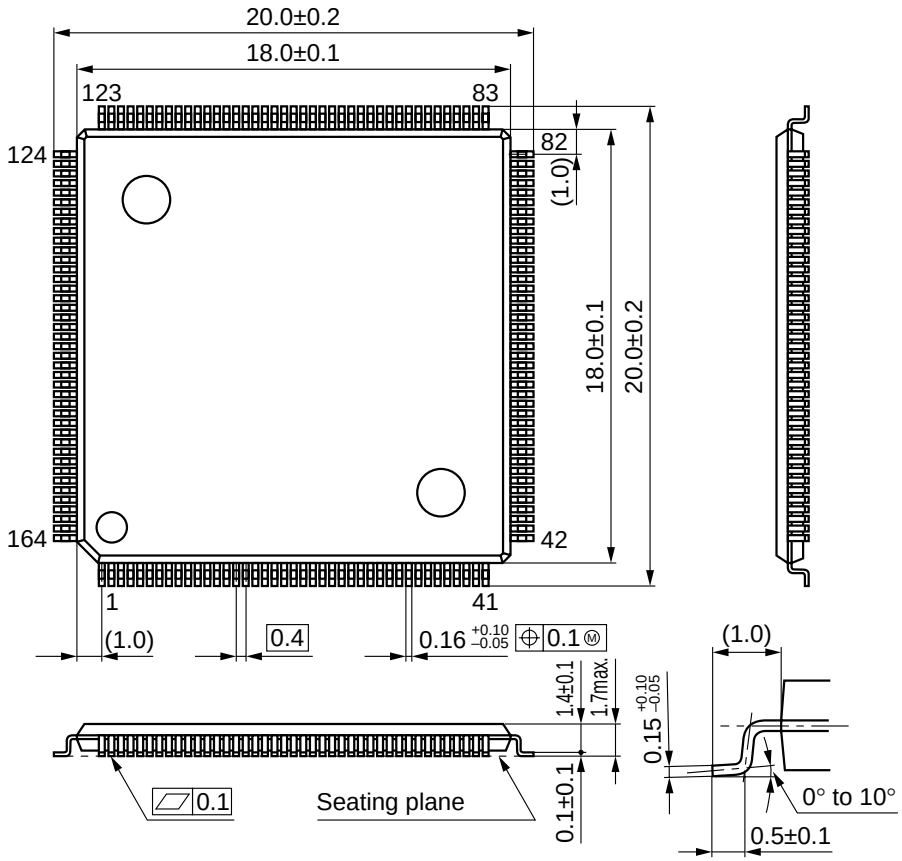


• Interlaced 1.33 megapixel CCD camera system structure



■ Package Dimensions (Unit: mm)

• LQFP164-P-1818



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