



## ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)<sup>1</sup> 25 °C

### Supply Voltages

Negative Supply Voltage ( $V_{EE}$  TO GND)  $-7.0$  to  $+0.5$  V  
 Ground Voltage Differential .....  $-0.5$  to  $+0.5$  V

### Input Voltage

Analog Input Voltage .....  $V_{EE}$  to  $+0.5$  V  
 Reference Input Voltage .....  $V_{EE}$  to  $+0.5$  V  
 Digital Input Voltage .....  $V_{EE}$  to  $+0.5$  V  
 Reference Current  $V_{RTF}$  to  $V_{RBF}$  ..... 25 mA

### Output

Digital Output Current ..... 0 to  $-30$  mA

### Temperature

Operating Temperature, ambient .....  $-25$  to  $+85$  °C  
 junction .....  $+150$  °C  
 Lead Temperature, (soldering 10 seconds) .....  $+300$  °C  
 Storage Temperature .....  $-65$  to  $+150$  °C

**Note:** 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

## ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{EE} = -5.2$  V,  $R_{Source} = 50 \Omega$ ,  $V_{RBF} = -2.00$  V,  $V_{R2} = -1.00$  V,  $V_{RTF} = 0.00$  V,  $f_{CLK} = 125$  MHz, Duty Cycle = 50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A			SPT7710B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>DC Accuracy</b>									
Integral Linearity Error	$f_{CLK} = 100$ kHz	VI	-0.75	$\pm 0.60$	+0.75	-0.95	$\pm 0.80$	+0.95	LSB
Differential Linearity Error	$f_{CLK} = 100$ kHz	VI	-0.75		+0.75	-0.95		+0.95	LSB
No missing codes			Guaranteed			Guaranteed			
<b>Analog Input</b>									
Offset Error $V_{RT}$		VI	-30		+30	-30		+30	mV
Offset Error $V_{RB}$		VI	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	Volts
Input Capacitance	Over full input range	V							pF
Input Resistance		V		10			10		k $\Omega$
Input Current		VI		250	500		250	500	$\mu$ A
Input Slew Rate		V		1,000			1,000		V/ $\mu$ s
Large Signal Bandwidth	$V_{IN} = F.S.$	V		210			210		MHz
Small Signal Bandwidth	$V_{IN} = 500$ mV <sub>P-P</sub>	V		335			335		MHz
Clock Synchronous Input Currents		V		40			40		$\mu$ A
<b>Reference Input</b>									
Ladder Resistance		VI	100	200	300	100	200	300	$\Omega$
Reference Bandwidth		V		10			10		MHz
<b>Timing Characteristics</b>									
Maximum Sample Rate		IV	125	150		125	150		MSPS
Clock to Data Delay		V		2.4			2.4		ns
Output Delay Tempco		V		2			2		ps/°C
CLK-to-Data Ready Delay ( $t_D$ )		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns
<b>Dynamic Performance</b>									
Signal-to-Noise Ratio	$f_{IN} = 3.58$ MHz	VI	46	48		45	47		dB
	$f_{IN} = 50$ MHz	VI	42	46		40	44		dB
Total Harmonic Distortion	$f_{IN} = 3.58$ MHz	VI		-52	-48		-50	-46	dB
	$f_{IN} = 50$ MHz	VI		-44	-40		-43	-39	dB
Signal-to-Noise and Distortion (SINAD)	$f_{IN} = 3.58$ MHz	VI	45	48		43	46		dB
	$f_{IN} = 50$ MHz	VI	39	42		37	40		dB

## ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{EE} = -5.2$  V,  $R_{Source} = 50 \Omega$ ,  $V_{RBF} = -2.00$  V,  $V_{R2} = -1.00$  V,  $V_{RTF} = 0.00$  V,  $f_{CLK} = 125$  MHz, Duty Cycle = 50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A			SPT7710B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>Digital Inputs</b>									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	Volts
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	Volts
Clock Low Width, $t_{PWL}$		VI		4	5		4	5	ns
Clock High Width, $t_{PWH}$		VI		4	5		4	5	ns
<b>Digital Outputs</b>									
Digital Output High Voltage	50 $\Omega$ to -2 V	VI	-1.1			-1.1			Volts
Digital Output Low Voltage	50 $\Omega$ to -2 V	VI			-1.5			-1.5	Volts
<b>Power Supply Requirements</b>									
Supply Current	+25 °C	VI		425	550		425	550	mA
Power Dissipation	+25 °C	VI		2.2	2.9		2.2	2.9	W

### TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

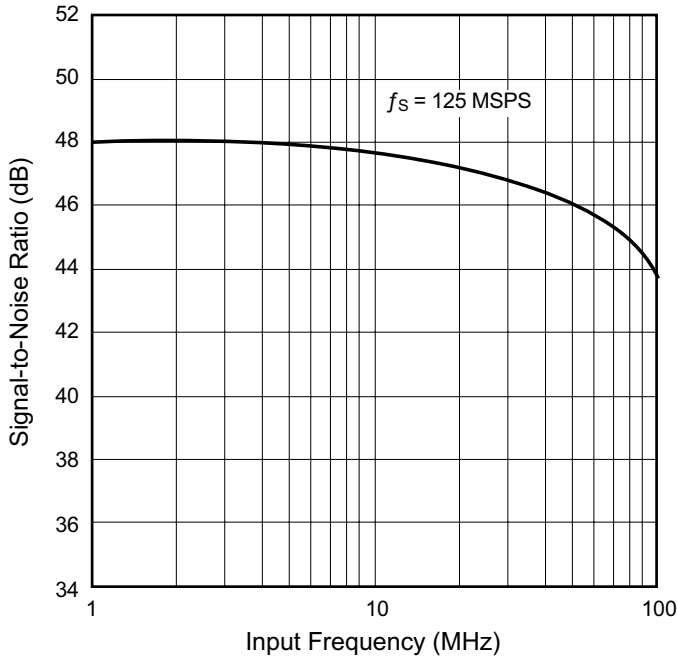
Unless otherwise noted, all test are pulsed tests; therefore,  $T_J = T_C = T_A$ .

### LEVEL TEST PROCEDURE

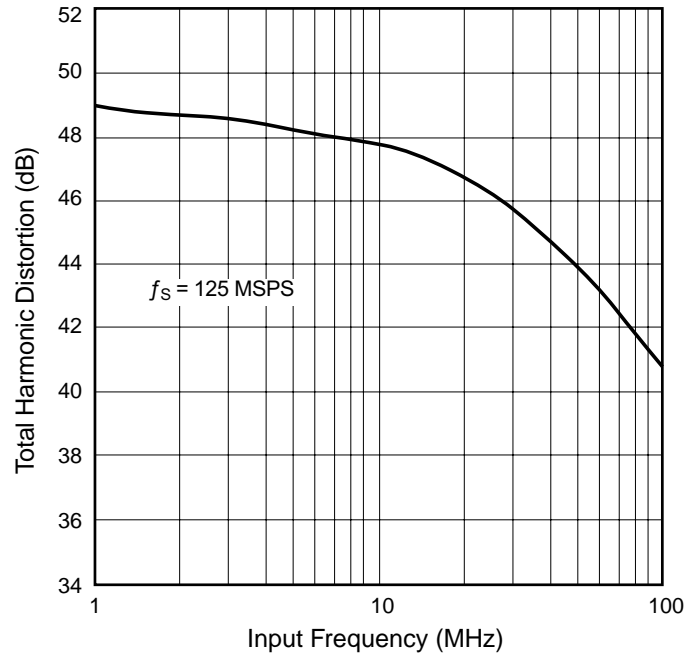
- I 100% production tested at the specified temperature.
- II 100% production tested at  $T_A = +25$  °C, and sample tested at the specified temperatures.
- III QA sample tested only at the specified temperatures.
- IV Parameter is guaranteed (but not tested) by design and characterization data.
- V Parameter is a typical value for information purposes only.
- VI 100% production tested at  $T_A = +25$  °C. Parameter is guaranteed over specified temperature range.

# TYPICAL PERFORMANCE CHARACTERISTICS

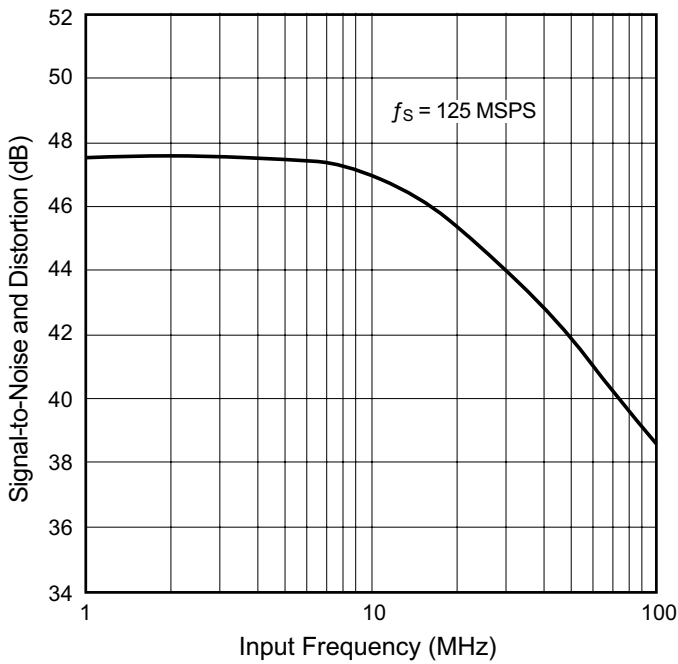
## SNR vs Input Frequency



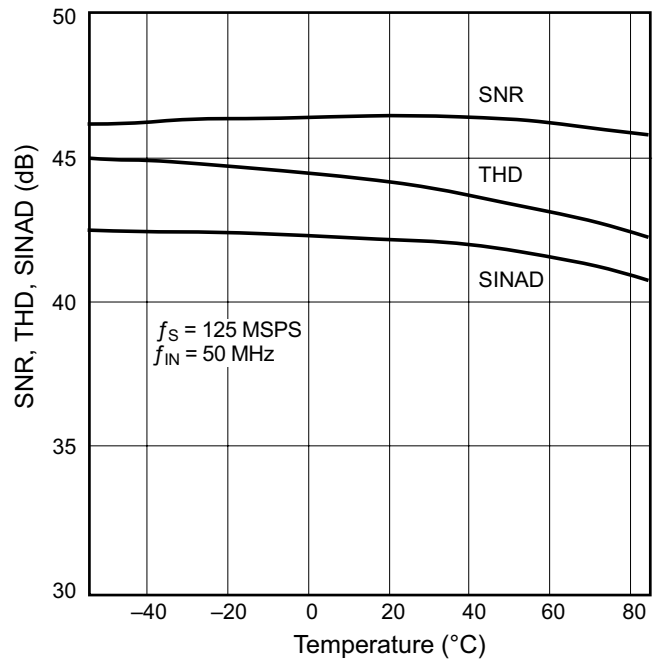
## THD vs Input Frequency



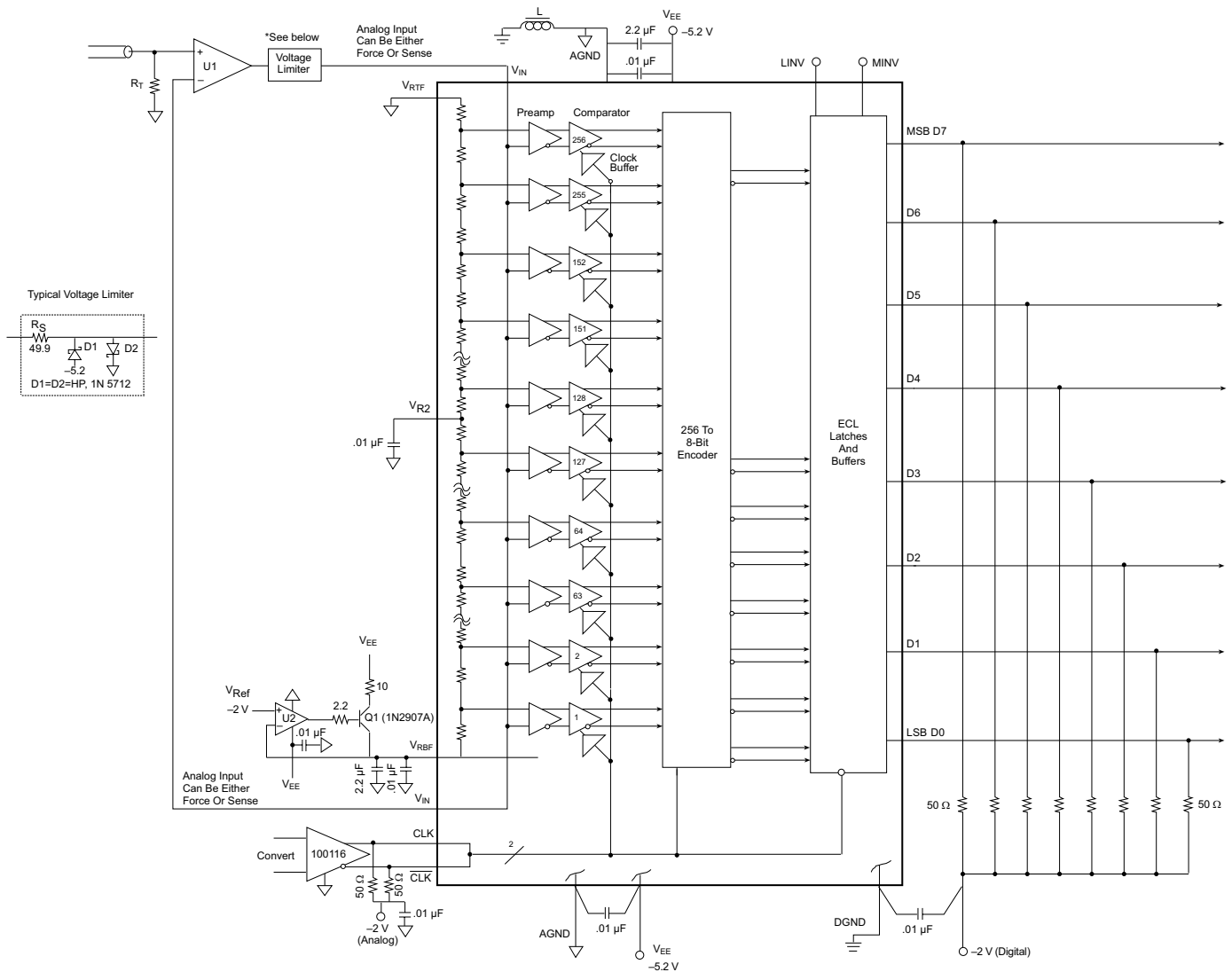
## SINAD vs Input Frequency



## SNR, THD, SINAD vs Temperature



**Figure 1 – Typical Interface Circuit 1**



**GENERAL DESCRIPTION**

The SPT7710 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant for varying input voltages and frequencies and, therefore, makes the part easier to drive than previous flash converters. The SPT7710 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

The SPT7710 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

**TYPICAL INTERFACE CIRCUIT**

The typical interface circuit is shown in figure 1. The SPT7710 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a



**Table I – Output Coding**

		BINARY		TWOs COMPLEMENT	
		TRUE	INVERTED	TRUE	INVERTED
ANALOG INPUT VOLTAGE	D8	MINV=LINV=0	MINV=LINV=1	MINV=1; LINV=0	MINV=0; LINV=1
		D7_____D0	D7_____D0	D7_____D0	D7_____D0
-2 V + 1/2 LSB	0	00000000 ↶ 00000001 ↶	11111111 ↶ 11111110 ↶	10000000 ↶ 10000001 ↶	01111111 ↶ 01111110 ↶
-1.0 V	0	01111111 ↶ 10000000 ↶	10000000 ↶ 01111111 ↶	11111111 ↶ 00000000 ↶	00000000 ↶ 11111111 ↶
0 V – 1/2 LSB	0	11111111 ↶ 11111110 ↶	00000000 ↶ 00000001 ↶	01111111 ↶ 01111110 ↶	10000000 ↶ 10000001 ↶
≥0 V	1	11111111	00000000	01111111	10000000

the same source. The SPT7710 is superior to similar devices, due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. An optional input buffer may be used.

**CLK,  $\overline{\text{CLK}}$  (CLOCK INPUTS)**

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since  $\overline{\text{CLK}}$  is internally biased to -1.3 V. (See clock input circuit.)  $\overline{\text{CLK}}$  may be left open, but a .01  $\mu\text{F}$  bypass capacitor from  $\overline{\text{CLK}}$  to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

**MINV, LINV (OUTPUT LOGIC CONTROL)**

These are ECL-compatible digital controls for changing the output code from straight binary to two’s complement, etc. For more information, see table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 k $\Omega$  resistor.

**D0 TO D7 (DIGITAL OUTPUTS)**

The digital outputs can drive ECL levels into 50  $\Omega$  when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 150  $\Omega$  to 1 k $\Omega$  loads.

**$V_{\text{RBF}}$ ,  $V_{\text{R2}}$ ,  $V_{\text{RTF}}$  (REFERENCE INPUTS)**

There are two reference inputs and one external reference voltage tap. These are -2 V ( $V_{\text{RBF}}$ ), mid-tap ( $V_{\text{R2}}$ ), and AGND ( $V_{\text{RTF}}$ ). The reference pins can be driven as shown in figure 1.  $V_{\text{R2}}$  should be bypassed to AGND for further noise suppression.

**$V_{\text{RBF}}$ ,  $V_{\text{RBS}}$ ,  $V_{\text{R1}}$ ,  $V_{\text{R2}}$ ,  $V_{\text{R3}}$ ,  $V_{\text{RTF}}$ ,  $V_{\text{RTS}}$  REFERENCE INPUTS (PGA AND CERQUAD PACKAGES ONLY)**

These are five external reference voltage taps from -2 V ( $V_{\text{RBF}}$ ) to AGND ( $V_{\text{RTF}}$ ) that can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired.  $V_{\text{RB}}$  and  $V_{\text{RT}}$  have force and sense pins for monitoring the top and bottom voltage references.

**N/C**

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

**DREAD – DATA READY; DRINV – DATA READY INVERSE (PGA AND CERQUAD PACKAGES ONLY)**

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7710’s decoders and latches. This function is useful for interfacing with high-speed memory. Using the data ready output to latch the output data ensures minimum set-up and hold times. DRINV is a data ready inverse control pin. (See the timing diagram.)

**D8 – OVERRANGE (PGA AND CERQUAD PACKAGES ONLY)**

This is an overrange function. When the SPT7710 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7710 into higher resolution systems.

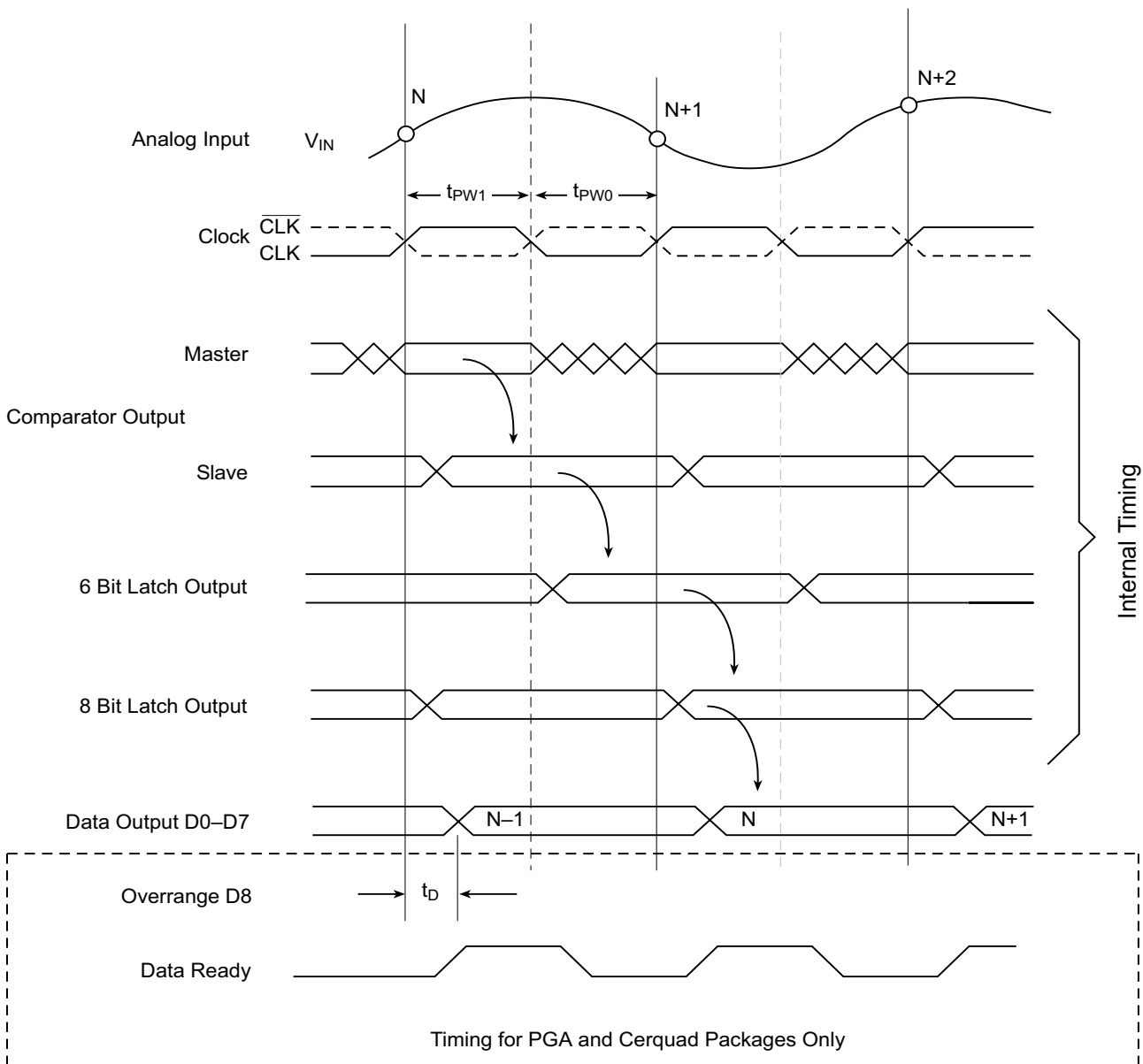
## OPERATION

The SPT7710 has 256 preamp/comparator pairs that are each supplied with the voltage from  $V_{RTF}$  to  $V_{RBF}$  divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at  $V_{IN}$  is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in

sequence from the top comparators, closest to  $V_{RTF}$  (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low.

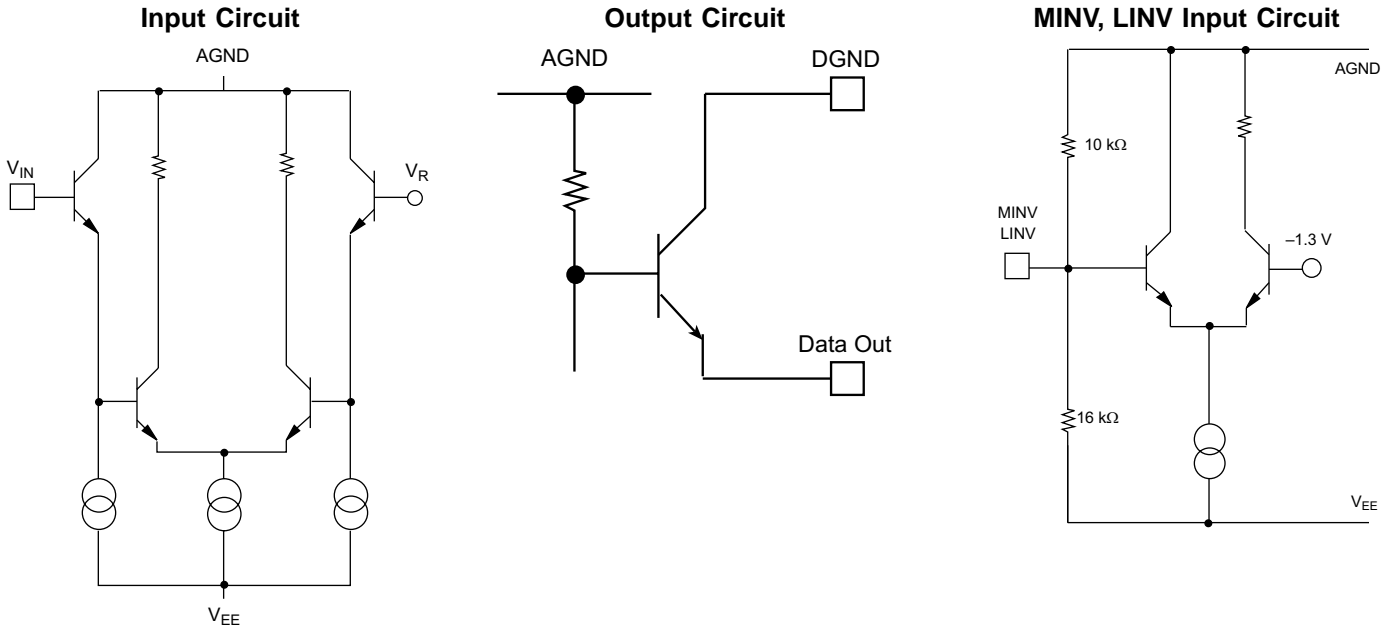
At the output of the decoders is a set of four 7-bit latches that are enabled (*track*) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns, and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions, which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 3 – Timing Diagram

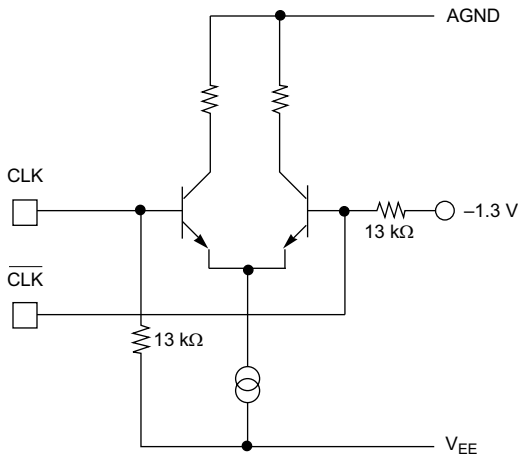




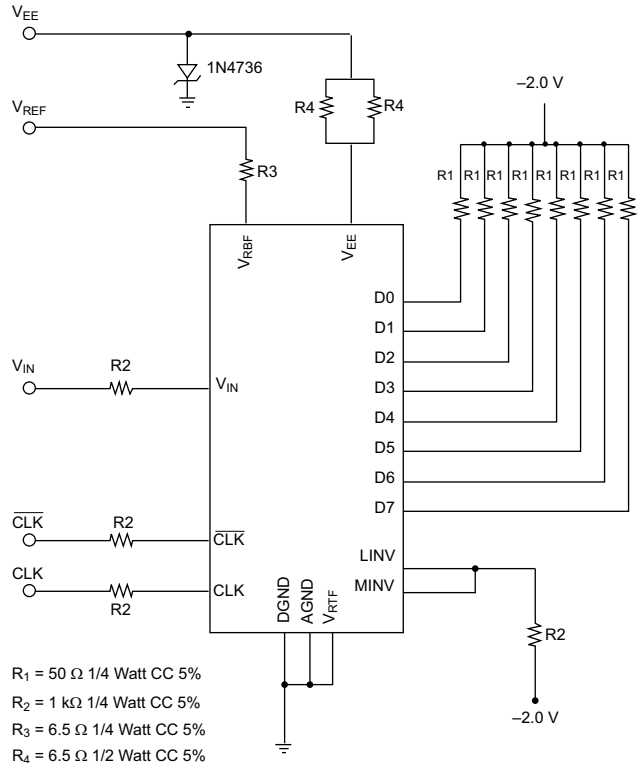
**Figure 4 – Subcircuit Schematics**



**Figure 5 – Clock Input**



**Figure 6 – Burn-In Circuit (42-lead DIP Package only)**



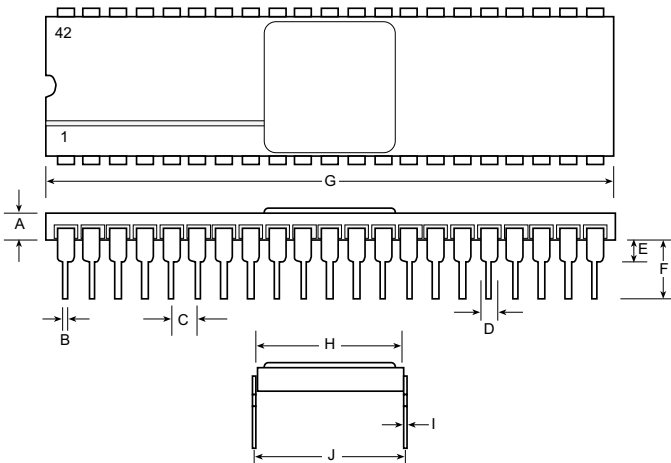
- $R_1 = 50 \Omega$  1/4 Watt CC 5%
- $R_2 = 1 k\Omega$  1/4 Watt CC 5%
- $R_3 = 6.5 \Omega$  1/4 Watt CC 5%
- $R_4 = 6.5 \Omega$  1/2 Watt CC 5%
- $V_{REF} = -2.0$  Volts
- $V_{EE} = -6.6$  Volts

**EVALUATION BOARDS**

The EB7710 evaluation board is available to aid designers in demonstrating the full performance of the SPT7710. This board includes a voltage reference circuit, clock driver circuit, output data latches, and an on-board reconstruction of the digital data. An application note describing the operation of this board, as well as application tips, is also available. Contact the factory for price and delivery.

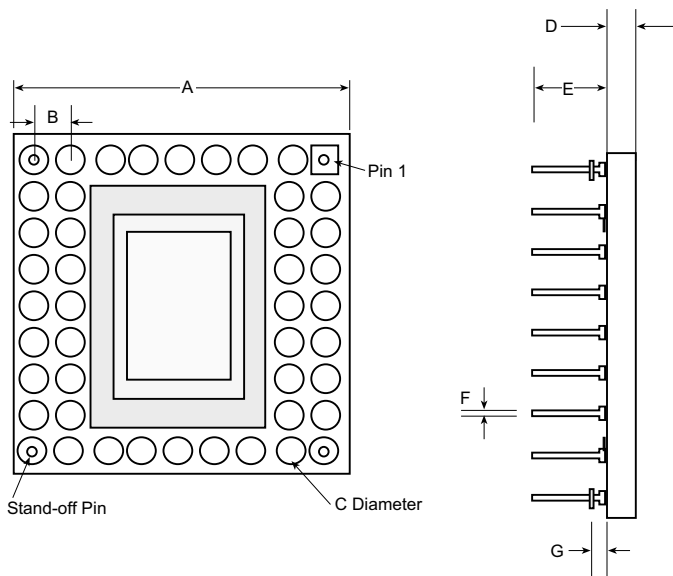
## PACKAGE OUTLINES

### 42-Lead Sidebraced DIP



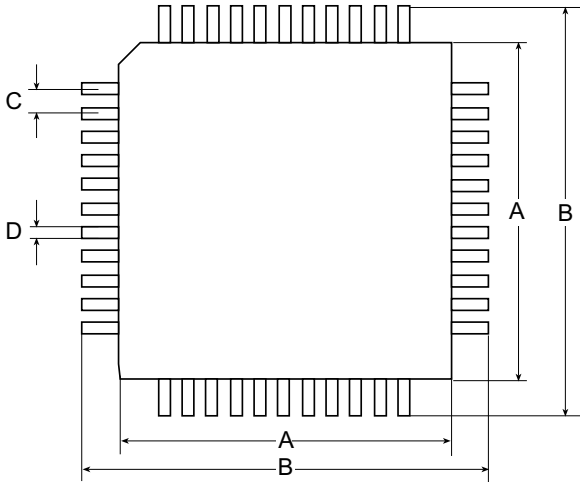
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D	.050 typ		1.27	
E	.050 typ		1.27	
F	0.275		6.99	
G	2.080	2.120	52.83	53.85
H	0.585	0.605	14.86	15.37
I	0.008	0.015	0.20	0.38
J	0.600	0.620	15.24	15.75

### 46-Lead Pin Grid Array



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.100 typ		2.54 typ	
C	.045 dia	.055 dia	1.14	1.40
D	0.084	0.096	2.13	2.44
E	0.169	0.193	4.29	4.90
F	.020 dia	.030 dia	0.51	0.76
G	.050 typ		1.27 typ	

### 44-Lead Cerquad



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.550 typ		13.97 typ	
B	0.685	0.709	17.40	18.00
C	0.037	0.041	0.94	1.04
D	0.016 typ		0.41 typ	
E	0.008 typ		0.20 typ	
F	0.027	0.051	0.69	1.30
G	0.006 typ		0.15 typ	
H	0.080	0.089	2.03	2.26

