# 2SK2788

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

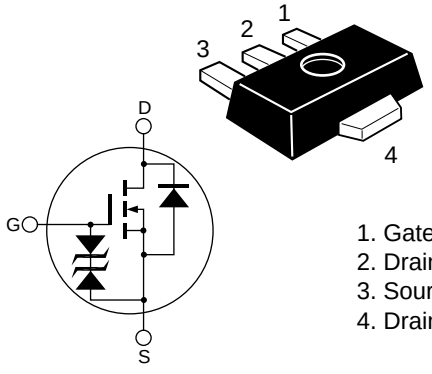
ADE-208-538
1st. Edition

## Features

- Low on-resistance
  $R_{DS(on)}$ = 0.12Ω typ ($V_{GS}$ = 10 V, $I_D$ = 1 A)
- Low drive current
- High speed switching
- 4V gate drive devices.

## Outline

UPAK




1. Gate
2. Drain
3. Source
4. Drain

Hitachi semiconductor

## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 60 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ | 2 | A |
| Drain peak current | $I_{D(pulse)}$*[1] | 4 | A |
| Body to drain diode reverse drain current | $I_{DR}$ | 2 | A |
| Channel dissipation | Pch*[2] | 1 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

Notes: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

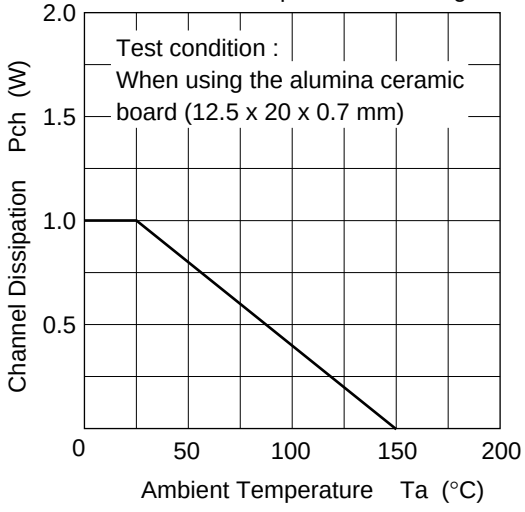
## Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 60 | — | — | V | $I_D$ = 10mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±20 | — | — | V | $I_G$ = ±100µA, $V_{DS}$ = 0 |
| Zero gate voltege drain current | $I_{DSS}$ | — | — | 10 | µA | $V_{DS}$ = 60 V, $V_{GS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±16V, $V_{DS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.0 | — | 2.0 | V | $I_D$ = 1mA, $V_{DS}$ = 10V |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.12 | 0.16 | Ω | $I_D$ = 1 A, $V_{GS}$ = 10V*[1] |
| | $R_{DS(on)}$ | — | 0.16 | 0.25 | Ω | $I_D$ = 1A, $V_{GS}$ = 4V*[1] |
| Forward transfer admittance | $\|y_{fs}\|$ | 1.6 | 2.8 | — | S | $I_D$ = 1A, $V_{DS}$ = 10V*[1] |
| Input capacitance | Ciss | — | 180 | — | pF | $V_{DS}$ = 10V |
| Output capacitance | Coss | — | 90 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 30 | — | pF | f = 1MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 9 | — | ns | $V_{GS}$ = 10V, $I_D$ = 1A |
| Rise time | $t_r$ | — | 15 | — | ns | $R_L$ = 30Ω |
| Turn-off delay time | $t_{d(off)}$ | — | 40 | — | ns | |
| Fall time | $t_f$ | — | 35 | — | ns | |
| Body to drain diode forward voltage | $V_{DF}$ | — | 0.9 | — | V | $I_D$ = 2A, $V_{GS}$ = 0 |
| Body to drain diode reverse recovery time | $t_{rr}$ | — | 35 | — | ns | $I_F$ = 2A, $V_{GS}$ = 0<br>$di_F/dt$ = 50A/µs |

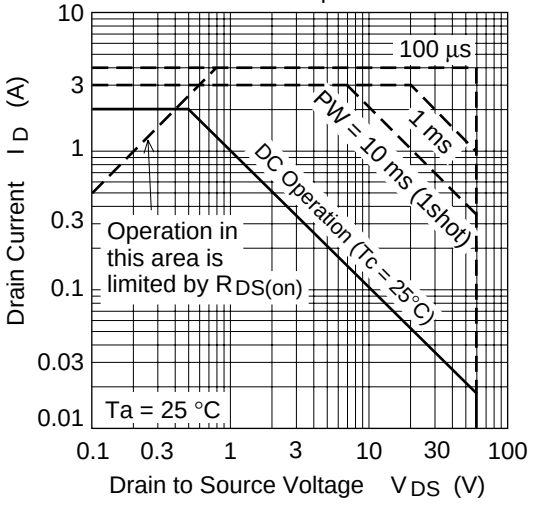
Notes: 1. Pulse test
2. Marking is “VY”

## Main Characteristics

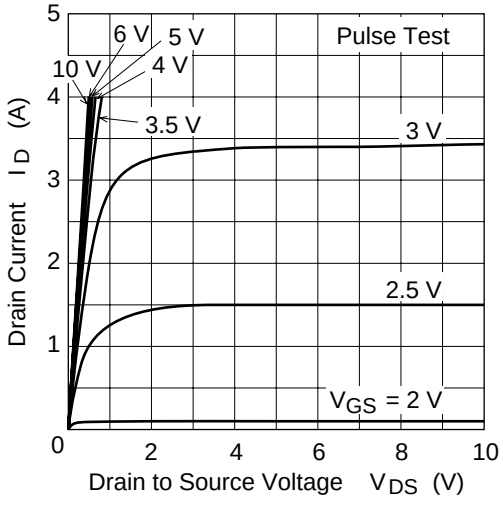
Power vs. Temperature Derating



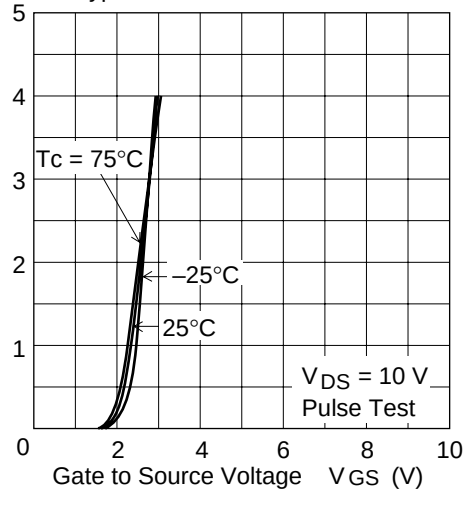

Maximum Safe Operation Area



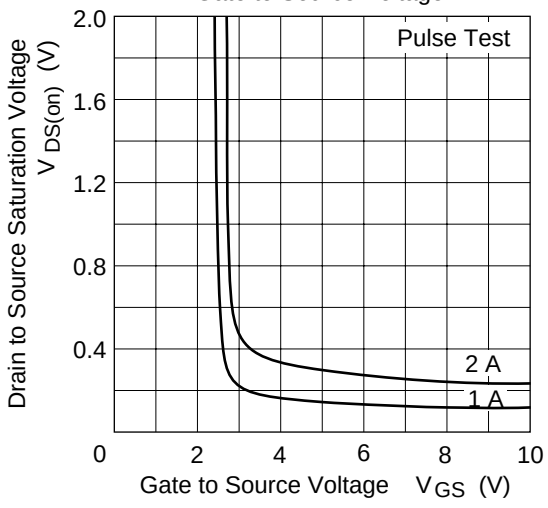

Typical Output Characteristics



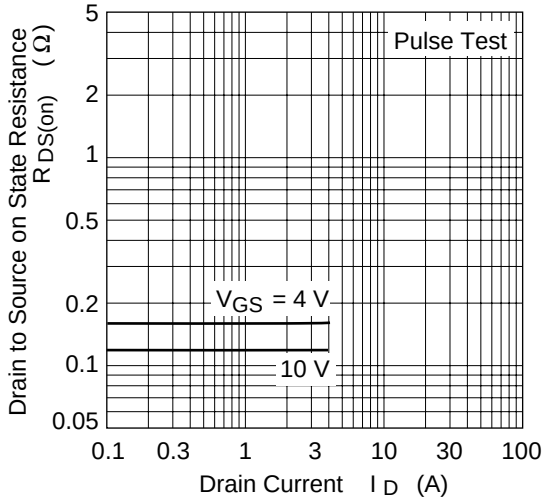

Typical Transfer Characteristics



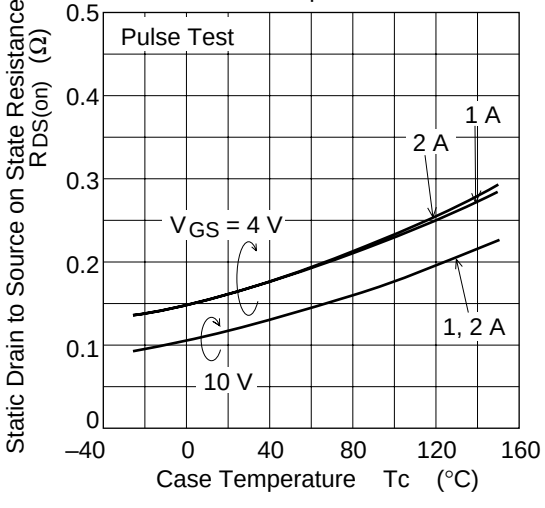
Drain to Source Saturation Voltage vs. Gate to Source Voltage



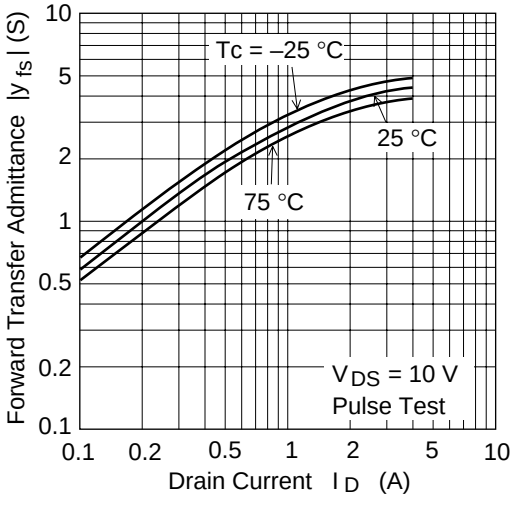

Static Drain to Source on State Resistance vs. Drain Current



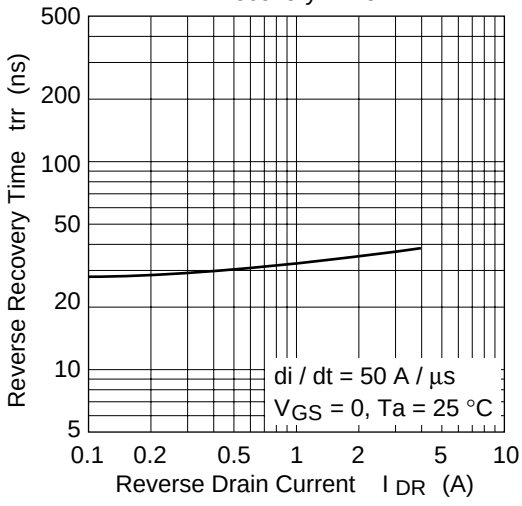

Static Drain to Source on State Resistance vs. Temperature



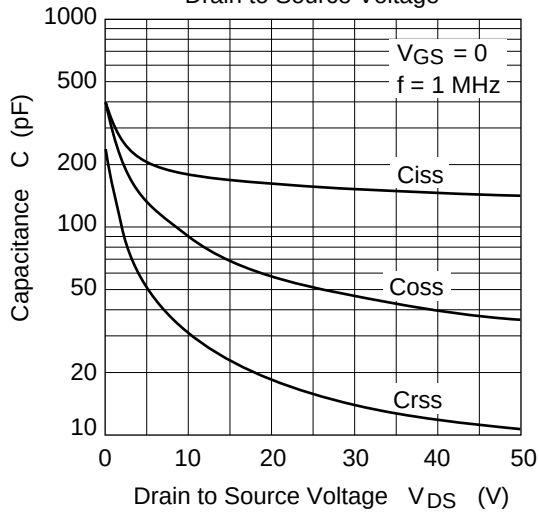

Forward Transfer Admittance vs. Drain Current



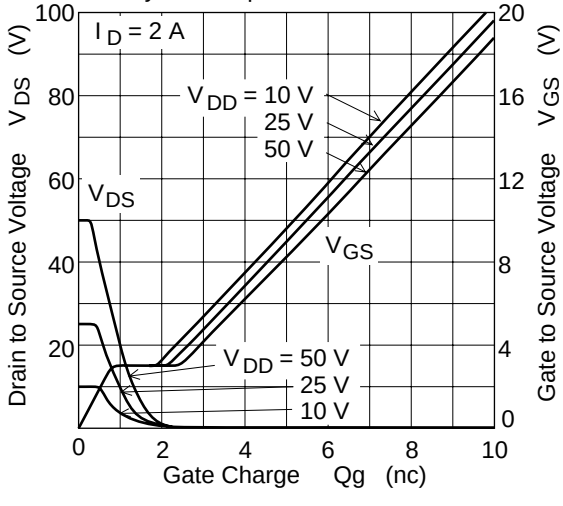
Body to Drain Diode Reverse Recovery Time



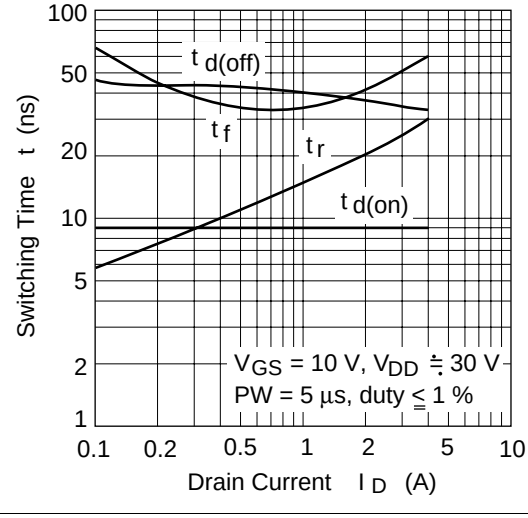

Typical Capacitance vs. Drain to Source Voltage



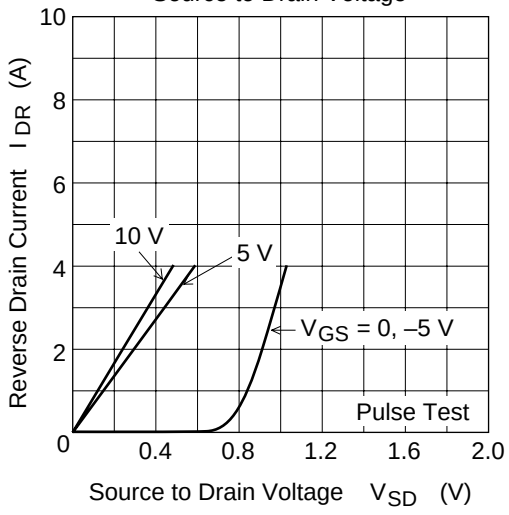

Dynamic Input Characteristics



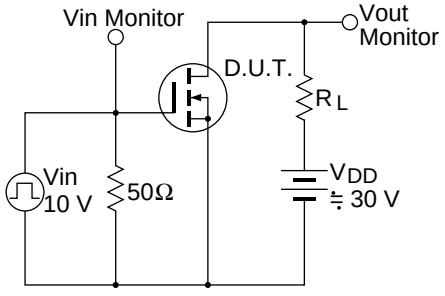

Switching Characteristics



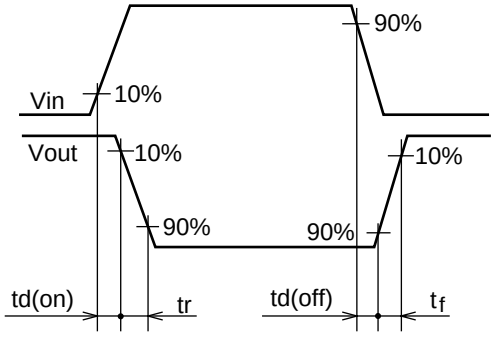
Reverse Drain Current vs.
Source to Drain Voltage




Switching Time Test Circuit

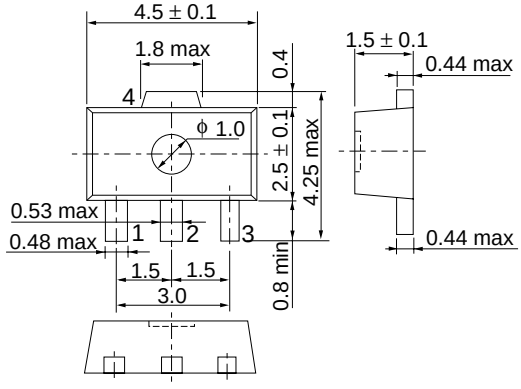


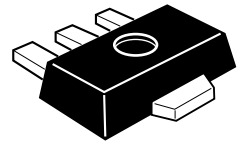

Waveform



## Package Dimensions

**Unit: mm**



| Hitachi Code | UPAK |
|---|---|
| EIAJ | SC–62 |
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