

# 16-Mbit (2048K x 8) Static RAM

## Features

- **Very high speed: 55 ns and 70 ns**
  - **Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
  - **Typical active current: 15 mA @ f = f<sub>max</sub>**
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{CE_1}$ ,  $\overline{CE_2}$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

## Functional Description<sup>[1]</sup>

The CY62168DV30 is a high-performance CMOS static RAMs organized as 2048Kbit words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by 90% when

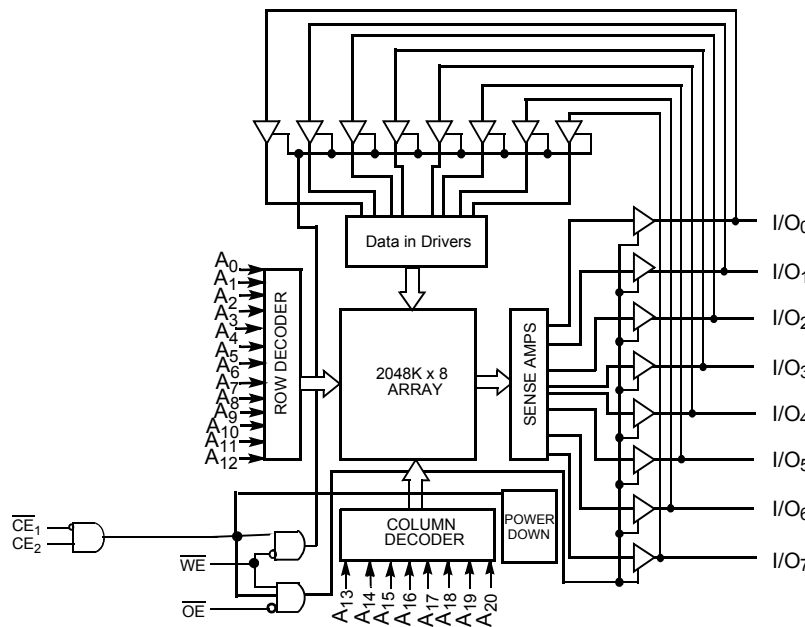
addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ( $\overline{CE_1}$ ) HIGH or Chip Enable 2 ( $\overline{CE_2}$ ) LOW. The input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when: deselected Chip Enable 1 ( $\overline{CE_1}$ ) HIGH or Chip Enable 2 ( $\overline{CE_2}$ ) LOW, outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation (Chip Enable 1 ( $\overline{CE_1}$ ) LOW and Chip Enable 2 ( $\overline{CE_2}$ ) HIGH and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable 1 ( $\overline{CE_1}$ ) LOW and Chip Enable 2 ( $\overline{CE_2}$ ) HIGH and Write Enable ( $\overline{WE}$ ) input LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>).

Reading from the device is accomplished by taking Chip Enable 1 ( $\overline{CE_1}$ ) and Output Enable ( $\overline{OE}$ ) LOW and Chip Enable 2 ( $\overline{CE_2}$ ) HIGH while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

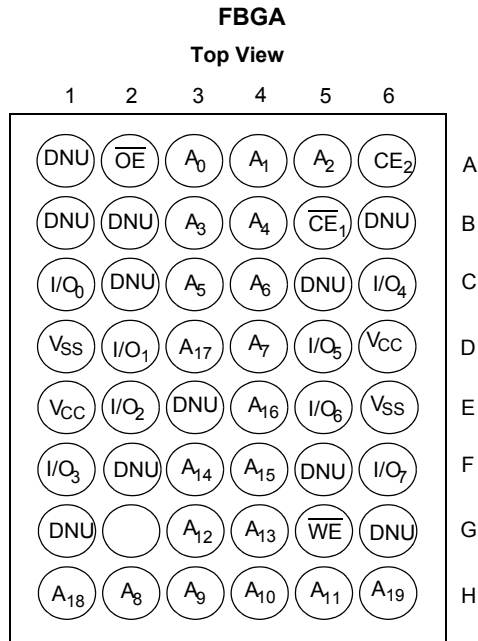
The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE_1}$  LOW and  $\overline{CE_2}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE_1}$  LOW and  $\overline{CE_2}$  HIGH and  $\overline{WE}$  LOW). See the truth table for a complete description of read and write modes.

## Logic Block Diagram



**Note:**

1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> ( $\mu$ A)	
	Min.	Typ. <sup>[3]</sup>	Max.		f = 1 MHz		f = f <sub>max</sub>			
					Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62168DV30L	2.2	3.0	3.6	55	2	4	15	30	2.5	30
				70			12	25		
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22
				70			12	25		

**Notes:**

2. DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC(max)}$  + 0.3V
- DC Voltage Applied to Outputs in High-Z State<sup>[4, 5]</sup>..... -0.3V to  $V_{CC(max)}$  + 0.3V

- DC Input Voltage<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC(max)}$  + 0.3V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> ) <sup>[6]</sup>	V <sub>CC</sub> <sup>[7]</sup>
Industrial	-40°C to +85°C	2.2V – 3.6V

**DC Electrical Characteristics (Over the Operating Range)**

Parameter	Description	Test Conditions	CY62168DV30-55			CY62168DV30-70			Unit	
			Min.	Typ. <sup>[3]</sup>	Max.	Min.	Typ. <sup>[3]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7   I <sub>OH</sub> = -0.1 mA	2.0			2.0			V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6   I <sub>OH</sub> = -1.0 mA	2.4			2.4				
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7   I <sub>OL</sub> = 0.1 mA			0.4			0.4	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6   I <sub>OH</sub> = 2.1 mA			0.4			0.4		
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3		
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	-0.3		0.6	-0.3		0.6	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	-0.3		0.8	-0.3		0.8		
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output disabled	-1		+1	-1		+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>   V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0mA, CMOS level		15	30		12	25	mA	
		f = 1 MHz		2	4		2	4		
I <sub>SB1</sub>	Automatic CE Power-down Current – CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, )	L		2.5	30		2.5	30	μA
			LL		2.5	22		2.5	22	
I <sub>SB2</sub>	Automatic CE Power-down Current – CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V	L		2.5	30		2.5	30	μA
			LL		2.5	22		2.5	22	

**Thermal Resistance**

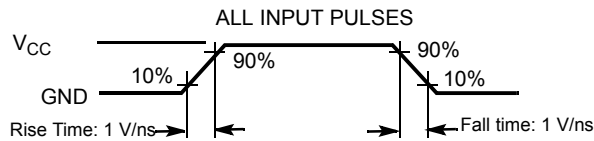
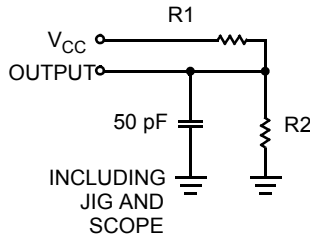
Parameter	Description	Test Conditions	BGA	Unit
Θ <sub>JA</sub>	Thermal Resistance <sup>[8]</sup> (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	55	°C/W
Θ <sub>JC</sub>	Thermal Resistance <sup>[8]</sup> (Junction to Case)		16	°C/W

**Notes:**

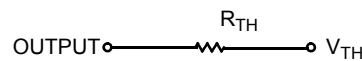
4. V<sub>IL(min)</sub> = -0.2V for pulse durations less than 20 ns.
5. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
6. T<sub>A</sub> is the "Instant-On" case temperature.
7. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 100 μs wait time after V<sub>CC</sub> stabilization..
8. Tested initially and after any design or process changes that may affect these parameters.

**Capacitance<sup>[8]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ.})}$	8	pF
$C_{OUT}$	Output Capacitance		10	pF

**AC Test Loads and Waveforms**


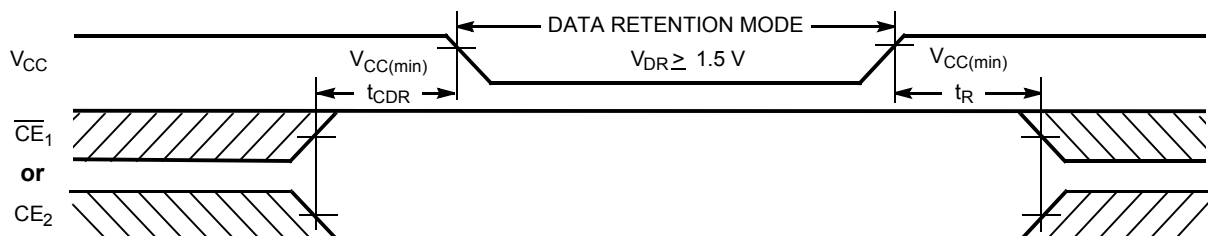
Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.50V	3.0V	Unit
R1	16600	1103	$\Omega$
R2	15400	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.2	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5		3.6	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5\text{V}$ $CE_1 \geq V_{CC} - 0.2\text{V}$ or $CE_2 \leq 0.2\text{V}$ $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	L		15	$\mu\text{A}$
			LL		10	$\mu\text{A}$
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Note:**

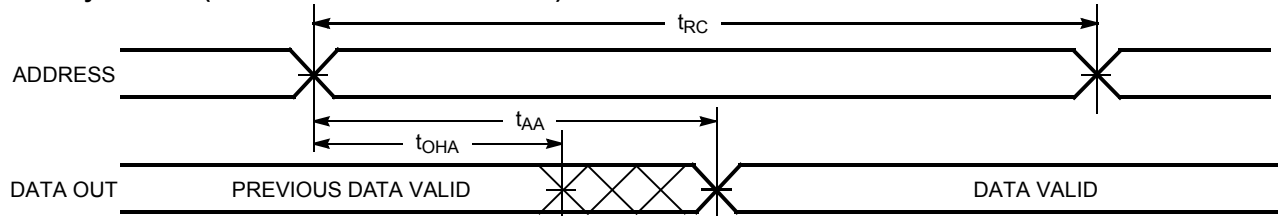
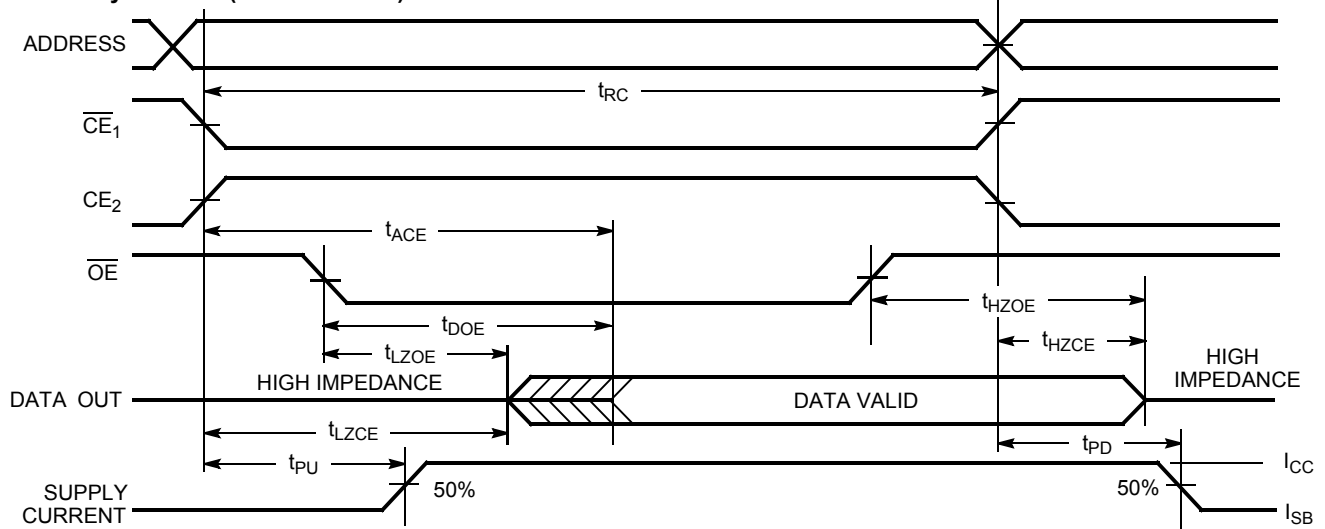
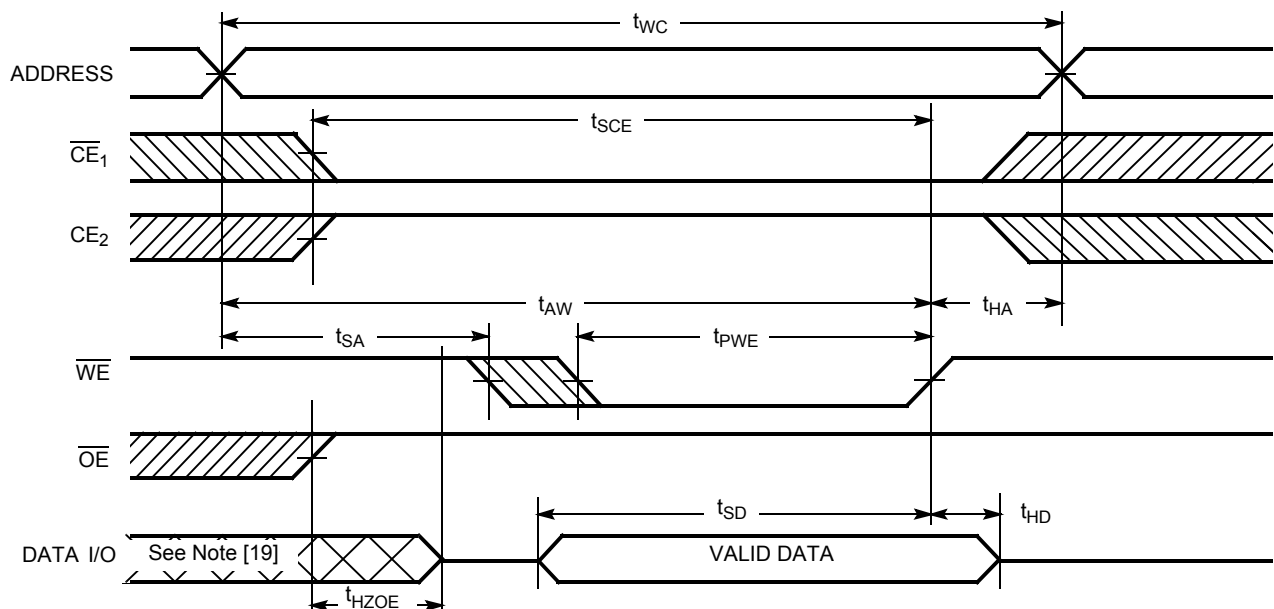
 9. Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} \geq 100\ \mu\text{s}$  or stable at  $V_{CC(\text{min.})} \geq 100\ \mu\text{s}$ .

**Switching Characteristics** Over the Operating Range <sup>[10]</sup>

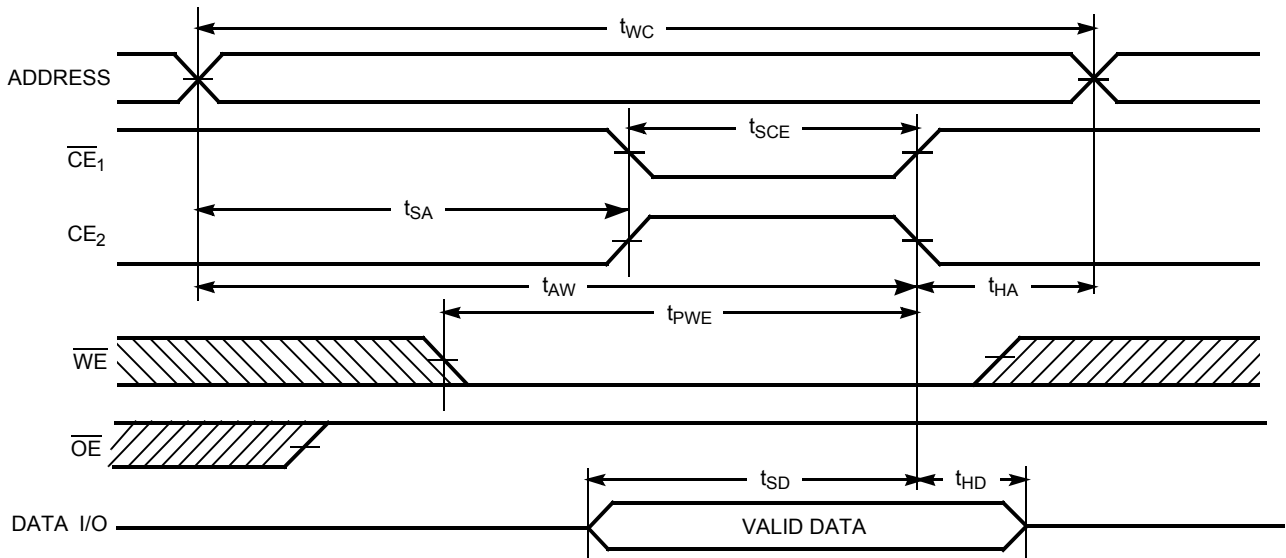
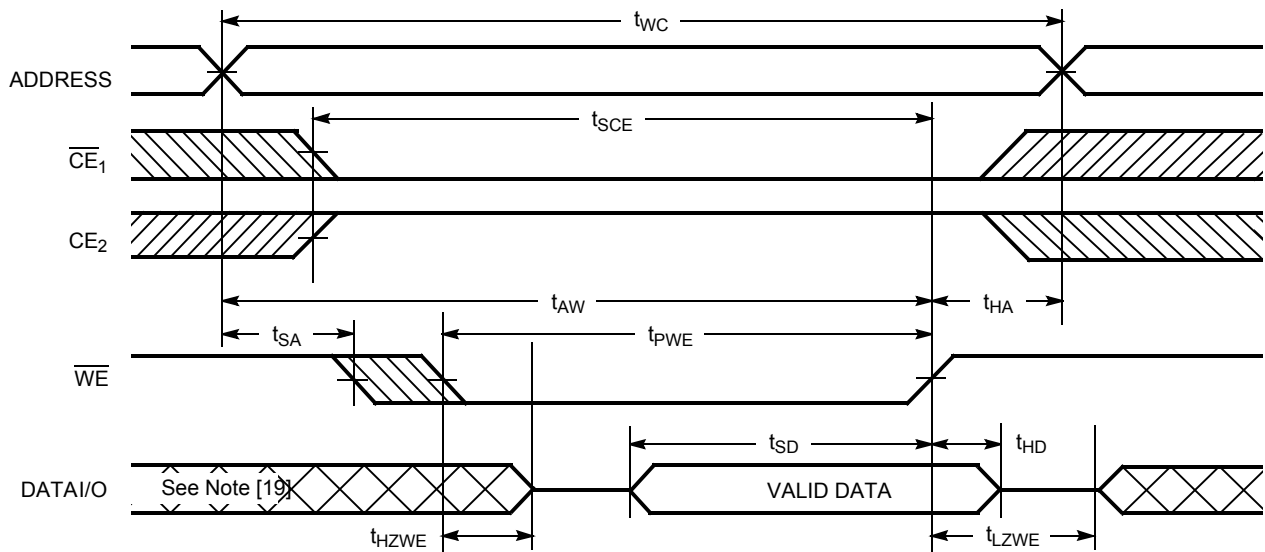
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Data Valid		55		70	ns
$t_{DOE}$	OE LOW to Data Valid		25		35	ns
$t_{LZOE}$	OE LOW to Low Z <sup>[11]</sup>	5		5		ns
$t_{HZOE}$	OE HIGH to High Z <sup>[11, 12]</sup>		20		25	ns
$t_{LZCE}$	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Low Z <sup>[11]</sup>	10		10		ns
$t_{HZCE}$	CE <sub>1</sub> HIGH or CE <sub>2</sub> LOW to High Z <sup>[11, 12]</sup>		20		25	ns
$t_{PU}$	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Power-Up	0		0		ns
$t_{PD}$	CE <sub>1</sub> HIGH or CE <sub>2</sub> LOW to Power-Down		55		70	ns
<b>Write Cycle<sup>[13]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Write End	40		60		ns
$t_{AW}$	Address Set-Up to Write End	40		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	WE Pulse Width	40		45		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	WE LOW to High Z <sup>[11, 12]</sup>		20		25	ns
$t_{LZWE}$	WE HIGH to Low Z <sup>[11]</sup>	10		10		ns

**Notes:**

10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)**<sup>[14, 15]</sup>

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[15, 16]</sup>

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)**<sup>[13, 17, 18]</sup>

**Notes:**

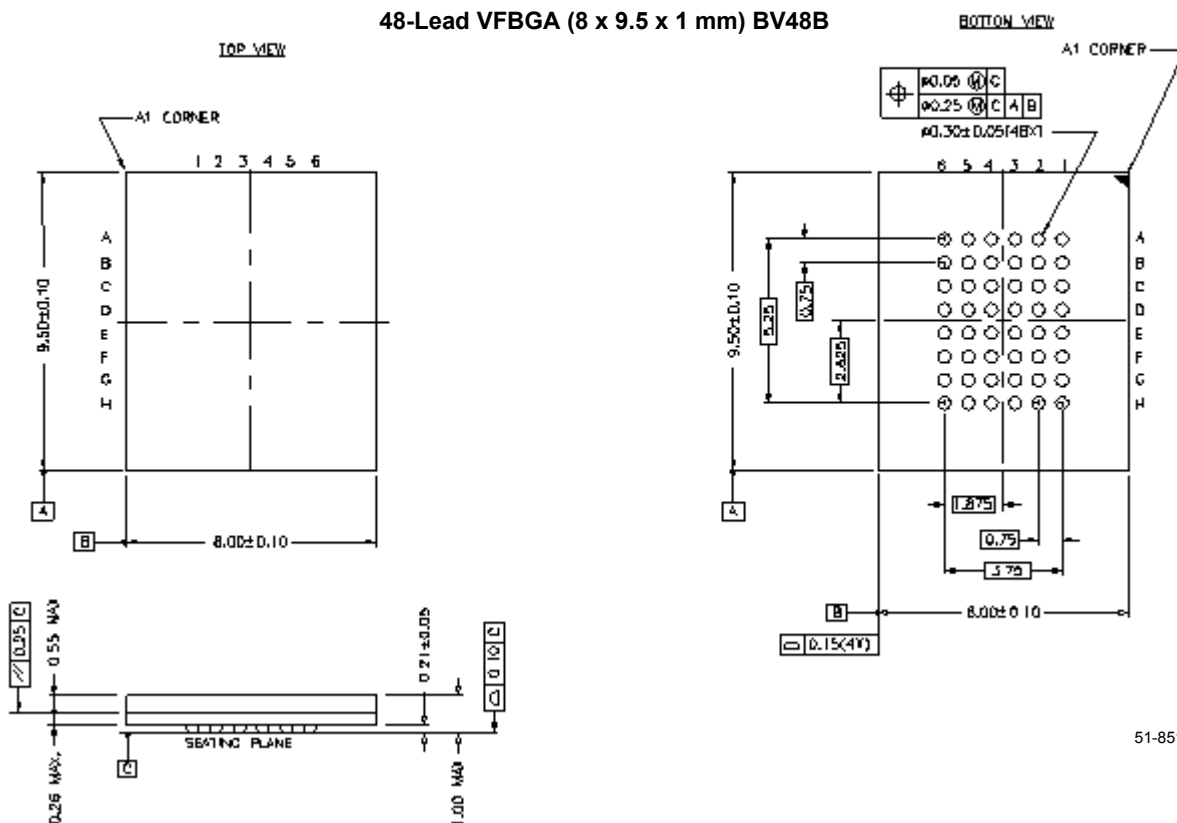
14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
15.  $\overline{WE}$  is HIGH for read cycle.
16. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
18. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** <sup>[13, 17, 18]</sup>

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** <sup>[19]</sup>

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> )	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	Data in (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62168DV30L-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	
70	CY62168DV30L-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	
55	CY62168DV30L-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	
70	CY62168DV30L-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	

**Package Diagrams**


51-85178-\*\*

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**Document History Page**

<b>Document Title: CY62168DV30 MoBL<sup>®</sup> 16-Mbit (2048K x 8) Static RAM</b>				
<b>Document Number: 38-05329</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	118409	09/30/02	GUG	New Data Sheet
*A	123693	02/05/03	DPM	Changed Advance Information to Preliminary Added package diagram
*B	126556	04/24/03	DPM	Minor change: Change sunset owner from DPM to HRT
*C	132869	01/15/04	XRJ	Changed Preliminary to Final
*D	272589	See ECN	PCI	Updated Final data sheet and added Pb-free package.