GALVANTECH, INC.

GVT71256ZC36/GVT71512ZC18
256K X 36/512K X 18 ZBL SRAM

SYNCHRONOUS ZBL SRAM PIPELINED OUTPUT

256K x 36 SRAM 512K x 18 SRAM

+3.3V SUPPLY, +3.3V or +2.5V I/O

FEATURES

- Zero Bus Latency, no dead cycles between write and read cycles
- Fast clock speed: 200, 166, 133, and 100MHz
- Fast access time: 3.2, 3.6, 4.2, 5.0ns
- Internally synchronized registered outputs eliminate the need to control OE#
- Single 3.3V -5% and +5% power supply VCC
- Separate VCCQ for 3.3V or 2.5V I/O
- Single R/W# (READ/WRITE) control pin
- Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications
- Interleaved or linear 4-word burst capability
- Individual byte write (BWa# - BWd#) control (may be tied LOW)
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- SNOOZE MODE for low power standby
- JTAG boundary scan
- Low profile 119 bump, 14mm x 22mm PBGA (Ball Grid Array) and 100 pin TQFP packages

OPTIONS MARKING

- Timing

5.0ns cycle/3.2ns access	-5
6.0ns cycle/3.6ns access	-6
7.5ns cycle/4.2ns access	-7.5
10ns cycle/5.0ns access	-10

- Package Versions

119-bump PBGA	B
100-pin TQFP	T

GENERAL DESCRIPTION

The GVT71256ZC36 and GVT71512ZC18 SRAMs are designed to eliminate dead cycles when transitions from READ to WRITE or vice versa. These SRAMs are optimized for 100 percent bus utilization and achieves Zero Bus Latency (ZBL). They integrate 262,144x36 and 524,288x18 SRAM cells, respectively, with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion chip enables (CE#, CE2# and CE2), cycle start input (ADV/LD#), clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#), and read-write control (R/W#). BWc# and BWd# apply to GVT71256ZC36 only.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later, its associated data occurs, either read or write.

A clock enable (CKE#) pin allows operation of the GVT71256ZC36/GVT71512ZC18 to be suspended as long as necessary. All synchronous inputs are ignored when (CKE#) is high and the internal device registers will hold their previous values.

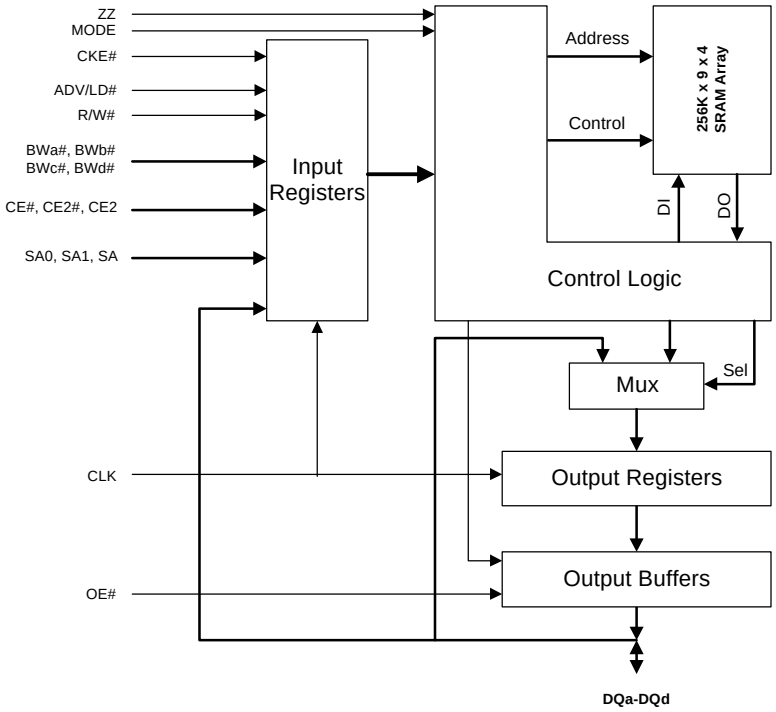
There are three chip enable pins (CE#, CE2, CE2#) that allow the user to deselect the device when desired. If any one of these three are not active when ADV/LD# is low, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (read or write) will be completed. The data bus will be in high impedance state two cycles after chip is deselected or a write cycle is initiated.

The GVT71256ZC36 and GVT71512ZC18 have an on-chip 2-bit burst counter. In the burst mode, the GVT71256ZC36 and GVT71512ZC18 provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/LD# signal is used to load a new external address (ADV/LD#=LOW) or increment the internal burst counter (ADV/LD#=HIGH)

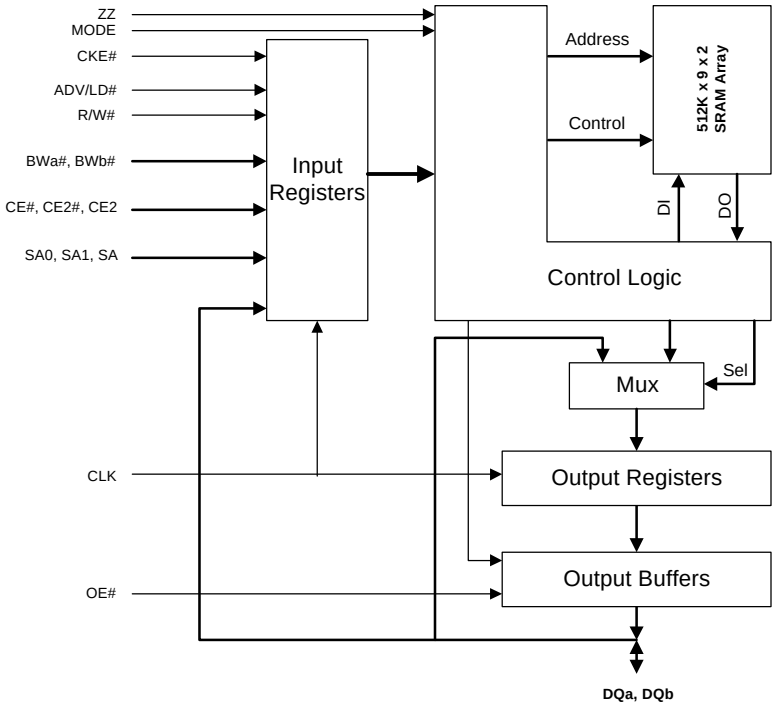
Output enable (OE#), snooze enable (ZZ) and burst sequence select (MODE) are the asynchronous signals. OE# can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

Four pins are used to implement JTAG test capabilities. The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

256K X 36 FUNCTIONAL BLOCK DIAGRAM



512K X 18 FUNCTIONAL BLOCK DIAGRAM



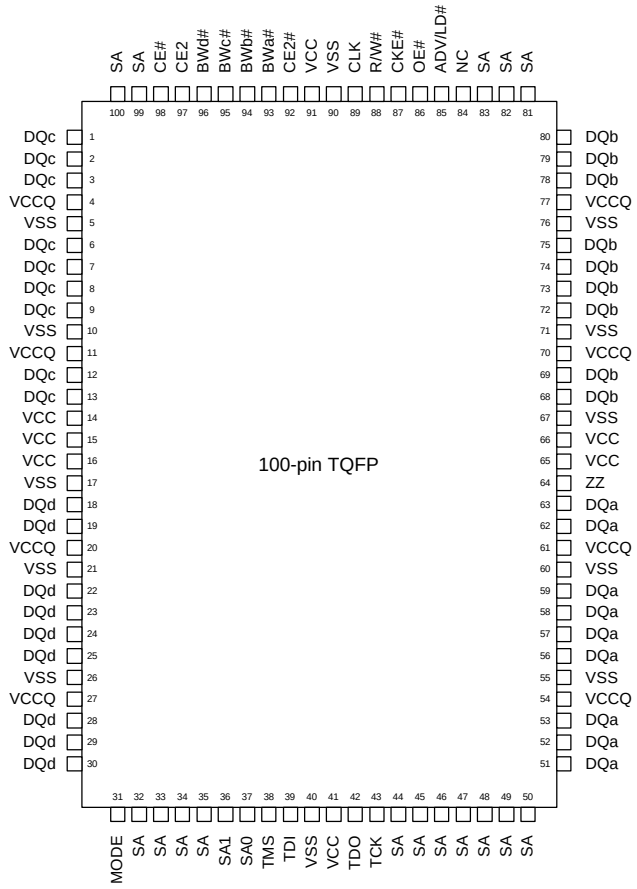
NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

256Kx36, 119-Bump PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	SA	SA	NC	SA	SA	VCCQ
B	NC	CE2	SA	ADV/LD#	SA	CE2#	NC
C	NC	SA	SA	VCC	SA	SA	NC
D	DQc	DQc	VSS	NC	VSS	DQb	DQb
E	DQc	DQc	VSS	CE#	VSS	DQb	DQb
F	VCCQ	DQc	VSS	OE#	VSS	DQb	VCCQ
G	DQc	DQc	BWc#	SA	BWb#	DQb	DQb
H	DQc	DQc	VSS	R/W#	VSS	DQb	DQb
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	BWd#	NC	BWa#	DQa	DQa
M	VCCQ	DQd	VSS	CKE#	VSS	DQa	VCCQ
N	DQd	DQd	VSS	SA1	VSS	DQa	DQa
P	DQd	DQd	VSS	SA0	VSS	DQa	DQa
R	NC	SA	MODE	VCC	VCC	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VCCQ	TMS	TDI	TCK	TDO	NC	VCCQ

TOP VIEW 119 LEAD BGA

256Kx36, 100-PIN TQFP (Top View)



PIN DESCRIPTIONS

256Kx36 TQFP PINS	256Kx36 PBGA PINS	SYMBOL	TYPE	DESCRIPTION
37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 83, 99, 100	4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 3T, 4T, 5T	SA0, SA1, SA	Input-Synchronous	Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/LD# LOW, CKE# LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated.
93, 94, 95, 96	5L 5G 3G 3L	BWa#, BWb#, BWc#, BWd#	Input-Synchronous	Synchronous Byte Write Enables: Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/W# and ADV/LD# are sampled LOW), the appropriate byte write signal (BWx#) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/W# is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins. BWx# can all be tied LOW if always doing write to the entire 36-bit word.
87	4M	CKE#	Input-Synchronous	Synchronous Clock Enable Input: When CKE# is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CKE# sampled HIGH on the device outputs is as if the low to high clock transition did not occur. For normal operation, CKE# must be sampled LOW at rising edge of clock.
88	4H	R/W#	Input-Synchronous	Read Write: R/W# signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by ADV/LD# is a Read or Write operation. The data bus activity for the current cycle takes place two clock cycles later.

PIN DESCRIPTIONS (continued)

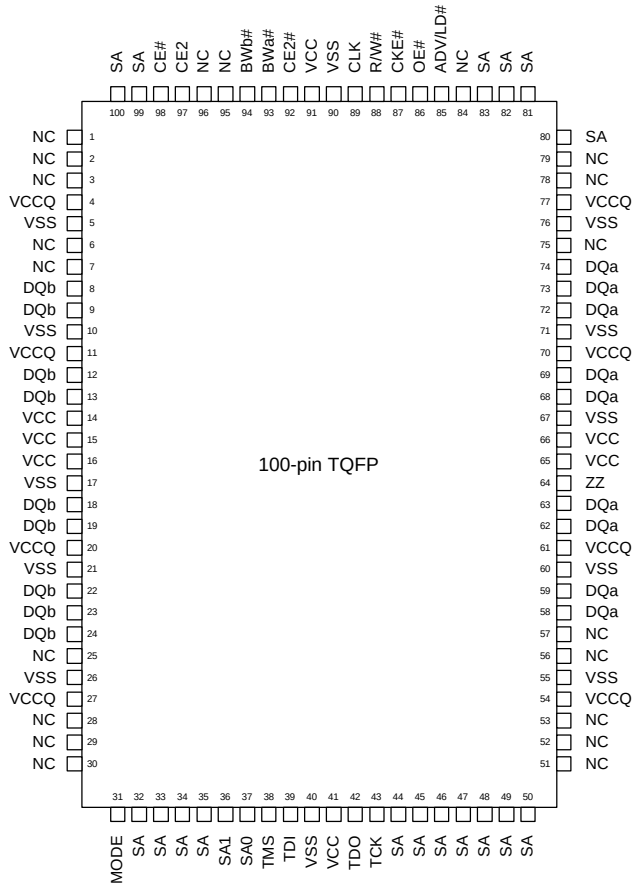
256Kx36 TQFP PINS	256Kx36 PBGA PINS	SYMBOL	TYPE	DESCRIPTION
89	4K	CLK	Input-Synchronous	Clock: This is the clock input to GVT71256ZC36. Except for OE#, ZZ and MODE, all timing references for the device are made with respect to the rising edge of CLK.
98, 92	4E, 6B	CE#, CE2#	Input-Synchronous	Synchronous Active Low Chip Enable: CE# and CE2# are used with CE2 to enable the GVT71256ZC36. CE# or CE2# sampled HIGH or CE2 sampled LOW, along with ADV/LD# LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be HIGH-Z two clock cycles after chip deselect is initiated.
97	2B	CE2	input-Synchronous	Synchronous Active High Chip enable: CE2 is used with CE# and CE2# to enable the chip. CE2 has inverted polarity but otherwise is identical to CE# and CE2#.
86	4F	OE#	Input	Asynchronous Output Enable: OE# must be LOW to read data. When OE# is HIGH, the I/O pins are in high impedance state. OE# does not need to be actively controlled for read and write cycles. In normal operation, OE# can be tied LOW.
85	4B	ADV/LD#	Input-Synchronous	Advance/Load: ADV/LD# is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When ADV/LD# is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and R/W# are ignored when ADV/LD# is sampled HIGH.
31	3R	MODE	Input-Static	Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input.
64	7T	ZZ	Input-Asynchronous	Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC.
51, 52, 53, 56-59, 62, 63 68, 69, 72-75, 78, 79, 80 1, 2, 3, 6-9, 12, 13 18, 19, 22-25, 28, 29, 30	(a) 6P, 7P, 7N, 6N, 6M, 6L, 7L, 6K, 7K, (b) 7H, 6H, 7G, 6G, 6F, 6E, 7E, 7D, 6D, (c) 2D, 1D, 1E, 2E, 2F, 1G, 2G, 1H, 2H, (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQa DQb DQc DQd	Input/Output	Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins.
38 39 43	2U 3U 4U	TMS TDI TCK	Input	IEEE 1149.1 test inputs. LVTTL-level inputs. If SERIAL BOUNDARY SCAN (JTAG) is not used, these pins can be floating (i.e. No Connect) or be connected to VCC.
42	5U	TDO	Output	IEEE 1149.1 test output. LVTTL-level output. If SERIAL BOUNDARY SCAN (JTAG) is not used, these pins can be floating (i.e. No Connect).
14, 15, 16, 41, 65, 66, 91	4C, 2J, 4J, 6J, 4R, 5R	VCC	Supply	Power Supply: +3.3V -5% and +5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	VSS	Ground	Ground: GND.
4, 11, 20, 27, 54, 61, 70, 77	1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	VCCQ	I/O Supply	Output Buffer Supply: +3.3V -0.165V and +0.165V for 3.3V I/O. +2.5V -0.125V and +0.4V for 2.5V I/O.
84	4A, 1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 7R, 1T, 2T, 6T, 6U	NC	-	No Connect: These signals are not internally connected. It can be left floating or be connected to VCC or to GND.

512Kx18, 119-Bump PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	SA	SA	NC	SA	SA	VCCQ
B	NC	CE2	SA	ADV/LD#	SA	CE2#	NC
C	NC	SA	SA	VCC	SA	SA	NC
D	DQb	NC	VSS	NC	VSS	DQa	NC
E	NC	DQb	VSS	CE#	VSS	NC	DQa
F	VCCQ	NC	VSS	OE#	VSS	DQa	VCCQ
G	NC	DQb	BWb#	SA	VSS	NC	DQa
H	DQb	NC	VSS	R/W#	VSS	DQa	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	BWa#	DQa	NC
M	VCCQ	DQb	VSS	CKE#	VSS	NC	VCCQ
N	DQb	NC	VSS	SA1	VSS	DQa	NC
P	NC	DQb	VSS	SA0	VSS	NC	DQa
R	NC	SA	MODE	VCC	VCC	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VCCQ	TMS	TDI	TCK	TDO	NC	VCCQ

TOP VIEW 119 LEAD BGA

512Kx18, 100-PIN TQFP (Top View)



PIN DESCRIPTIONS

512Kx18 TQFP PINS	512Kx18 PBGA PINS	SYMBOL	TYPE	DESCRIPTION
37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 83, 99, 100	4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 6B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 2T, 3T, 5T, 6T	SA0, SA1, SA	Input-Synchronous	Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/LD# LOW, CKE# LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated.
93, 94,	5L 3G	BWa#, BWb#	Input-Synchronous	Synchronous Byte Write Enables: Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/W# and ADV/LD# are sampled LOW), the appropriate byte write signal (BWx#) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/W# is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BWa# controls DQa pins; BWb# controls DQb pins. BWx# can all be tied LOW if always doing write to the entire 18-bit word.
87	4M	CKE#	Input-Synchronous	Synchronous Clock Enable Input: When CKE# is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CKE# sampled HIGH on the device outputs is as if the low to high clock transition did not occur. For normal operation, CKE# must be sampled LOW at rising edge of clock.
88	4H	R/W#	Input-Synchronous	Read Write: R/W# signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by ADV/LD# is a Read or Write operation. The data bus activity for the current cycle takes place two clock cycles later.

PIN DESCRIPTIONS (continued)

512Kx18 TQFP PINS	512Kx18 PBGA PINS	SYMBOL	TYPE	DESCRIPTION
89	4K	CLK	Input-Synchronous	Clock: This is the clock input to GVT71512ZC18. Except for OE#, ZZ and MODE, all timing references for the device are made with respect to the rising edge of CLK.
98, 92	4E, 6B	CE#, CE2#	Input-Synchronous	Synchronous Active Low Chip Enable: CE# and CE2# are used with CE2 to enable the GVT71512ZC18. CE# or CE2# sampled HIGH or CE2 sampled LOW, along with ADV/LD# LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be HIGH-Z two clock cycles after chip deselect is initiated.
97	2B	CE2	input-Synchronous	Synchronous Active High Chip enable: CE2 is used with CE# and CE2# to enable the chip. CE2 has inverted polarity but otherwise is identical to CE# and CE2#.
86	4F	OE#	Input	Asynchronous Output Enable: OE# must be LOW to read data. When OE# is HIGH, the I/O pins are in high impedance state. OE# does not need to be actively controlled for read and write cycles. In normal operation, OE# can be tied LOW.
85	4B	ADV/LD#	Input-Synchronous	Advance/Load: ADV/LD# is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When ADV/LD# is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and R/W# are ignored when ADV/LD# is sampled HIGH.
31	3R	MODE	Input-Static	Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input.
64	7T	ZZ	Input-Asynchronous	Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC.
58, 59, 62, 63, 68, 69, 72, 73, 74 8, 9, 12, 13, 18, 19, 22, 23, 24	(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQa DQb	Input/Output	Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte "a" is DQa pins; Byte "b" is DQb pins.
38 39 43	2U 3U 4U	TMS TDI TCK	Input	IEEE 1149.1 test inputs. LVTTL-level inputs. If SERIAL BOUNDARY SCAN (JTAG) is not used, these pins can be floating (i.e. No Connect) or be connected to VCC.
42	5U	TDO	Output	IEEE 1149.1 test output. LVTTL-level output. If SERIAL BOUNDARY SCAN (JTAG) is not used, these pins can be floating (i.e. No Connect).
14, 15, 16, 41, 65, 66, 91	4C, 2J, 4J, 6J, 4R, 5R	VCC	Supply	Power Supply: +3.3V -5% and +5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	VSS	Ground	Ground: GND.
4, 11, 20, 27, 54, 61, 70, 77	1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	VCCQ	I/O Supply	Output Buffer Supply: +3.3V -0.165V and +0.165V for 3.3V I/O. +2.5V -0.125V and +0.4V for 2.5V I/O.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 84, 95, 96	4A, 1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U	NC	-	No Connect: These signals are not internally connected. It can be left floating or be connected to VCC or to GND.

PARTIAL TRUTH TABLE FOR READ/WRITE[1]

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
Read	H	X	X	X	X
No Write	L	H	H	H	H
Write Byte a (DQa)[2]	L	L	H	H	H
Write Byte b (DQb)[2]	L	H	L	H	H
Write Byte c (DQc)[2]	L	H	H	L	H
Write Byte d (DQd}[2]	L	H	H	H	L
Write all bytes	L	L	L	L	L

Note:1

1. L means logic LOW. H means logic HIGH. X means "Don't Care."
2. Multiple bytes may be selected during the same cycle.
3. BWc# and BWd# apply to 256Kx36 device only.

INTERLEAVED BURST ADDRESS TABLE (MODE = VCC or NC)

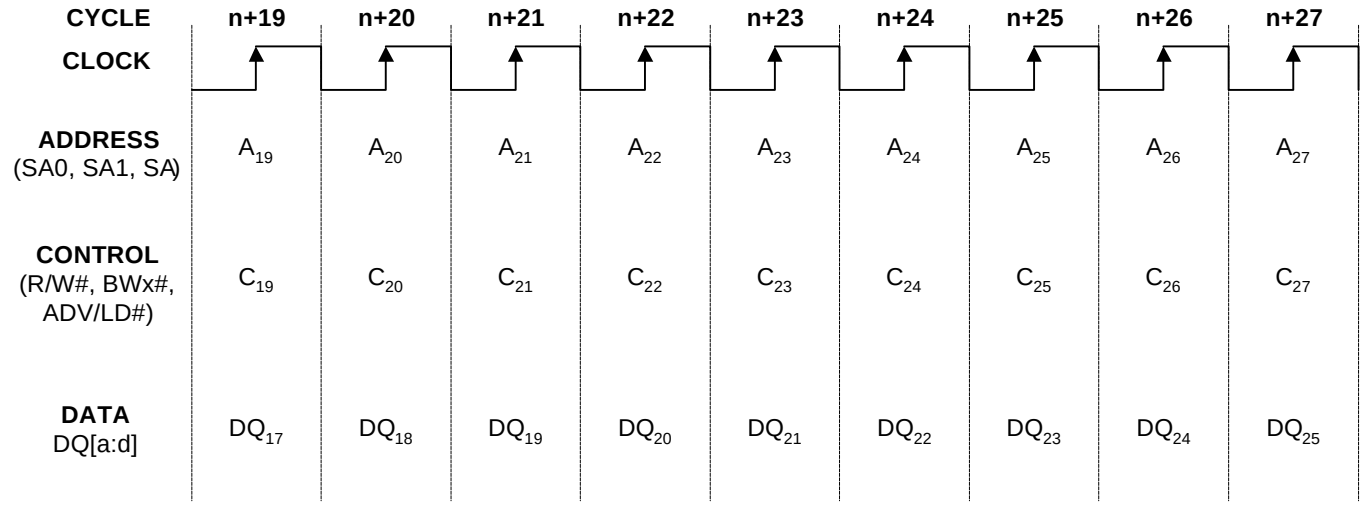
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[1]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{00}	A...A_{11}	A...A_{10}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{10}	A...A_{01}	A...A_{00}

LINEAR BURST ADDRESS TABLE (MODE = VSS)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[1]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{10}	A...A_{11}	A...A_{00}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{00}	A...A_{01}	A...A_{10}

Note:
1. Upon completion of the Burst sequence, the counter wraps around to its initial state and continues counting.

FUNCTIONAL TIMING DIAGRAM



Note:
1. This assumes that CKE#, CE#, CE2 and CE2# are all True.
2. All addresses, control and data-in are only required to meet set-up and hold time with respect to the rising edge of clock. Data out is valid after a clock-to-data delay from the rising edge of clock.
3. DQc and DQd apply to 256Kx36 device only.

TRUTH TABLE(1-9)

OPERATION	PREVIOUS CYCLE	ADDRESS USED	R/W#	ADV/LD#	CE#	CKE#	BWx#	OE#	DQ (2 cycles later)	NOTES
DESELECT CYCLE	X	X	X	L	H	L	X	X	High-Z	
CONTINUE DESELECT/NOP	DESELECT	X	X	H	X	L	X	X	High-Z	10
READ CYCLE (BEGIN BURST)	X	External	H	L	L	L	X	X	Q	
READ CYCLE (CONTINUE BURST)	READ	Next	X	H	X	L	X	X	Q	10
DUMMY READ (BEGIN BURST)	X	External	H	L	L	L	X	H	High-Z	11
DUMMY READ (CONTINUE BURST)	READ	Next	X	H	X	L	X	H	High-Z	10, 11
WRITE CYCLE (BEGIN BURST)	X	External	L	L	L	L	L	X	D	
WRITE CYCLE (CONTINUE BURST)	WRITE	Next	X	H	X	L	L	X	D	10
ABORT WRITE (BEGIN BURST)	X	External	L	L	L	L	H	X	High-Z	11
ABORT WRITE (CONTINUE BURST)	WRITE	Next	X	H	X	L	H	X	High-Z	10, 11
IGNORE CLOCK EDGE /NOP	X	X	X	H	X	H	X	X	-	12

Note:

1. L means logic LOW. H means logic HIGH. X means "Don't Care." High-Z means HIGH IMPEDANCE. BWx# = L means [BWa#*BWb#*BWc#*BWd#] equals LOW. BWx# = H means [BWa#*BWb#*BWc#*BWd#] equals HIGHBWc# and BWd# apply to 256Kx36 device only.
2. CE# equals H means CE# and CE2# are LOW along with CE2 being HIGH. CE# equals L means CE# or CE2# is HIGH or CE2 is LOW. CE# equals X means CE#, CE2# and CE2 are "Don't Care."
3. BWa# enables WRITE to byte "a" (DQa pins). BWb# enables WRITE to byte "b" (DQb pins). BWc# enables WRITE to byte "c" (DQc pins). BWd# enables WRITE to byte "d" (DQd pins). DQc, DQd, BWc# and BWd# apply to 256Kx36 device only.
4. The device is not in SNOOZE MODE, i.e. the ZZ pin is LOW.
5. During SNOOZE MODE, the ZZ pin is HIGH and all the address pins and control pins are "Don't Care." The SNOOZE MODE can only be entered two cycles after the WRITE cycle, otherwise the WRITE cycle may not be completed
6. All inputs, except OE#, ZZ and MODE pins, must meet setup time and hold time specification against the clock (CLK) LOW-to-HIGH transition edge.
7. OE# may be tied to LOW for all the operation. This device automatically turns off the output driver during WRITE cycle.
8. Device outputs are ensured to be in High-Z during device power-up
9. This device contains a 2-bit burst counter. The address counter is incremented for all CONTINUE BURST cycles. Address wraps to the initial address every fourth burst cycle.
10. CONTINUE BURST cycles, whether READ or WRITE, use the same control signals. The type of cycle performed, READ or WRITE, depends upon the R/W# control signal at the BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
11. DUMMY READ and ABORT WRITE cycles can be entered to setup subsequent READ or WRITE cycles or to increment the burst counter.
12. When an IGNORE CLOCK EDGE cycle enters, the output data (Q) will remain the same if the previous cycle is READ cycle or remain High-Z if the previous cycle is WRITE or DESELECT cycle.

ABSOLUTE MAXIMUM RATINGS *

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +125°
Junction Temperature .....+125°
Power Dissipation 2.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCC+0.3	V	1,2
	All Other Inputs	V_{IH}	2.0	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-	5	uA	
MODE and ZZ Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-	30	uA	6
Output Leakage Current	Output(s) disabled, 0 V ≤ V_{OUT} ≤ VCC	IL_O	-	5	uA	
Output High Voltage	I_{OH} = -5.0mA for 3.3V I/O	V_{OH}	2.4		V	1
	I_{OH} = -1.0mA for 2.5V I/O		2.0		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	3.135	3.465	V	1
I/O Supply Voltage	3.3V I/O	VCCQ	3.135	3.465	V	1
	2.5V I/O		2.4	2.9	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-5	-6	-7.5	-10	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; VCC =MAX; outputs open, ADV/LD# = X, f = f_{MAX} [2]	Icc	200	560	480	410	350	mA	3, 4, 5, 7
CMOS Standby	Device deselected; VCC = MAX ; all inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	15	30	30	30	30	mA	4, 5, 7
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	20	50	50	50	50	mA	4, 5, 7
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB4}	50	230	200	190	170	mA	4, 5, 7

Note:

1. All voltages referenced to VSS (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2
   Undershoot: V_{IL} ≤ -2.0V for t ≤ ^tKC /2.
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. "Device Deselected" means the device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means the device is active.
5. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
6. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±50 µA.
7. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f = 0 means no input lines are changing.

AC ELECTRICAL CHARACTERISTICS

(Note 2) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +5%)

DESCRIPTION		-5 200MHz		-6 166MHz		-7.5 133MHz		-10 100MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	5.0		6.0		7.5		10		ns	
Clock HIGH time	^tKH	1.8		2.1		2.6		3.5		ns	
Clock LOW time	^tKL	1.8		2.1		2.6		3.5		ns	
Output Times											
Clock to output valid	^tKQ		3.2		3.6		4.2		5.0	ns	
Clock to output invalid	^tKQX	1.0		1.0		1.0		1.0		ns	
Clock to output in Low-Z	^tKQLZ	1.0		1.0		1.0		1.0		ns	1, 3, 4
Clock to output in High-Z	^tKQHZ	1.0	3.0	1.0	3.0	1.0	3.0	1.0	3.0	ns	1, 3, 4
OE to output valid	^tOEQ		3.2		3.6		4.2		5.0	ns	
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	1, 3, 4
OE to output in High-Z	^tOEHZ		3.5		3.5		3.5		3.5	ns	1, 3, 4
Setup Times											
Address and Controls	^tS	1.5		1.5		1.8		2.0		ns	5
Data In	^tSD	1.5		1.5		1.8		2.0		ns	5
Hold Times											
Address and Controls	^tH	0.5		0.5		0.5		0.5		ns	5
Data In	^tHD	0.5		0.5		0.5		0.5		ns	5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	4	4	pF	1
Input/Output Capacitance (DQ)		C_O	7	6.5	pF	1

THERMAL CONSIDERATION

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	25	$^oC/W$	
Thermal Resistance - Junction to Case		Θ_{JC}	9	$^oC/W$	

Note:

8. This parameter is sampled.
9. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
10. Output loading is specified with CL=5pF as in Fig. 2.
11. At any given temperature and voltage condition, ^tKQHZ is less than ^tKQLZ and ^tOEHZ is less than ^tOELZ.
12. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

AC TEST CONDITIONS FOR 3.3V I/O

Input pulse levels	0V to 3.0V
Input rise and fall times	1ns
Output rise and fall times(max)	1.8ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1

OUTPUT LOADS FOR 3.3V I/O

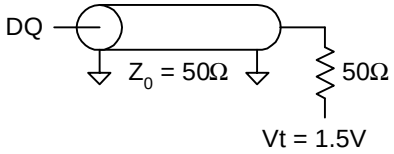


Fig. 1 OUTPUT LOAD EQUIVALENT

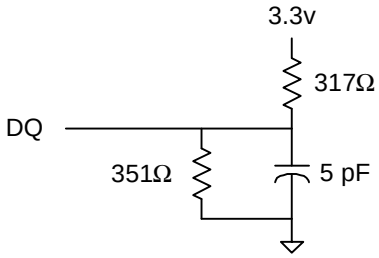


Fig. 2 OUTPUT LOAD EQUIVALENT

AC TEST CONDITIONS FOR 2.5V I/O

Input pulse levels	0V to 2.5V
Input rise and fall times	1ns
Output rise and fall times(max)	1.8ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 1A

OUTPUT LOADS FOR 2.5V I/O

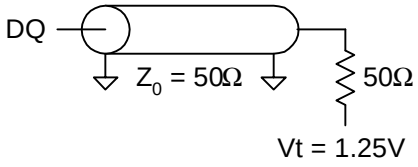
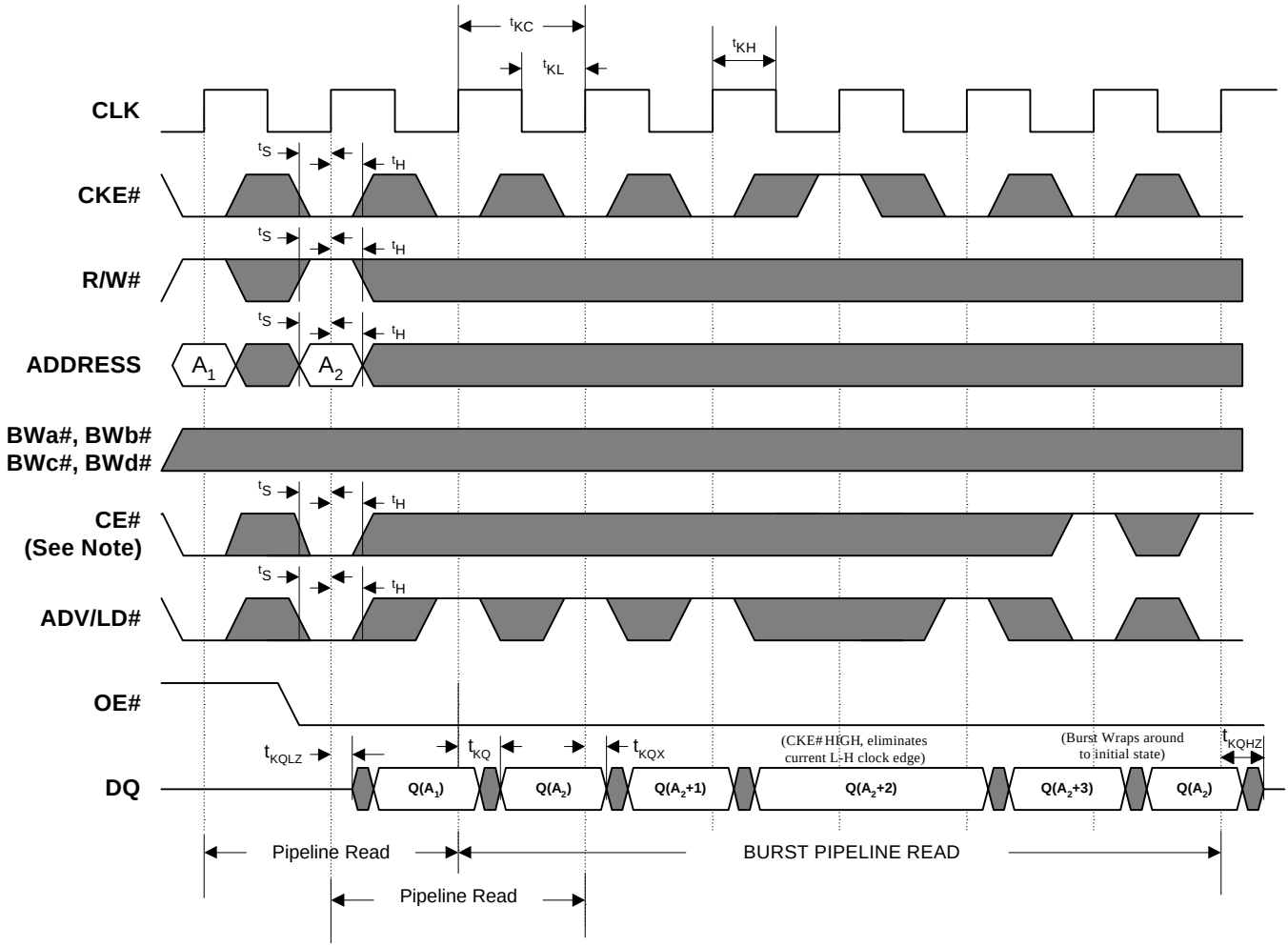


Fig. 1A OUTPUT LOAD EQUIVALENT

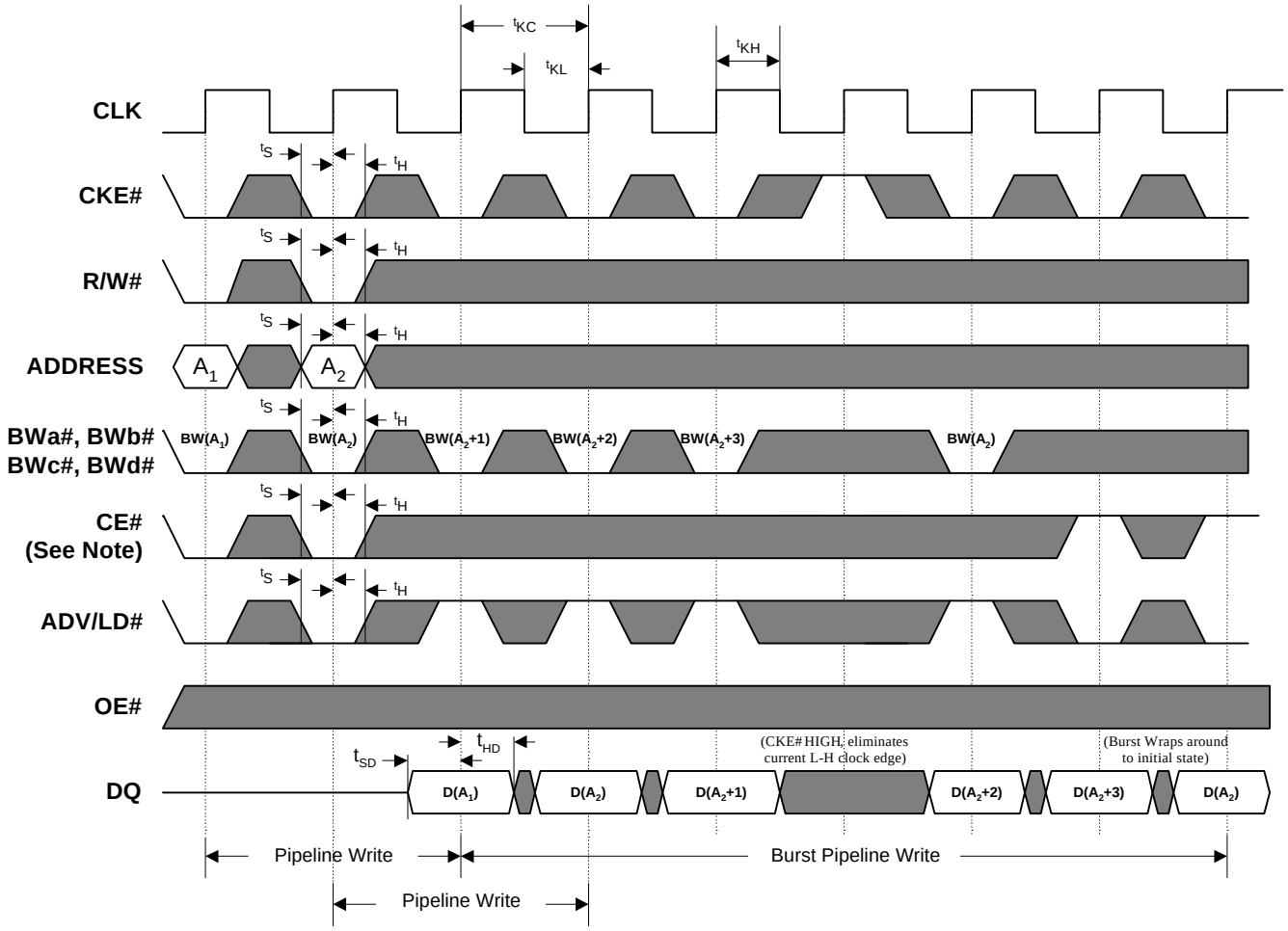
READ TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $Q(A_2)$ represents the first output from the external address A_2; $Q(A_2+1)$ represents the next output data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD# LOW .
4. R/W# is "Don't Care" when the SRAM is bursting (ADV/LD# sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM .
5. BWc# and BWd# apply to 256Kx36 device only.

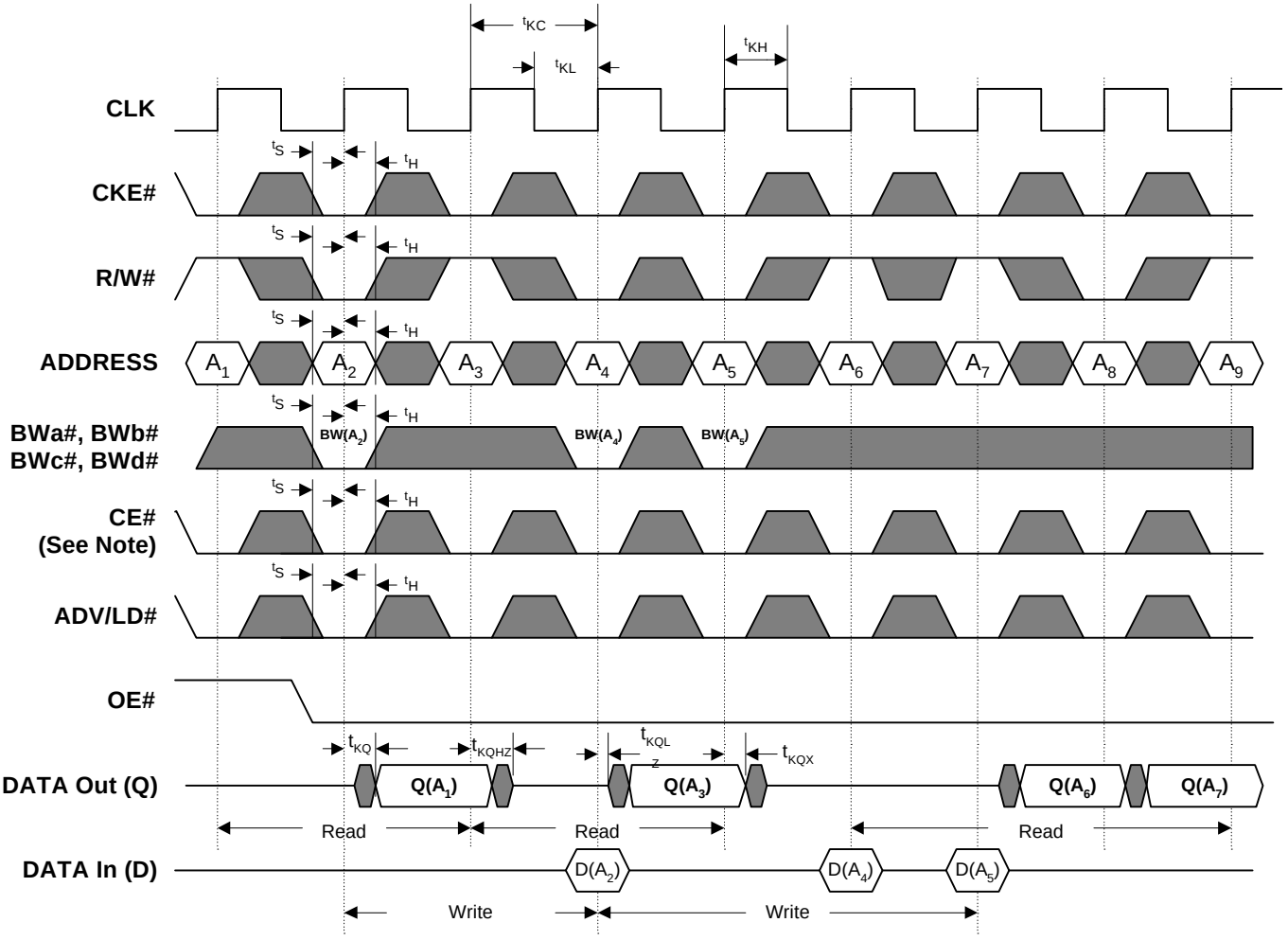
WRITE TIMIN G



Note:

1. D(A_1) represents the first input to the external address A1. D(A_2) represents the first input to the external address A_2; D(A_2+1) represents the next input data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input .
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH .
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD# LOW .
4. R/W# is “Don’t Care” when the SRAM is bursting (ADV/LD# sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM .
5. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM .
6. BWc# and BWd# apply to 256Kx36 device only.

READ/WRITE TIMIN G

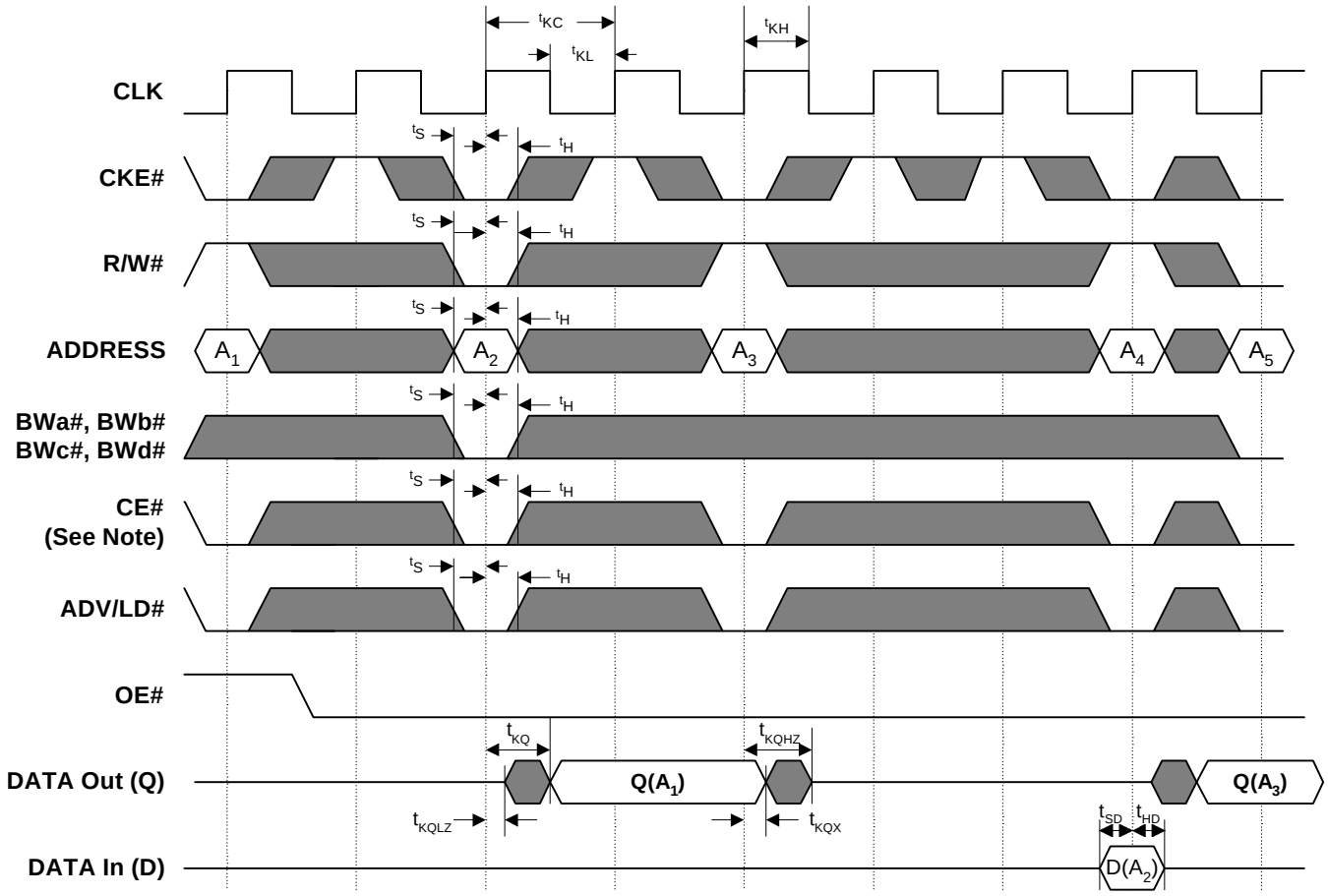


Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $D(A_2)$ represents the input data to the SRAM corresponding to address A_2.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH .
3. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM .

.4. BWc# and BWd# apply to 256Kx36 device only.

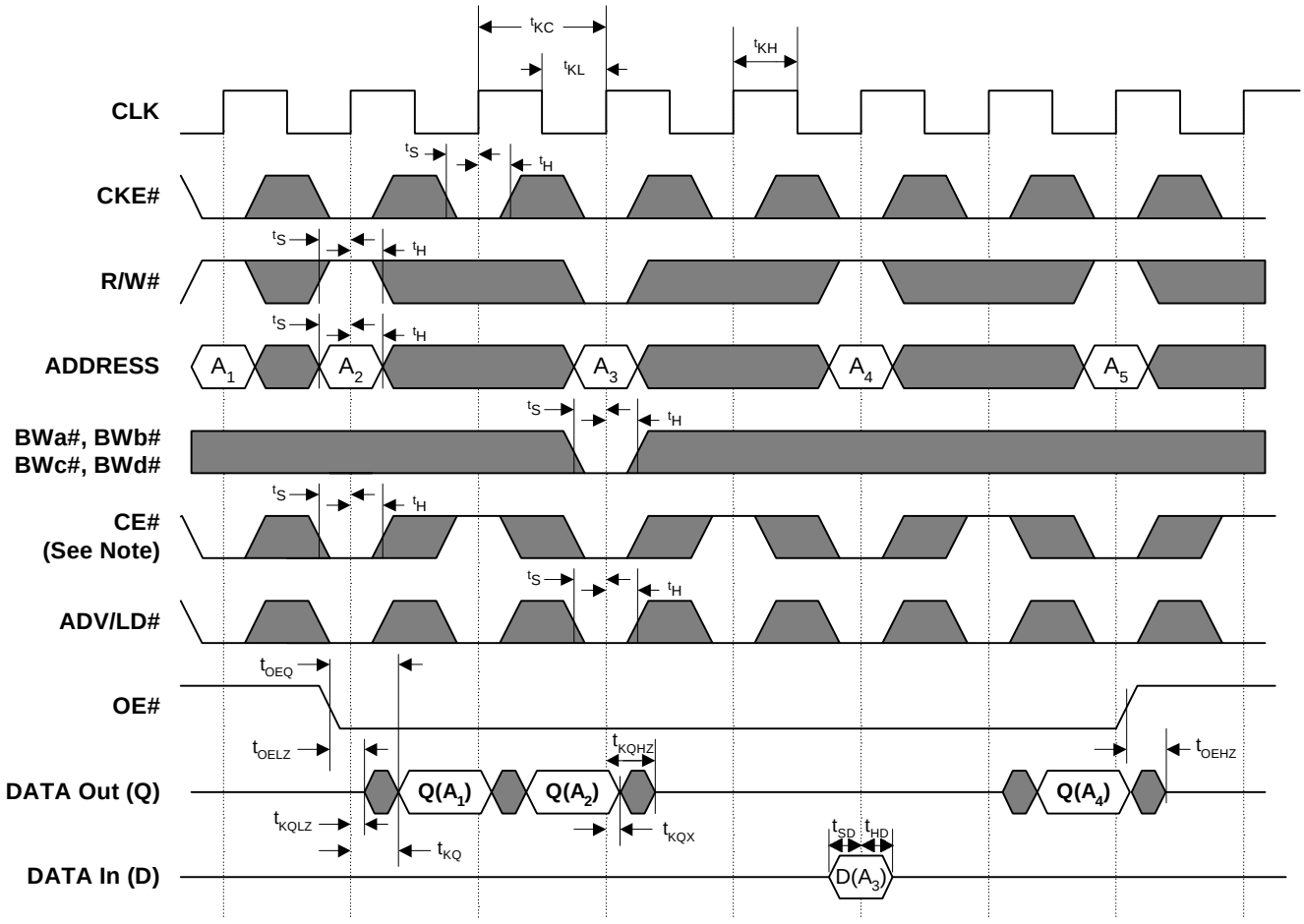
CKE# TIMIN G



Note:

1. Q(A_1) represents the first output from the external address A_1. D(A_2) represents the input data to the SRAM corresponding to address A_2.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH .
3. CKE# when sampled HIGH on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal register in the SRAM will retain their previous state .
4. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM .
5. BWc# and BWd# apply to 256Kx36 device only.

CE# TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $D(A_3)$ represents the input data to the SRAM corresponding to address A_3, etc.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH .
3. When either one of the Chip enables (CE#, CE2 or CE2#) is sampled inactive at the rising clock edge, a chip deselect cycle is initiated. The data-bus High-Z two cycles after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed .
4. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM .
5. BWc# and BWd# apply to 256Kx36 device only.

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

OVERVIEW

This device incorporates a serial boundary scan access port (TAP). This port is designed to operate in a manner consistent with IEEE Standard 1149.1-1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the critical speed path of the device. Nevertheless, the device supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using LVTTL/LVCMOS logic level signaling.

DISABLING THE JTAG FEATURE

It is possible to use this device without using the JTAG feature. To disable the TAP controller without interfering with normal operation of the device, TCK should be tied LOW (VSS) to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be pulled up to VCC through a resistor. TDO should be left unconnected. Upon power-up the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TCK - TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS - TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TDI - TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 3, TAP Controller State Diagram). It is allowable to leave this pin unconnected if it is not used in an application. The pin is pulled up internally, resulting in a logic HIGH level. TDI is connected to the most significant bit (MSB) of any register. (See Figure 4.)

TDO - TEST DATA OUT (OUTPUT)

The TDO output pin is used to serially clock data-out from the registers. The output that is active depending on the state of the TAP state machine (refer to Figure 3, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. TDO is connected to the least significant bit (LSB) of any register. (See Figure 4.)

PERFORMING A TAP RESET

The TAP circuitry does not have a reset pin (TRST#, which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH (VCC) for five rising edges of TCK and pre-loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

At power-up, the TAP is reset internally to ensure that TDO is in a High-Z state.

TEST ACCESS PORT (TAP) REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is connected between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction upon power-up or whenever the

controller is placed in the test-logic reset state. When the TAP controller is in the Capture-IR state, the two least significant bits of the serial instruction register are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

The bypass register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the device TAP to another device in the scan chain with minimum delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The Boundary scan register is connected to all the input and bidirectional I/O pins (not counting the TAP pins) on the device. This also includes a number of NC pins that are reserved for future needs. There are a total of 70 bits for x36 device and 51 bits for x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the device I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table describes the order in which the bits are connected. The first column defines the bit's position in the boundary scan register. The MSB of the register is connected to TDI, and LSB is connected to TDO. The second column is the signal name and the third column is the bump number. The third column is the TQFP pin number and the fourth column is the BGA bump number.

INDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the device as described in the Identification Register Definitions table.

TAP CONTROLLER INSTRUCTION SET

OVERWIEW

There are two classes of instructions defined in the IEEE Standard 1149.1-1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the device or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction sets for this device are listed in the following tables.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this device.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the device responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between two instructions. Unlike SAMPLE/PRELOAD instruction, EXTEST places the device outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in the instruction upon power-up and at any time the TAP controller is placed in the test-logic reset state.

SAMPLE-Z

If the High-Z instruction is loaded in the instruction register, all output pins are forced to a High-Z state and the boundary scan register is connected between TDI and TDO pins when the TAP controller is in a Shift-DR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. The PRELOAD portion of the command is not implemented in this device, so the device TAP controller is not fully IEEE 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded in the instruction register and the TAP controller is in the Capture-DR state, a snap shot of the data in the device's input and I/O buffers is loaded into the boundary scan register. Because the device system clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the input and I/O ring contents while the buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. To guarantee that the boundary scan register will capture the correct value of a signal, the device input signals must be stabilized long enough to meet the TAP controller's capture setup plus hold time (tCS plus tCH). The device clock input(s) need not be paused for any other TAP operation except capturing the input and I/O ring contents into the boundary scan register.

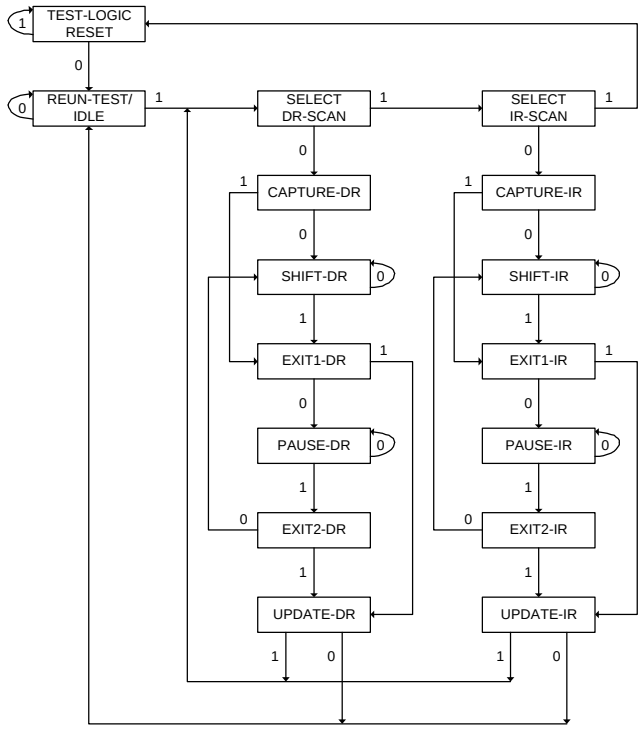
Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP controller is in the Shift-DR state, the bypass register is placed between TDI and TDO. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

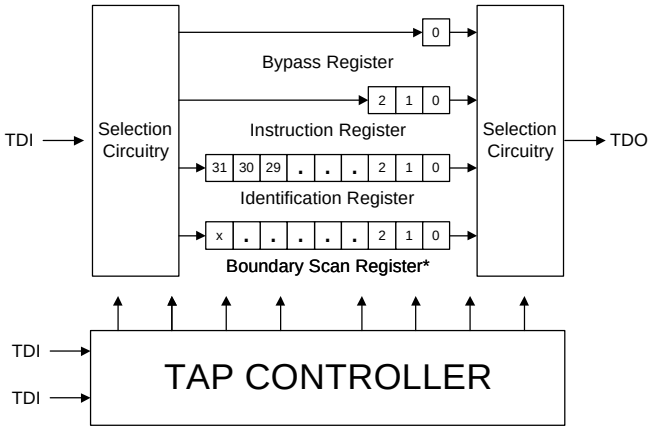
RESERVED

Do not use these instructions. They are reserved for future use.



Note: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Figure 3
TAP CONTROLLER STATE DIAGRAM



*X = 70 for the x36 configuration;
*X = 51 for the x18 configuration.

Figure 4
TAP CONTROLLER BLOCK DIAGRAM

TAP AC TEST CONDITIONS

Input pulse levels	VSS to 3.0V
Iutput rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load termination supply voltage	1.5V

TAP OUTPUT LOADS

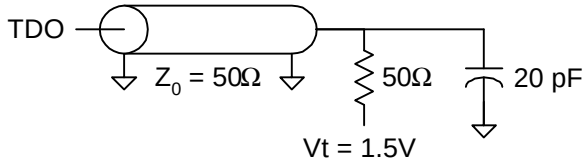


Figure 5
TAP AC OUTPUT LOAD EQUIVALENT

TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

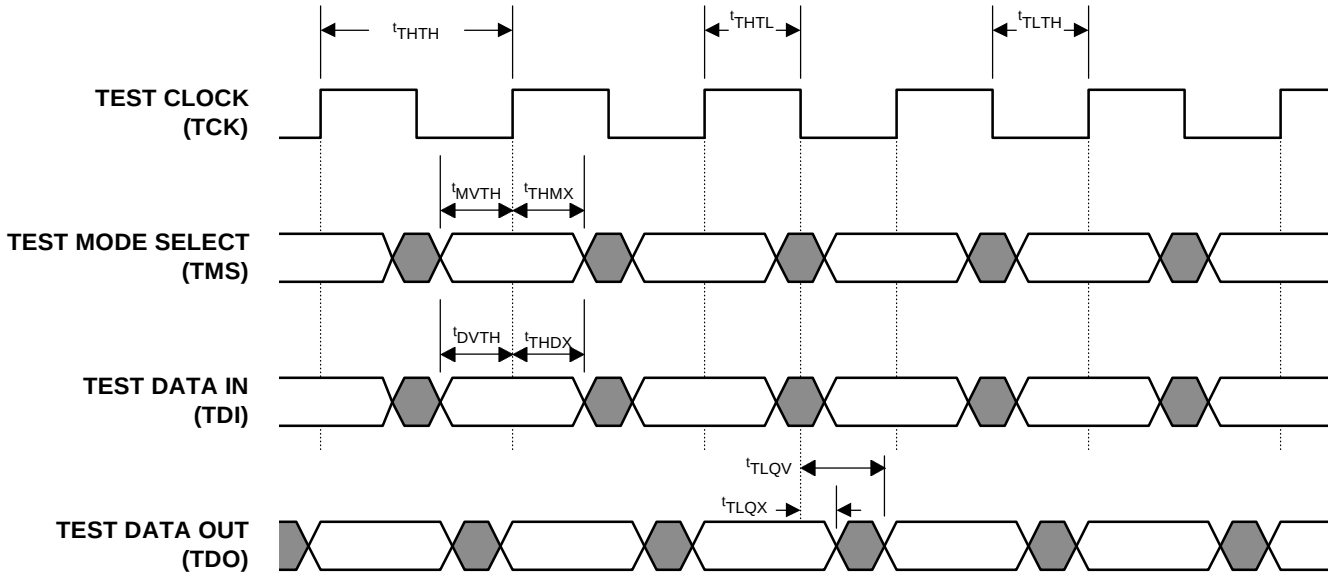
($20^oC \le T_j \le 110°C$; VCC = 3.3V -0.2V and +0.3V unless otherwise noted)

DESCRIPTIOP N	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage		V_{IH}	2.0	VCC + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{Il}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le VCC$	IL_I	-5.0	5.0	uA	
TMS and TDI input Leakage Current	$0V \le V_{IN} \le VCC$	IL_I	-30	30	uA	
Output Leakage Current	Output disabled, $0V \le V_{IN} \le VCCQ$	IL_O	-5.0	5.0	uA	
LVCMOS Output Low Voltage	I_{OLC} = 100uA	V_{OLC}		0.2		1, 3
LVCMOS Output High Voltage	I_{OHC} = 100uA	V_{OHC}	VCC - 0.2			1, 3
LVTTL Output Low Voltage	I_{OLT} = 8.0mA	V_{OLT}		0.4		1
LVTTL Output High Voltage	I_{OHT} = 8.0mA	V_{OHT}	2.4			1

NOTE:

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH}(AC) \le VCC + 1.5V$ for $t \le {}^tKHKH/2$.
   Undershoot: $V_{IL}(AC) \le -0.5V$ for $t \le {}^tKHKH/2$
   Power-up: $V_{IH} \le +3.6V$ and $VCC \le 3.135V$ and $VCCQ \le 1.4V$ for $t \le 200ms$
   During normal operation, VCCQ must not exceed VCC. Control input signals (such as R/W#, ADV/LD#, etc.) may not have pulse widths less than ${}^tKHKL$ (MIN).
3. This parameter is sampled.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) ($20^oC \le T_j \le 110°C$; VCC = 3.3V -0.2V and +0.3V)

DESCRIPTION	SYM	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	20		ns
Clock frequency	^fTF		50	MHz
Clock HIGH time	^tTHTL	8		ns
Clock LOW time	^tTLTH	8		ns
Output Times				
TCK LOW to TDO unknown	^tTLQX	0		ns
TCK LOW to TDO valid	^tTLQV		10	ns
TDI valid to TCK HIGH	^tDVTH	5		ns
TCK HIGH to TDI invalid	^tTHDX	5		ns
Setup Times				
TMS setup	^tMVTH	5		ns
Capture setup	^tCS	5		ns
Hold Times				
TMS hold	^tTHMX	5		ns
Capture hold	^tCH	5		ns

NOTE:

1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 5.

IDENTIFICATION REGISTER DEFINITION S

INSTRUCTION FIELD	256K x 36	512K x 18	DESCRIPTION
REVISION NUMBER (31:28)	XXXX	XXXX	Reserved for revision number.
DEVICE DEPTH (27:23)	00110	00111	Defines depth of 256K or 512K words.
DEVICE WIDTH (22:18)	00100	00011	Defines width of x36 or x18 bits.
RESERVED (17:12)	XXXXXX	XXXXXX	Reserved for future use.
GALVANTECH JEDEC ID CODE (11:1)	00011100100	00011100100	Allows unique identification of DEVICE vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

SCAN REGISTER SIZE S

REGISTER NAM E	BIT SIZE (x36)	BIT SIZE (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	70	51

INSTRUCTION CODE S

Instructio n	Code	Descriptio n
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. This instruction is not IEEE 1149.1-compliant.
IDCODE	001	Preloads ID register with vendor ID code and places it between TDI and TDO. This instruction does not affect device operations.
SAMPLE-Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state.
RESERVED	011	Do not use these instructions; they are reserved for future use.
SAMPLE/PRE-LOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not affect device oper a-tions. This instruction does not implement IEEE 1149.1 PRELOAD function and is therefore not 1149.1-compliant.
RESERVED	101	Do not use these instructions; they are reserved for future use.
RESERVED	110	Do not use these instructions; they are reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This instruction does not affect device operations.

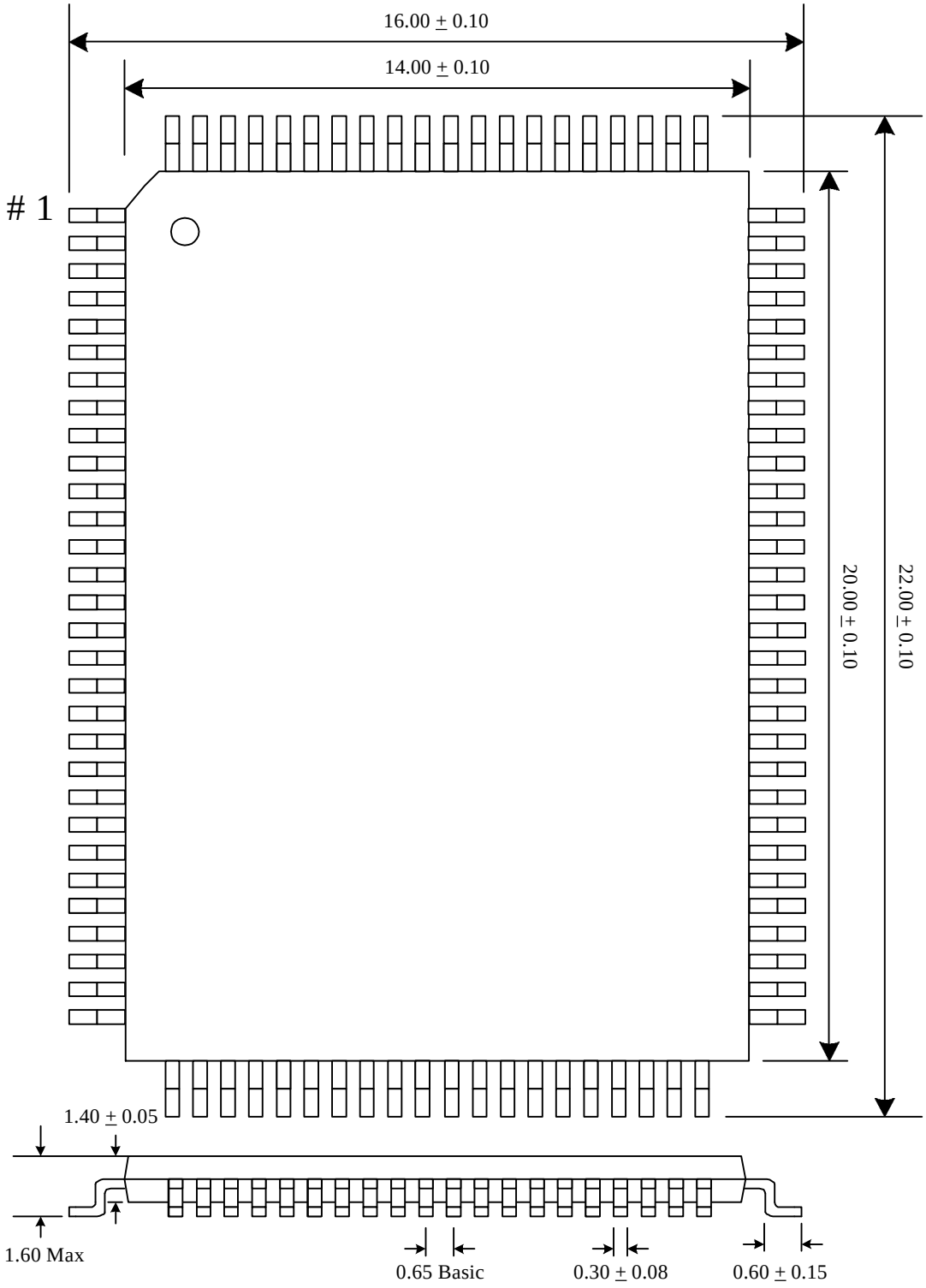
BOUNDARY SCAN ORDER (256K x 36)

BIT#	SINGAL NAME	TQFP	BUMP ID
1	SA	44	2R
2	SA	45	3T
3	SA	46	4T
4	SA	47	5T
5	SA	48	6R
6	SA	49	3B
7	SA	50	5B
8	DQa	51	6P
9	DQa	52	7N
10	DQa	53	6M
11	DQa	56	7L
12	DQa	57	6K
13	DQa	58	7P
14	DQa	59	6N
15	DQa	62	6L
16	DQa	63	7K
17	ZZ	64	7T
18	DQb	68	6H
19	DQb	69	7G
20	DQb	72	6F
21	DQb	73	7E
22	DQb	74	6D
23	DQb	75	7H
24	DQb	78	6G
25	DQb	79	6E
26	DQb	80	7D
27	SA	81	6A
28	SA	82	5A
29	SA	83	4G
30	NC	84	4A
31	ADV/LD#	85	4B
32	OE#	86	4F
33	CKE#	87	4M
34	R/W#	88	4H
35	CLK	89	4K
36	CE2#	92	6B
37	BWa#	93	5L
38	BWb#	94	5G
39	BWc#	95	3G
40	BWd#	96	3L
41	CE2	97	2B
42	CE#	98	4E
43	SA	99	3A
44	SA	100	2A
45	DQc	1	2D
46	DQc	2	1E
47	DQc	3	2F
48	DQc	6	1G
49	DQc	7	2H
50	DQc	8	1D
51	DQc	9	2E
52	DQc	12	2G
53	DQc	13	1H
54	NC	14	5R
55	DQd	18	2K
56	DQd	19	1L
57	DQd	22	2M
58	DQd	23	1N
59	DQd	24	2P
60	DQd	25	1K
61	DQd	28	2L
62	DQd	29	2N
63	DQd	30	1P
64	MODE	31	3R
65	SA	32	2C
66	SA	33	3C
67	SA	34	5C
68	SA	35	6C
69	SA1	36	4N
70	SA0	37	4P

BOUNDARY SCAN ORDER (512K x 18)

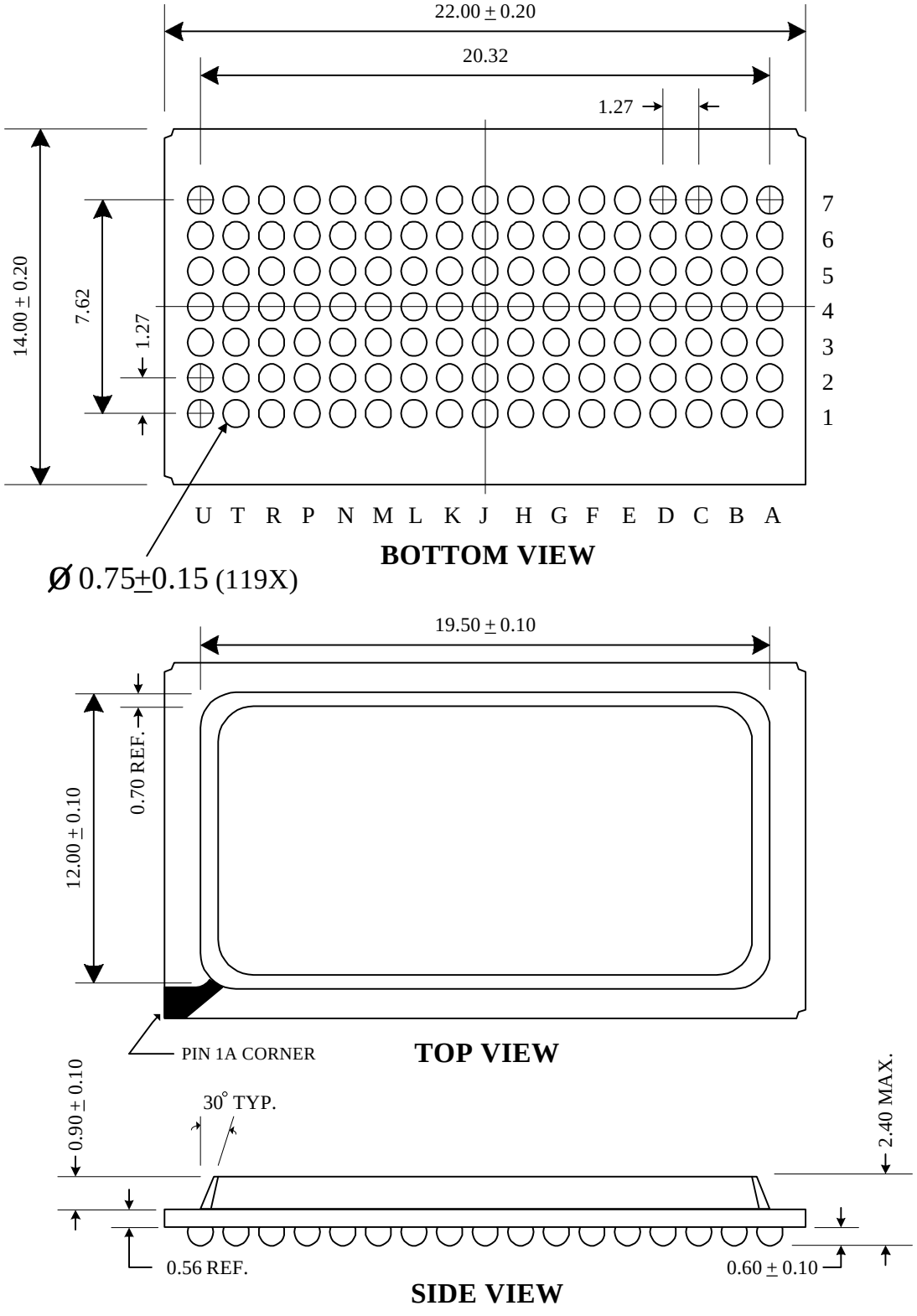
BIT#	SINGAL NAME	TQFP	BUMP ID
1	SA	44	2R
2	SA	45	2T
3	SA	46	3T
4	SA	47	5T
5	SA	48	6R
6	SA	49	3B
7	SA	50	5B
8	DQa	58	7P
9	DQa	59	6N
10	DQa	62	6L
11	DQa	63	7K
12	ZZ	64	7T
13	DQa	68	6H
14	DQa	69	7G
15	DQa	72	6F
16	DQa	73	7E
17	DQa	74	6D
18	SA	80	6T
19	SA	81	6A
20	SA	82	5A
21	SA	83	4G
22	NC	84	4A
23	ADV/LD#	85	4B
24	OE#	86	4F
25	CKE#	87	4M
26	R/W#	88	4H
27	CLK	89	4K
28	CE2#	92	6B
29	BWa#	93	5L
30	BWb#	94	3G
31	CE2	97	2B
32	CE#	98	4E
33	SA	99	3A
34	SA	100	2A
35	DQb	8	1D
36	DQb	9	2E
37	DQb	12	2G
38	DQb	13	1H
39	NC	14	5R
40	DQb	18	2K
41	DQb	19	1L
42	DQb	22	2M
43	DQb	23	1N
44	DQb	24	2P
45	MODE	31	3R
46	SA	32	2C
47	SA	33	3C
48	SA	34	5C
49	SA	35	6C
50	SA1	36	4N
51	SA0	37	4P

100 Pin TQFP Package Dimension s



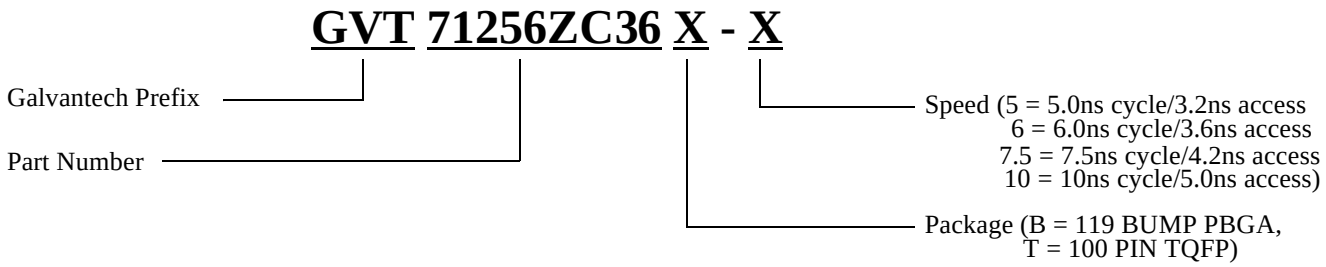
Note: All dimensions in Millimeters

7 x 17 (119-lead) BGA Dimension s



Note: All dimensions in Millimeters

Ordering Information for 256K x 36



Ordering Information for 512K x 18