# M66312P/FP

## 8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

## DESCRIPTION

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

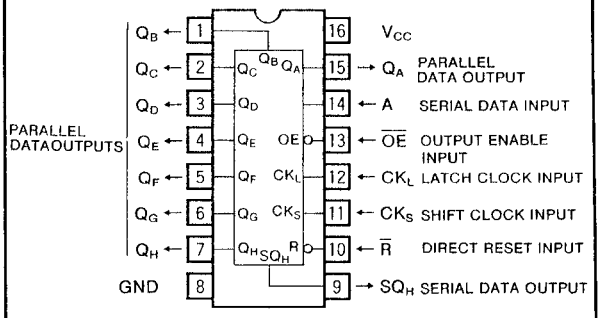
This product guarantees the output electric current of 16mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

## FEATURES

- High output current $I_{OL}$=16mA, $I_{OH}$=−16mA
- High speed (clock freguency) : 30MHz (typ)
  ($C_L$=50pF, $V_{CC}$=5V)
- Low power dissipation : 20μW/package (max)
  ($V_{CC}$=5V, Ta=25℃, quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range : Ta=−40~+85℃

## PIN CONFIGURATION (TOP VIEW)

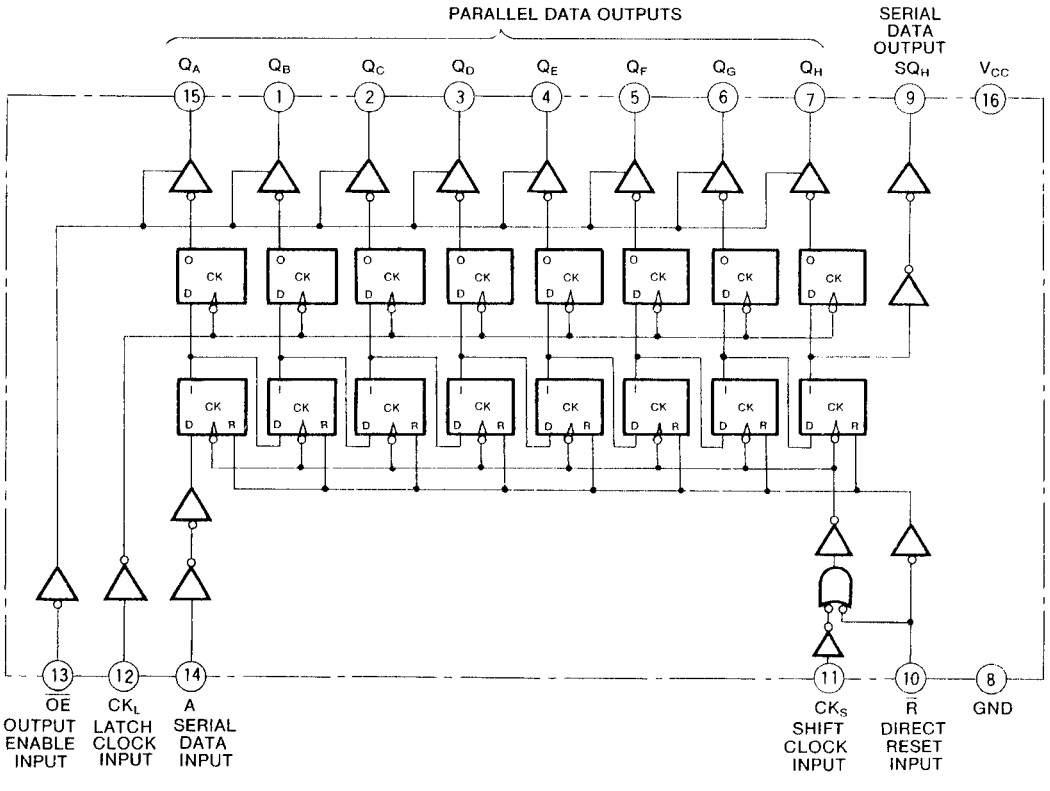



Outline 16P4
16P2N-A

## APPLICATION

LED array drive of PRINTER
LED array drive of BUTTON TELEPHONE

## LOGIC DIAGRAM



## 8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

## FUNCTIONAL DESCRIPTION

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input $CK_S$ and latch clock input $CK_L$ are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shiting registers one by one when a pulse is impressed to $CK_S$. When A is "H", the signal of "H" shifts. When A is "L", the signal of "L" shifts.

When the pulse is impressed to $CK_L$, the contents of the shifting register at that time are stored in a latching register, and they appear in the output from $Q_A$ through $Q_H$ are 3-state outputs.

To extend the number of bits, serial data output $SQ_H$ is used to output the 8-bit of the shift register.

By connecting CKs and $CK_L$, the shift register state delayed by 1 clock cycle is output at $Q_A$ through $Q_H$.

When reset input $\overline{R}$ is low, shift register and $SQ_H$ will be reset. To reset $Q_A$ through $Q_H$ to low-level, $CK_L$ must be changed from low-level to high-level after the shift register is reset by $\overline{R}$.

When output-enable input $\overline{OE}$ is high, $Q_A$ through $Q_H$ will become high impedance state, but $SQ_H$ is not changed. Even if $\overline{OE}$ is changed, shift operation is not affected.

## FUNCTION TABLE (Note : 1)

| Operation mode | | Input | | | | | Parallel data output | | | | | | | | Serial data output |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $\overline{R}$ | $CK_S$ | $CK_L$ | A | $\overline{OE}$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ | $Q_H$ | $SQ_H$ |
| Reset | Shift $t_1$ | L | X | X | X | L | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ | $Q_E^0$ | $Q_F^0$ | $Q_G^0$ | $Q_H^0$ | L |
| | Latch $t_2$ | X | X | ↑ | X | L | L | L | L | L | L | L | L | L | L |
| Shift latch operation | Shift $t_1$ | H | ↑ | X | H | L | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ | $Q_E^0$ | $Q_F^0$ | $Q_G^0$ | $Q_H^0$ | $q_G^0$ |
| | Latch $t_2$ | H | X | ↑ | X | L | H | $q_A^0$ | $q_B^0$ | $q_C^0$ | $q_D^0$ | $q_E^0$ | $q_F^0$ | $q_G^0$ | $q_G^0$ |
| | Shift $t_1$ | H | ↑ | X | L | L | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ | $Q_E^0$ | $Q_F^0$ | $Q_G^0$ | $Q_H^0$ | $q_G^0$ |
| | Latch $t_2$ | H | X | ↑ | X | L | L | $q_A^0$ | $q_B^0$ | $q_C^0$ | $q_D^0$ | $q_E^0$ | $q_F^0$ | $q_G^0$ | $q_G^0$ |
| 3 state | | X | X | X | X | H | Z | Z | Z | Z | Z | Z | Z | Z | $q_H$ |

Note 1 : ↑ : Change from low-level to high-level
$Q^0$ : Output state Q before $CK_L$ changed
X : Irrelevant
$q^0$ : Contents of shift register before $CK_S$ changed
q : Contents of shift register
$t_1$, $t_2$ : $t_2$ is set after $t_1$ is set
Z : High impedance

## 8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

## ABSOLUTE MAXIMUM RATINGS (Ta=−40∼+85℃, unless otherwise noted)

| Symbol | Parameter | | Conditions | Ratings | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.5∼+7.0 | V |
| $V_I$ | Input voltage | | | −0.5∼$V_{CC}$+0.5 | V |
| $V_O$ | Output voltage | | | −0.5∼$V_{CC}$+0.5 | V |
| $I_{IK}$ | Input protection diode current | | $V_I$ < 0V | −20 | mA |
| | | | $V_I$ > $V_{CC}$ | 20 | |
| $I_{OK}$ | Output parasitic diode current | | $V_O$ < 0V | −20 | mA |
| | | | $V_O$ > $V_{CC}$ | 20 | |
| $I_O$ | Output current per output pin | $Q_A$∼$Q_H$ | | ±35 | mA |
| | | $SQ_H$ | | ±25 | |
| $I_{CC}$ | Supply/GND current | | $V_{CC}$, GND | ±132 | mA |
| Pd | Power dissipation | | (Note 2) | 500 | mW |
| Tstg | Storage temperature range | | | −65∼+150 | ℃ |

Note 2 : M66312FP ; $T_a$=−40∼+70℃, $T_a$=70∼85℃ are derated at −6mW/℃.

## RECOMMENDED OPERATING CONDITIONS ($T_a$=−40∼+85℃, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| Topr | Operating temperature range | | −40 | | +85 | ℃ |
| tr, tf | Input rising and falling time | $V_{CC}$=4.5V | 0 | | 500 | ns |
| | | $V_{CC}$=5.5V | 0 | | 400 | |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$=4.5∼5.5V, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_a$=25℃ | | | $T_a$=−40∼+85℃ | | |
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High-level input voltage | $V_O$=0.1V, $V_{CC}$−0.1V<br>$\|I_O\|$=20μA | | 0.70×$V_{CC}$ | | | 0.70×$V_{CC}$ | | V |
| $V_{IL}$ | Low-level input voltage | $V_O$=0.1V, $V_{CC}$−0.1V<br>$\|I_O\|$=20μA | | | | 0.30×$V_{CC}$ | | 0.30×$V_{CC}$ | V |
| $V_{OH}$ | High-level output voltage<br>$Q_A$∼$Q_H$ | $V_I$=$V_{IH}$, $V_{IL}$ | $I_{OH}$=−20μA | $V_{CC}$−0.1 | | | $V_{CC}$−0.1 | | V |
| | | $V_{CC}$=4.5V | $I_{OH}$=−16mA | 3.70* | | | 3.55* | | |
| $V_{OH}$ | High-level output voltage<br>$SQ_H$ | $V_I$=$V_{IH}$, $V_{IL}$ | $I_{OH}$=−20μA | $V_{CC}$−0.1 | | | $V_{CC}$−0.1 | | V |
| | | $V_{CC}$=4.5V | $I_{OH}$=−4mA | 4.0 | | | 3.9 | | |
| $V_{OL}$ | Low-level output voltage<br>$Q_A$∼$Q_H$ | $V_I$=$V_{IH}$, $V_{IL}$ | $I_{OL}$=20μA | | | 0.1 | | 0.1 | V |
| | | $V_{CC}$=4.5V | $I_{OL}$=16mA | | | 0.7* | | 0.85* | |
| $V_{OL}$ | Low-level output voltage<br>$SQ_H$ | $V_I$=$V_{IH}$, $V_{IL}$ | $I_{OL}$=20μA | | | 0.1 | | 0.1 | V |
| | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | | 0.4 | | 0.5 | |
| $I_{IH}$ | High-level input current | $V_I$=$V_{CC}$, $V_{CC}$=5.5V | | | | 0.1 | | 1.0 | μA |
| $I_{IL}$ | Low-level input current | $V_I$=GND, $V_{CC}$=5.5V | | | | −0.1 | | −1.0 | μA |
| $I_{OZH}$ | Off state high-level output current $Q_A$∼$Q_H$ | $V_I$=$V_{IH}$, $V_{IL}$ | $V_O$=$V_{CC}$ | | | 1.0 | | 10.0 | μA |
| $I_{OZL}$ | Off state low-level output current $Q_A$∼$Q_H$ | $V_{CC}$=5.5V | $V_O$=GND | | | −1.0 | | −10.0 | μA |
| $I_{CC}$ | Quiescent supply current | $V_I$=$V_{CC}$, GND, $V_{CC}$=5.5V | | | | 4.0 | | 40.0 | μA |

* : Limits of single PIN operating state

## 8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

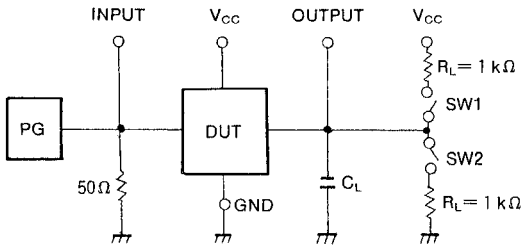
## SWITCHING CHARACTERISTICS ($V_{CC}$= 5 V)

| Symbol | Parameter | Test conditions | Limits | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=25℃ | | | $T_a$=−40~+85℃ | | |
| | | | Min | Typ | Max | Min | Max | |
| $f_{max}$ | Maximum clock frequency | $C_L$=50pF | 15 | | | 12 | | MHz |
| $t_{PLH}$ | Low-level to high-level and high-level to low-level | | | | 70 | | 88 | ns |
| $t_{PHL}$ | output propagation time CKs-$SQ_H$ | $C_L$=15pF | | | 70 | | 88 | ns |
| $t_{PHL}$ | High-level to low-level output propagation time $\overline{R}$-$SQ_H$ | (Note 3) | | | 60 | | 76 | ns |
| $t_{PLH}$ | Low-level to high-level and high-level to low-level | $C_L$=50pF | | | 60 | | 76 | ns |
| $t_{PHL}$ | output propagation time $CK_L$-$Q_A$~$Q_H$ | (Note 3) | | | 60 | | 76 | ns |
| $t_{PLZ}$ | Output disable time from low-level and high-level | $C_L$=5pF | | | 50 | | 64 | ns |
| $t_{PHZ}$ | $\overline{OE}$-$Q_A$~$Q_H$ | (Note 3) | | | 50 | | 64 | ns |
| $t_{PZL}$ | Output enable time to low-level and high-level | $C_L$=50pF | | | 56 | | 70 | ns |
| $t_{PZH}$ | $\overline{OE}$-$Q_A$~$Q_H$ | (Note 3) | | | 56 | | 70 | ns |

## TIMING REQUIREMENTS ($V_{CC}$= 5 V)

| Symbol | Parameter | Test conditions | Limits | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=25℃ | | | $T_a$=−40~+85℃ | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_w$ | $CK_S$, $CK_L$, $\overline{R}$ pulse width | | 32 | | | 40 | | ns |
| $t_{su}$ | A setup time with respect to $CK_S$ | | 40 | | | 50 | | ns |
| $t_{su}$ | $CK_S$ setup time with respect to $CK_L$ | | 40 | | | 50 | | ns |
| $t_h$ | A hold time with respect to $CK_S$ | | 10 | | | 10 | | ns |
| $t_{rec}$ | $\overline{R}$ recovery time with respect to $CK_S$ | | 20 | | | 26 | | ns |

Note 3 : Test Circuit




| Item | SW1 | SW2 |
|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | OPEN | OPEN |
| $t_{PLZ}$ | CLOSE | OPEN |
| $t_{PHZ}$ | OPEN | CLOSE |
| $t_{PZL}$ | CLOSE | OPEN |
| $t_{PZH}$ | OPEN | CLOSE |

(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr =6ns, tf=6ns

(2) The capacitance $C_L$ includes stray wiring capacitance and the probe input capacitance.