OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6665-xx

DOT MATRIX LCD CONTROLLER WITH 17-DOT COMMON DRIVER AND 80-DOT SEGMENT DRIVER

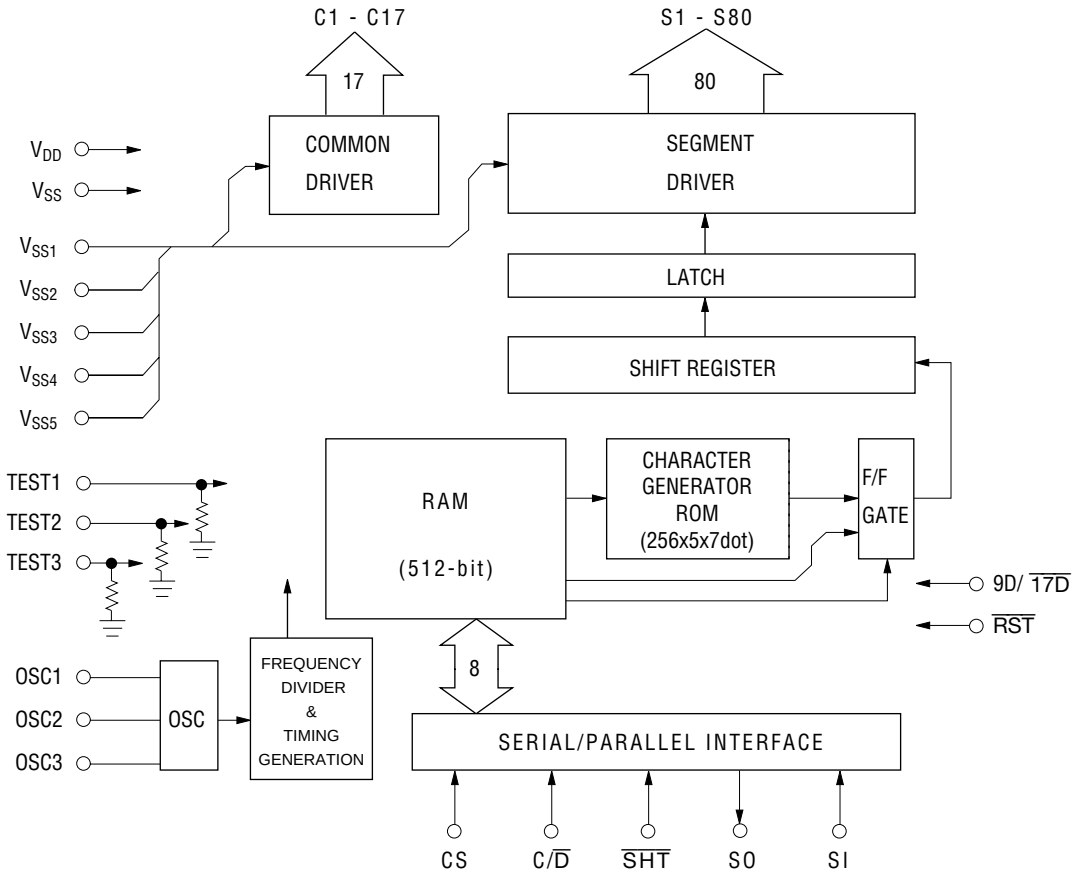
GENERAL DESCRIPTION

The MSM6665-xx is a dot-matrix LCD control driver which has functions of displaying characters, cursor and arbitrators.
The MSM6665-xx is provided with a 17-dot common driver, 80-dot segment driver, display RAM and character ROM, and is controlled with the commands from the serial interface.
The character ROM can change the font data by mask option.
The MSM6665-01 has standard ROM with 256 different character fonts.
The MSM6665-xx can drive a variety of LCD panels because of the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

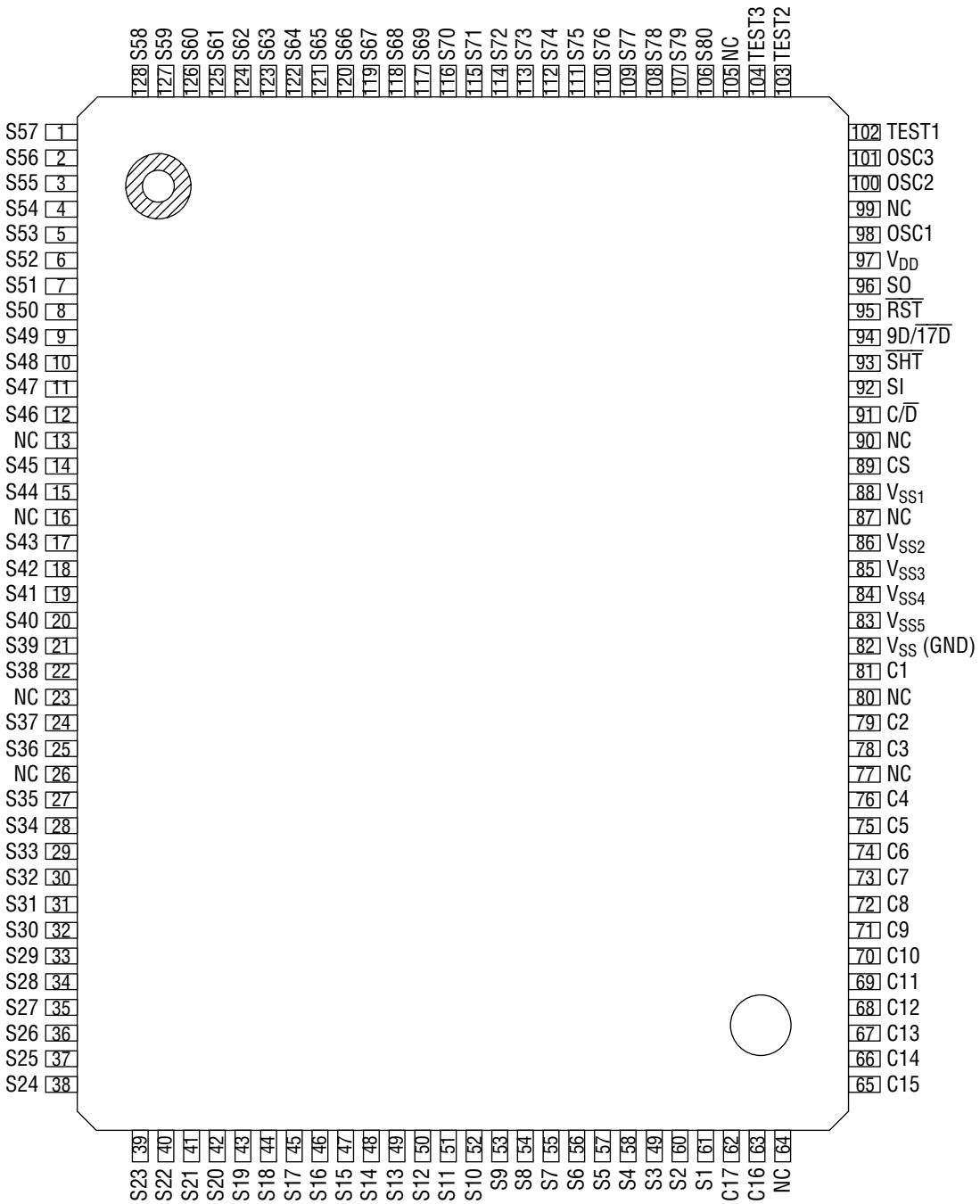
FEATURES

- Logic supply voltage : 2.5 to 5.5 V
- LCD driving voltage : 3.0 to 6.0 V
- Serial interface
- Contains a 17-dot common driver and an 80-dot segment driver
- Contains ROM with character fonts of (5 x 7 dot) x 256
- Built-in RC oscillator circuit
- Provided with 80-dot arbitrators
- Switchable between 1/9 duty (1 line; characters + cursor + arbitrator) and 1/17 duty (2 lines; characters + cursor, 1 line; arbitrator)
- Character blink operation can be switched between all-characters lighting-on mode and all-characters lighting-off mode
- Arbitrator blink operation can be switched between 5-dot unit mode and 1-dot unit mode
- Package options:
  128-pin plastic QFP (QFP128-P-1420-0.50-K) (Product name: MSM6665-01GS-K)
  Al pad chip (Product name: MSM6665-xx)
  xx indicates code number.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connection

128-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable pin
Supply Voltage	V_{DD}	Ta=25°C, V_{DD}–V_{SS}	–0.3 to +7	V	V_{DD}, V_{SS}
Bias Voltage	V_{BI}	Ta=25°C, V_{DD}–V_{SS5}	–0.3 to +7	V	V_{DD}, V_{SS5}
Input Voltage	V_I	—	–0.3 to V_{DD}+0.3	V	All inputs
Power Dissipation	P_D	Ta=85°C *1 QFP128-1420	630	mW	—
Storage Temperature	T_{STG}	—	–55 to +150	°C	—

*1: The power dissipation depends on the heat sink characteristic of the package. Set a junction temperature at 150°C or lower.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit	Applicable pin
Supply Voltage	V_{DD}	V_{DD}–V_{SS}	2.5 to 5.5	V	V_{DD}, V_{SS}
Bias Voltage	V_{BI}	V_{DD}–V_{SS5}	3 to 6	V	V_{DD}, V_{SS5}
Operating Frequency	f_{op}	*2	65 to 115	kHz	OSC1
Operating Temperature	T_{op}	—	–40 to +85	°C	—

*2: RC oscillation, external input clock frequency

List of bias voltages

(V_{BI}=V_{DD}–V_{SS5})

Symbol	1/5 bias	1/4 bias	Remarks
V_{DD}	V_{DD}	V_{DD}	Highest voltage
V_{SS1}	V_{DD}–1/5V_{BI}	V_{DD}–1/4V_{BI}	—
V_{SS2}	V_{DD}–2/5V_{BI}	V_{DD}–2/4V_{BI}	—
V_{SS3}	V_{DD}–3/5V_{BI}		—
V_{SS4}	V_{DD}–4/5V_{BI}	V_{DD}–3/4V_{BI}	—
V_{SS5}	V_{SS5}	V_{SS5}	Lowest voltage

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD}=2.5 to 3.5V, V_{BI}=3 to 6V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage 1	V_{IH1}	External clock input	0.8V_{DD}	—	V_{DD}	V	OSC1
"L" Input Voltage 1	V_{IL1}	External clock input	0	—	0.2V_{DD}	V	OSC1
"H" Input Voltage 2	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	Input pins except OSC1
"L" Input Voltage 2	V_{IL2}	—	0	—	0.2V_{DD}	V	Input pins except OSC1
"H" Input Current 1	I_{IH1}	V_I=V_{DD}	—	—	1	µA	Input pins except TEST
"L" Input Current	I_{IL}	V_I=0V	—	—	–1	µA	Input pins
"H" Input Current 2	I_{IH2}	Pull-down resistance, V_I=V_{DD}	0.05	—	0.4	mA	TEST1-TEST3
"H" Output Voltage	V_{OH}	I_O=–1.5mA	V_{DD}–0.5	—	—	V	S0
"L" Output Voltage	V_{OL}	I_O=500µA	—	—	0.5	V	S0
OFF Leakage	I_{OFF}	V_I=V_{DD}/0V	—	—	±1	µA	S0
OSC "H" Output Current	I_{OH}	V_I=V_{DD}–0.5V	—	—	–0.25	mA	OSC2, OSC3
OSC "L" Output Current	I_{OL}	V_I=0.5V	0.25	—	—	mA	OSC2, OSC3
COM Output Resistance	R_C	I_O=±50µA	—	—	6	kΩ	C1-C17
SEG Output Resistance	R_S	I_O=±10µA	—	—	15	kΩ	S1-S80
Supply Current 1	I_{DD1}	RC oscillation, f≒80kHz C=56pF, R_S=10kΩ R=76kΩ, no load	—	—	0.5	mA	—
Supply Current 2	I_{DD2}	External clock, f=80kHz	—	—	100	µA	—

DC Characteristics (2)

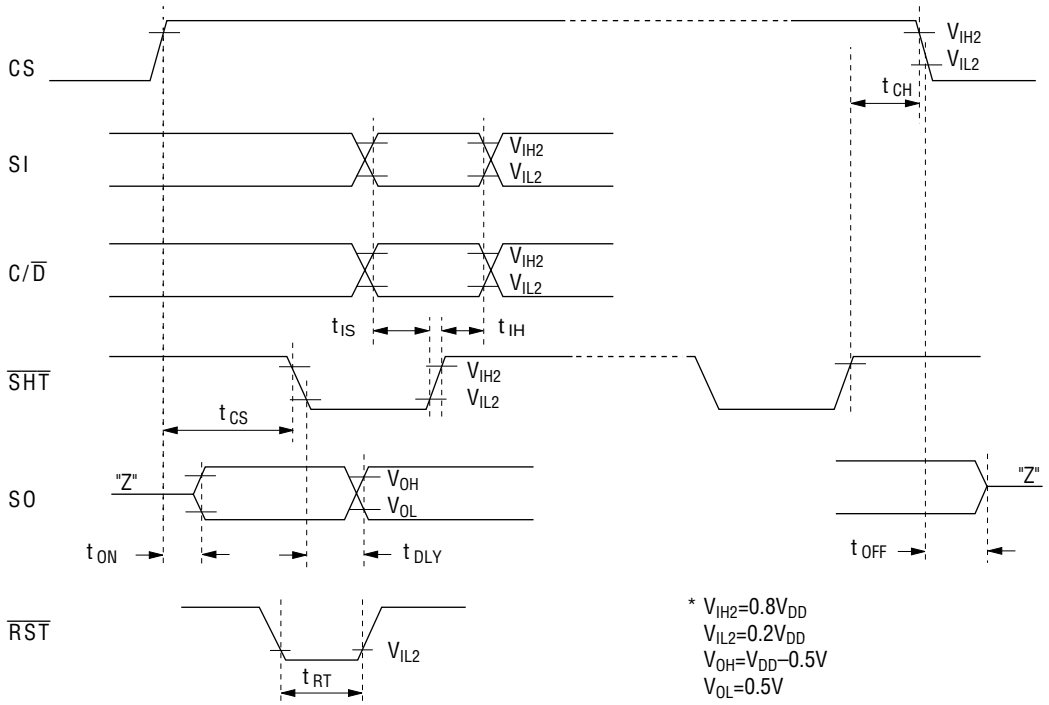
(V_{DD}=4.5 to 5.5V, V_{BI}=3 to 6V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage 1	V_{IH1}	External clock input	0.8V_{DD}	—	V_{DD}	V	OSC1
"L" Input Voltage 1	V_{IL1}	External clock input	0	—	0.2V_{DD}	V	OSC1
"H" Input Voltage 2	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	Input pins except OSC1
"L" Input Voltage 2	V_{IL2}	—	0	—	0.2V_{DD}	V	Input pins except OSC1
"H" Input Current 1	I_{IH1}	V_I=V_{DD}	—	—	1	µA	Input pins except TEST
"L" Input Current	I_{IL}	V_I=0V	—	—	–1	µA	Input pins
"H" Input Current 2	I_{IH2}	Pull-down resistance, V_I=V_{DD}	0.3	—	1.4	mA	TEST1-TEST3
"H" Output Voltage	V_{OH}	I_O=–1.5mA	V_{DD}–0.5	—	—	V	S0
"L" Output Voltage	V_{OL}	I_O=500µA	—	—	0.5	V	S0
OFF Leakage	I_{OFF}	V_I=V_{DD}/0V	—	—	±1	µA	S0
OSC "H" Output Current	I_{OH}	V_I=V_{DD}–0.5V	—	—	–0.5	mA	OSC2, OSC3
OSC "L" Output Current	I_{OL}	V_I=0.5V	0.5	—	—	mA	OSC2, OSC3
COM Output Resistance	R_C	I_O=±50µA	—	—	6	kΩ	C1-C17
SEG Output Resistance	R_S	I_O=±10µA	—	—	15	kΩ	S1-S80
Supply Current 1	I_{DD1}	RC oscillation, f≒80kHz C=56pF, R_S=10kΩ R=76kΩ, no load	—	—	1.1	mA	—
Supply Current 2	I_{DD2}	External clock, f=80kHz	—	—	400	µA	—

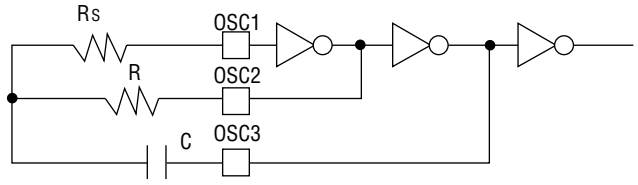
AC Characteristics

(V_{DD}–V_{SS}=2.5 to 5.5V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS Setup Time	t_{CS}	—	300	—	ns
CS Hold Time	t_{CH}	—	200	—	
SO ON Delay Time	t_{ON}	—	—	200	
SO OFF Delay Time	t_{OFF}	—	—	200	
SO Output Delay Time	t_{DLY}	C_L=45pF	0	200	
Input Setup Time	t_{IS}	—	200	—	
Input Hold Time	t_{IH}	—	200	—	
Input Waveform Rise Time, Fall Time	t_r, t_f	All inputs	—	50	
Reset Pulse Input Pulse Width	t_{RT}	—	5	—	µs

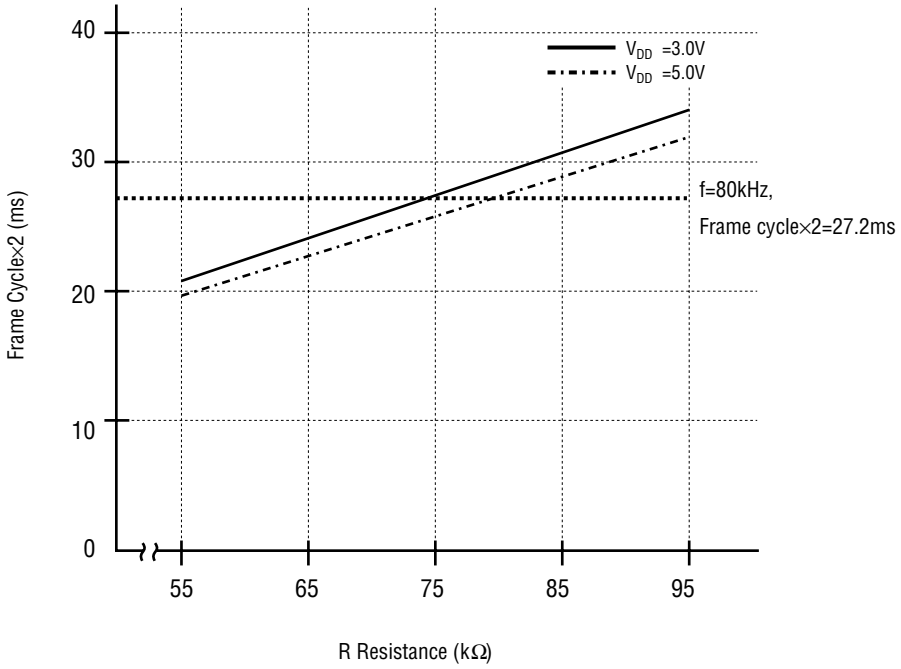


Oscillation Circuit



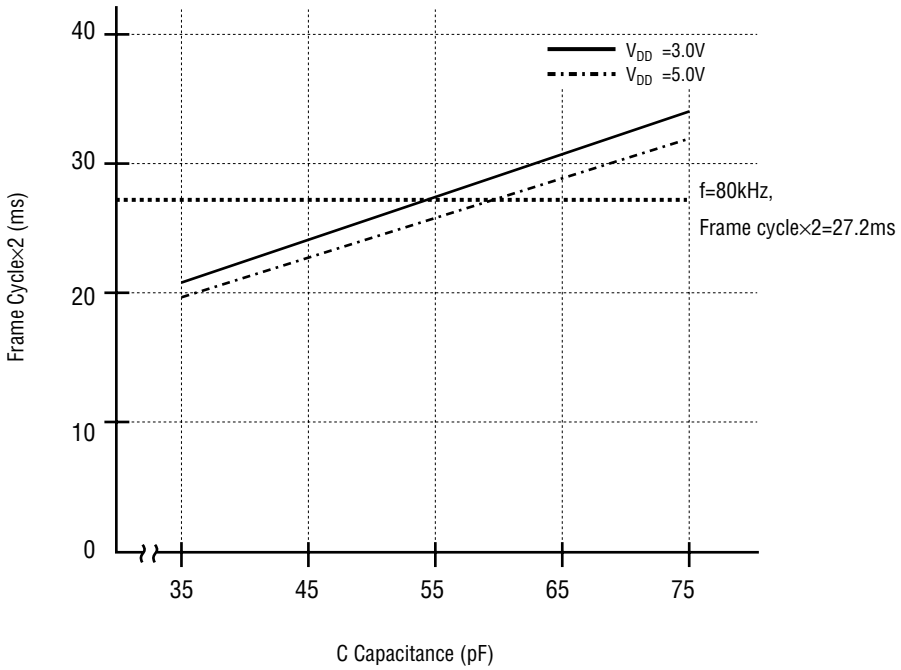
Oscillation Characteristics 1 (Rs=10kΩ, C=56pF, R variable characteristics)

1/17 duty



Oscillation Characteristics 2 (Rs=10kΩ, R=75kΩ, C variable characteristics)

1/17 duty



FUNCTIONAL DESCRIPTION

Pin Functional Description

- SI (Serial Input)

  Input pin for inputting serially commands and display data in an 8-bit unit.
  "H"="1" and "L"="0".
  When CS pin is at "H" level, read-in is executed by the leading edge of $\overline{SHT}$.
  Whether input data is a command or data is determined by selecting a C/$\overline{D}$ level at the 8th leading edge of $\overline{SHT}$.
  The input data is a command if C/$\overline{D}$="H", and display data if C/$\overline{D}$="L".

- C/$\overline{D}$ (Command/$\overline{Data}$)

  Input pin for determining whether input data for SI pin is a command or display data. Read-in is executed by the 8th leading edge of $\overline{SHT}$. The input data is a command if C/$\overline{D}$="H", and display data if C/$\overline{D}$="L".

- $\overline{SHT}$ ($\overline{Shift\ Clock}$)

  Clock input pin for reading-in SI input and C/$\overline{D}$ input.
  Read-in is executed by the clock leading edge. Read-in operation is complete with 8 clocks. Inputting data during BUSY may cause malfunction.
  Valid if CS pin is at "H" level.

- SO (Serial Out)

  Serial output pin for reading-out BUSY/NON-BUSY and display data. "H"="1" and "L"="0". If CS pin is at "H" level and Serial Out Enable is set with the command, output is executed. Otherwise, this pin becomes high impedance.
  BUSY/NON-BUSY is output when CS pin is at "H" level. BUSY if "L" and NON-BUSY if "H". It goes BUSY after the 8th leading edge of $\overline{SHT}$, then goes NON-BUSY automatically after a specified time.
  Display data is output synchronously with the leading edge of $\overline{SHT}$.
  Input the "SOE/D" instruction to set this output to serial out enable or a high impedance state because the pin status is undefined after the power is applied.

- CS (Chip Select)

  Chip Select input pin.
  "Chip Select ON" if CS pin is at "H" level, and "Chip Select OFF" at "L" level. When "L" level is input, SO pin becomes open and $\overline{SHT}$ pin becomes equivalent to "H" level inside of the IC. Moreover, it prevents the input stages of SI, C/$\overline{D}$ and $\overline{SHT}$ pins from current flowing.

* For SI, C/$\overline{D}$, $\overline{SHT}$, SO, and CS, refer to "I/O Procedure".

- $\overline{RST}$

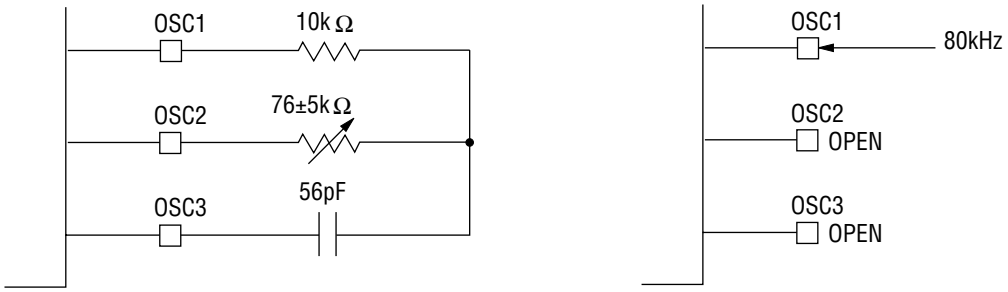
  Direct input reset input pin.
  By inputting "L" level pulse into $\overline{RST}$ pin, DISP, ABBC1/5, ABB, and BPC commands are set as D0="0". Before turning on the power, be sure to set $\overline{RST}$ pin at "L" level once. Setting this pin at "L" level during command execution may cause malfunction.

- 9D/$\overline{17D}$ (1/9Duty/$\overline{1/17Duty}$)

  Duty setting input pin.
  1/9 duty is set if this pin is at "H" level, and 1/17 duty at "L" level. Choice depends on the type of panel to be used.

If 1/9 duty is selected, common outputs C10 to C17 should be set open.

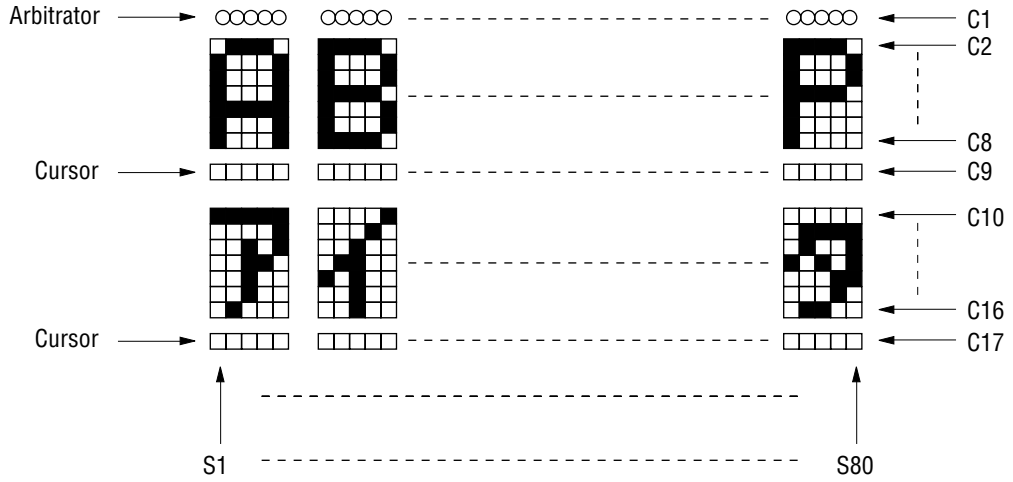
- TEST1, TEST2, TEST3
  Test signal input pins.
  The manufacturer uses these pins for testing.
  The user should connect this pin to GND or leave open.
- OSC1, OSC2, OSC3
  Pins used for 80kHz RC oscillation circuit formation and as external master clock input pin. Leave OSC2 and OSC3 open during input of external master clock.



[RC oscillation circuit formation] [External master clock input]

< Oscillation circuit wiring diagram >

- C1 - C17, S1 - S80 (Common 1 - 17, Segment 1 - 80)
  LCD output pins to be connected with the LCD panel. Turning into AC is made by frame inversion.
  Use the C1 to C9 pins during use at 1/9 duty, and leave the C10 to C17 pins open.
  →Refer to "Relationship between panel and LCD output".



<Relationship between panel and LCD output>

- V_{DD}, V_{SS}
  Supply voltage pins. V_{DD} should be set at "H" level.

V_{SS} is a GND pin. If the battery is used, V_{DD} is connected to the positive pin, and V_{SS} to the negative pin.

- V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SS5}
  LCD bias voltages input pins.

(EXAMPLE)

Case of 1/5 bias	($V_{BI}=V_{DD}-V_{SS5}$)	
Highest voltage :	V_{DD}	
	V_{SS1}	($V_{DD}-1/5\ V_{BI}$)
	V_{SS2}	($V_{DD}-2/5\ V_{BI}$)
	V_{SS3}	($V_{DD}-3/5\ V_{BI}$)
	V_{SS4}	($V_{DD}-4/5\ V_{BI}$)
Lowest voltage :	V_{SS5}	

Case of 1/4 bias	($V_{BI}=V_{DD}-V_{SS5}$)	
Highest voltage :	V_{DD}	
	V_{SS1}	($V_{DD}-1/4\ V_{BI}$)
	V_{SS2}, V_{SS3}	($V_{DD}-2/4\ V_{BI}$)
	V_{SS4}	($V_{DD}-3/4\ V_{BI}$)
Lowest voltage :	V_{SS5}	

List of Commands

X : Don't care

No.	Mnemonic	Operation	D								Comments
			7	6	5	4	3	2	1	0	
1	LPA	Load Pointer Address	1	1	A5	A4	A3	A2	A1	A0	Serial addresses 0 to 47
2	LOT	Load Option	1	0	1	1	X	X	I1	I0	Meanings for I1 and I0 are set as in the table below.
3	BKCG 1/0	Bank Change 1/0	1	0	0	X	0	0	0	1/0	Valid only when 1/9duty is selected. Switching between display addresses 0 to 15 and 16 to 31.
4	SOE/D	Serial Out Enable/Disable	1	0	0	X	0	1	1	1/0	Switching between output and high impedance of SO
5	DISP	Display on/off	1	0	0	X	1	0	0	1/0	Display ON if D0="1" Display OFF if D0="0" When at Display OFF, V_{DD} level voltage is output to all the COM and SEG pins.
6	ABBC 1/5	Arbitrator Blink Control 1/5 dot	1	0	0	1	1	1	0	1/0	Sets arbitrator blink in a 1dot unit or a 5dot unit. 1dot if D0="1", 5 dot if D0="0"
7	ABB	Arbitrator Blink	1	0	0	0	1	1	0	1/0	Data that is input via SI after setting D0="1", is set as data for arbitrator blink (1-dot unit). This is cancelled by D0="0"
8	AINC	Address Increment	1	0	0	X	1	X	1	X	Pointer address is incremented by 1.
9	CHB	Character Blink on/off	0	X	X	X	0	0	1/0	X	Controls blinking of characters and arbitrators (in 5 dots). Though arbitrator blink that is set as all-blank displayed is acceptable, blinking does not occur.
10	CSC	Cursor Control on/off	0	X	X	X	0	1	1/0	X	Turns cursor on or off.
11	CSB	Cursor Blink on/off	0	X	X	X	1	0	1/0	X	Controls blinking of cursor. But, though blinking setting with no cursor-on setting is acceptable, blinking does not occur.
12	CCB	Character & Cursor Blink on/off	0	X	X	X	1	1	1/0	X	CHB + CSB
13	BPC	Blink Pattern Control	1	0	0	X	0	0	1	1/0	Sets blink patterns of characters. (❑:chara.) if D0="1", (■:chara.) if D0="0"

Notes: 1. Entering commands number 1 to 7 and number 13 does not affect pointer address.
2. By entering commands number 8 to 12 or display code data, pointer address is automatically incremented by 1.
3. When Reset is entered, commands number 5 to 7 and number 13 are set to D0="0".

I1	I0	Operation
0	0	Operation is cancelled. (No operation)
0	1	Hereafter, equivalent to writing blank code at each AINC execution.
1	0	Hereafter, cursor-off and blink-cancellation are executed at each AINC execution.
1	1	Both of above two operations are indicated.

Command Description

[D7, D6, D5, D4, D3, D2, D1, D0], X=don't care

- LPA (Load Pointer Address)
  [1,1,A5,A4,A3,A2,A1,A0]
  The command sets "address" data into the address pointer to specify an address on which command execution affects and an address where display data is stored. The "address" is a number between 0H and 2FH, given by A0 through A5 in hexadecimal. When addresses 30H through 3FH are specified, display data and CHB, CSC, CSB, CCB commands become invalid through an address pointer is set up. Normally, the address pointer is a loop of 0H through 2FH.
- LOT (Load Option)
  [1,0,1,1,X,X,I1,I0]
  This command indicates some specific operation of display at the current address which is performed each time of AINC command execution.
  Operation is specified by bit I1 and I0 of the command.

I1	I0	Operation
0	0	Operation is cancelled. (No operation)
0	1	Hereafter, equivalent to writing blank code at each AINC execution.
1	0	Hereafter, Cursor-off and blink-cancellation are executed at each AINC execution.
1	1	Both of above two operations are indicated.

Note) When blink-cancellation is executed, all RAM data, which controls blinks for each bit of the arbitrator, go zeros.

- BKCG 1/0 (Bank Change 1/0)
  [1,0,0,X,0,0,0,1/0]
  Command used to do switching between display address groups (switching between BANKs), which is valid only when 1/9duty display is selected.
  When D0 is "0", display address range becomes 0 through 15, and 32 through 47.
  When D0 is "1", display address range becomes 16 through 31, and 32 through 47.
  Command execution and display data setting are not affected by Bank setting.
  The D0 status is not changed by Reset inputting. The D0 status is unknown when the system is powered on. So D0 must be set to "0" or "1" with the command.
- SOE/D (Serial Out Enable/Disable)
  [1,0,0,X,0,1,1,1/0]
  Command used to control the impedance of SO output pin.
  When D0 is "1", display data is output via SO pin. When D0 is "0", SO pin goes to high impedance.
  The D0 status is not changed by Reset inputting. The D0 status is unknown when the system is powered on. So D0 must be set to "0" or "1" with the command.

- DISP (Display on/off)
  [1,0,0,X,1,0,0,1/0]
  Command used to control lighing-on and lighting-off for the LCD panel.
  When D0 is "1", the display of the LCD panel goes on, and When D0 is "0", it goes off.
  When the display is off, the V_{DD} level voltage is output on all of pins of both the segment driver and the common driver.
  D0 is set to "0" after inputting Reset.

- ABBC 1/5 (Arbitrator Blink Control 1/5 dot)
  [1,0,0,1,1,1,0,1/0]
  Command used to do switching between arbitrator's blinking in a 1-dot unit and or in a 5-dot unit.
  When D0 is "1", arbitrator's blinking comes in the 1-dot unit mode.
  When D0 is "0", it comes in the 5-dot unit mode.
  D0="0" is set after inputting Reset.

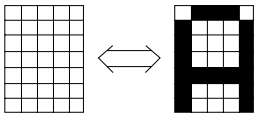
  Note) 1-dot unit blink setting → • See ABB.
  5-dot unit blink setting → • See CHB.

- ABB (Arbitrator Blink)
  [1,0,0,0,1,1,0,1/0]
  Command used to control on/off of blinking, which is valid only when arbitrator's blinking is set in the 1-dot unit mode.
  Data , which are entered via SI pin after setting D0="1", are taken as arbitrator blink data (1-dot unit).
  Input blink data correspond to each of arbitrator's dots. When "1", blinking is on, and when "0", blinking is off.
  Note that the arbitrator, which arbitrator-on is not specified, is not able to blink, though blink-setting is available. Dummy data must be entered into the arbitrator blink data D5 thru D7.
  It is impossible to write data in addressed 00H through 31H.
  D0="0" is set after inputting Reset.

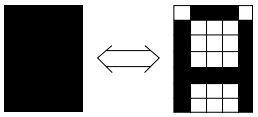
  Note) If blink is set in the 5-dot unit mode, ABB command setting (D0="1" or "0") is available, but blink-on/off setting via input of display data is impossible.

- AINC (Address Increment)
  [1,0,0,X,1,X,1,X]
  Command used to increment the value of the address pointer by 1.
  The pointer is increment by 1 each time this command is executed. The operation set by LOT command is given to the address before being increased by 1 each time this command is execution.

- CHB (Character Blink on/off)
  [0,X,X,X,0,0,1/0,X]
  Command used to control blinking of characters and arbitrator (5-dot unit).
  This command is executed to the address indicated by the address pointer. Blinking is on by setting D1="1", and off by setting D1="0".
  For blinking of characters, all lighting-on or all lighting-off, and characters-displaying are repeated.
  Choosing between all lighting-on and all lighting-off is controlled by BPC command.
  For arbitrator, only lighting bits repeat lighting-off or lighting-off. The blink control or arbitrator is valid only when ABBC1/5="0" and in the 5-dot unit mode.
  Refer to "BPC".
- CSC (Cursor Control on/off)
  [0,X,X,X,0,1,1/0,X]
  Command used to control lighting-on and lighting-off of cursor.
  This command is executed to the address indicated by the address pointer.The cursor is lighting on by setting D1="1", and lighting off by setting D1="0".
- CSB (Cursor Blink on/off)
  [0,X,X,X,0,1,1/0,X]
  Command used to control blinking of cursor.
  This command is executed to the address indicated by the address pointer. Blinking is on by setting D1="1", and off by setting D1="0".
  The blinking in the address, where cursor-lighting-on is not specified, does not occur, though the command of blinking is acceptable. Blinking starts by specifying cursor-lighting-on.
- CCB (Character & Cursor Blink on/off)
  [0,X,X,X,1,1,1/0,X]
  Command used to execute both CHB command and CSB command.
- BPC (Blink Pattern Control)
  [1,0,0,X,0,0,1,1/0]
  Command used to control blink patterns of characters.
  When D0="1" is set, all lighting-off (35 dots) and characters-displaying are repeated.
  When D0="0" is set, all lighting-on (35 dots) and characters-displaying are repeated.
  When D0="1" is set, if characters are blank, their blinkings do not occur in appearance.
  When D0="0" is set, if characters are in all lighting-on, their blinkings do not occur in appearance.
  D0 is set to "0" affer inputting Reset.



[D0 = "1"]

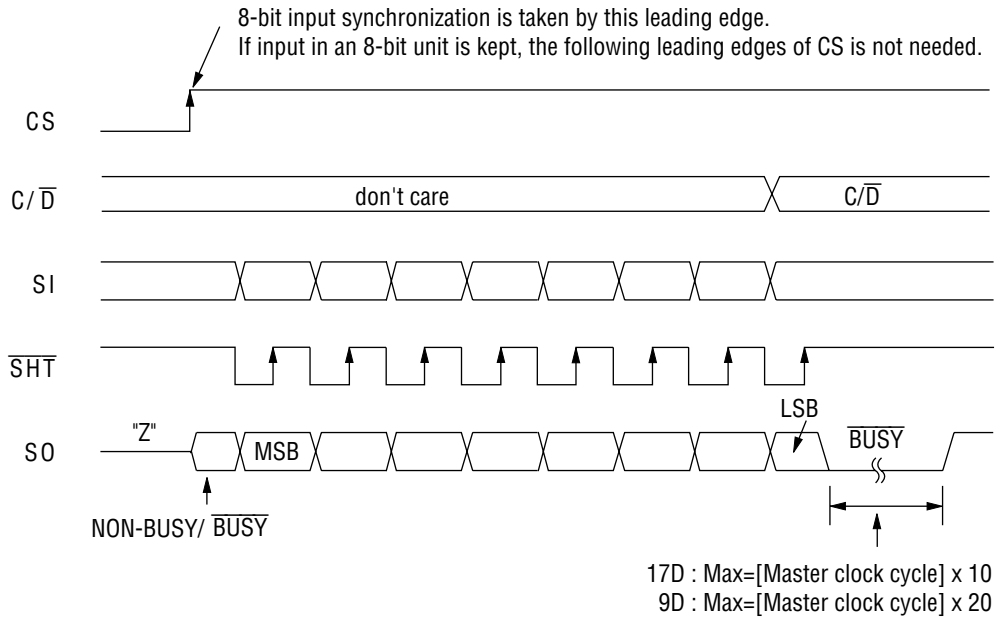


[D0 = "0"]

- Increment (+1) in address pointer
  When display data or arbitrator data (1-dot unit) is entered or when the following commands are executed, the address pointer is incremented by 1.
  AINC, CHB, CSC, CSB and CCB.

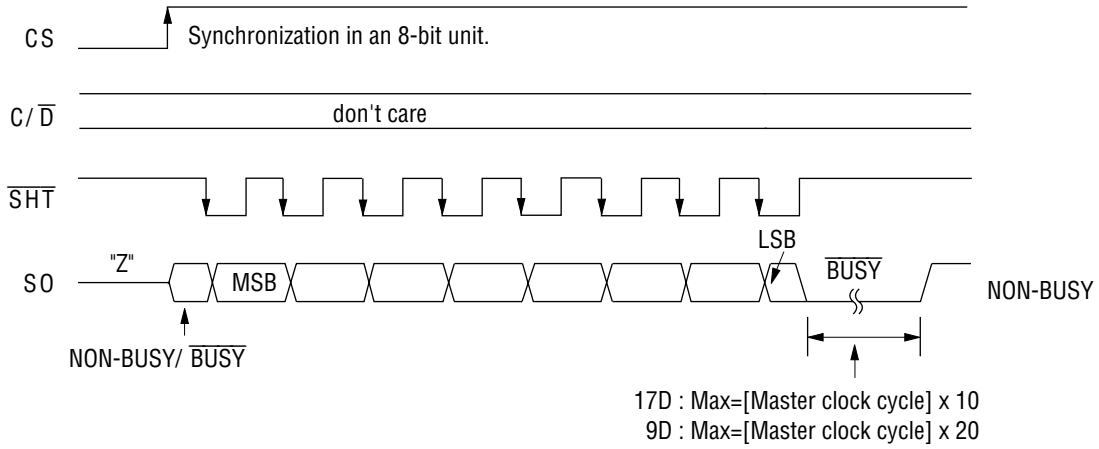
I/O Procedure

- Input timing (command input, display data input)



- Output timing (display code data output)

  Code data or arbitrator data indicated by the address pointer is always output, provided that the SOE command has already been input.



Note) If CS is set at "L" level when 8-bit read-out is not complete, and CS is set at "H" level again, then read-out operation is executed, uncomplete data will be output continually and the remaining read-out data will be zero.

Method of Calculating Various Types of Frequencies

- Original Clock Frequency and Blink Frequency

  Blink cycle calculation

  ([Original clock cycle] x 5) x 2^{14} = Blink cycle ..... Formula 1

  From formula 1, the blink frequency can be calculated.

  Example) When the original clock is 80kHz:

  Clock cycle Ts=12.5 [µs]

  From formula 1,

  Blink cycle Tb=(12.5 x 10^{-6} x 5) x 2^{14} = 1.024 [s]

  Thus,

  Blink frequency ≒ 1 [Hz]

- Original Clock Frequency and Frame Frequency

  Frame cycle calculation

  1/9 DUTY: (Original clock cycle) x 1152 = Frame cycle ..... Formula 2

  1/17 DUTY: (Original clock cycle) x 1088 = Frame cycle ..... Formula 3

  From formulas 2 and 3, the frame frequency can be calculated.

  Example) In the original clock 80kHz and 1/17 DUTY specifications:

  Clock cycle Ts=12.5 [µs]

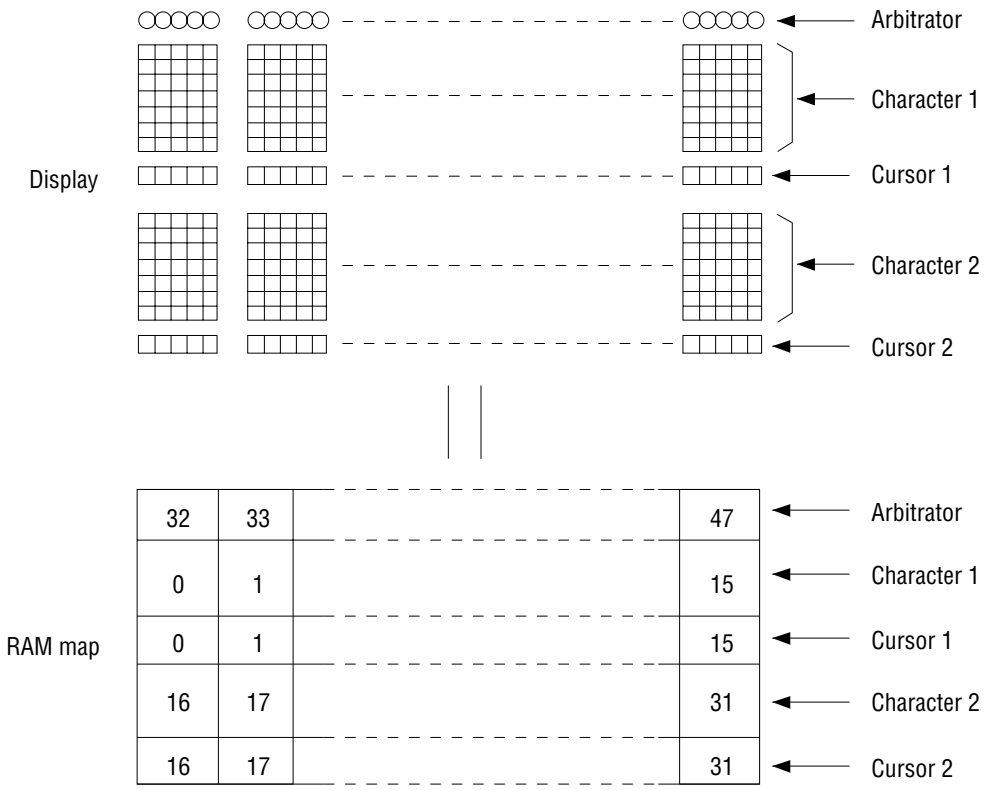
  From formula 3,

  Frame cycle Tf=12.5 x 10^{-6} x 1088 = 13.6 [ms]

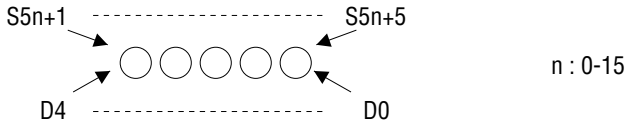
  Thus,

  Frame frequency ≒ 73.5 [Hz]

Display and Memory Address

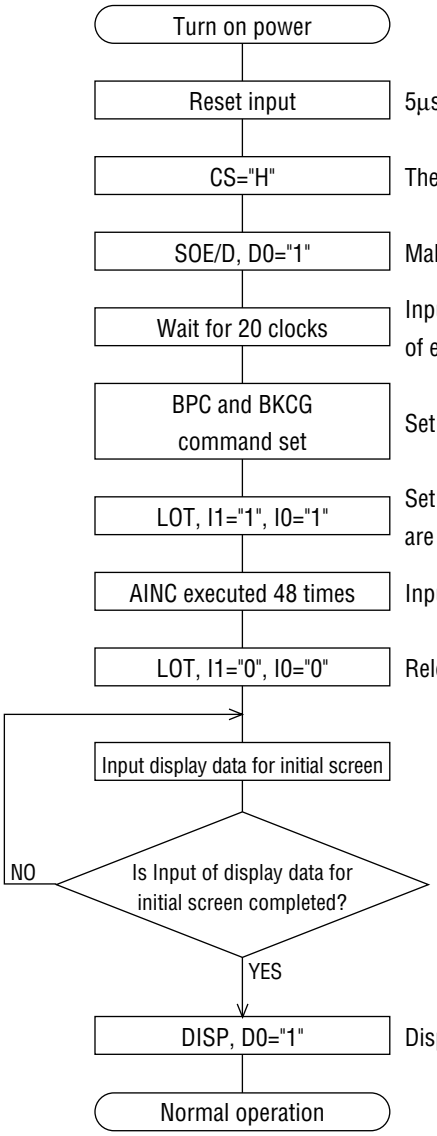


Note Characters are entered with codes.
Arbitrator is displayed with no CG ROM. The relationship between input data and display is shown below.



Dummy input is required for serial data D7 through D5.
Either "1" or "0" is available for data to be input into D7 through D5.

Flowchart for Power-On Timing



5μs required; external reset input or power-on reset input

The device is enabled.

Make the SO output enable, to perform busy detection.

Input a wait for the SOE/D command processing. (For the processing of each command after this, perform busy detection. *1)

Set the blink pattern and bank change mode.

Set the Load Option. (Blank-code writing and blink-cancellation are executed each time the AINC command is executed.)

Input the AINC command to clear the RAM data.

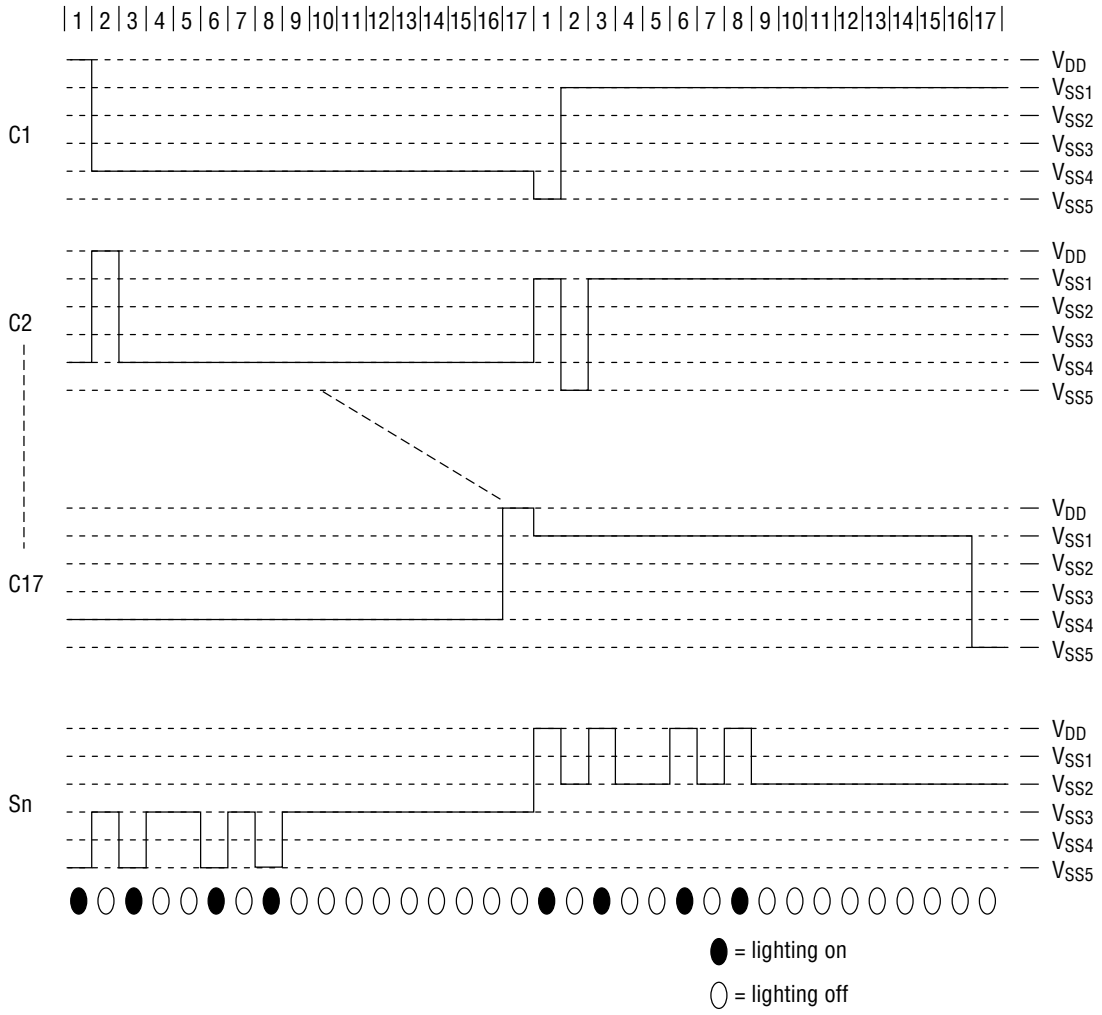
Release the Load Option.

Display is turned on and the initial screen is displayed.

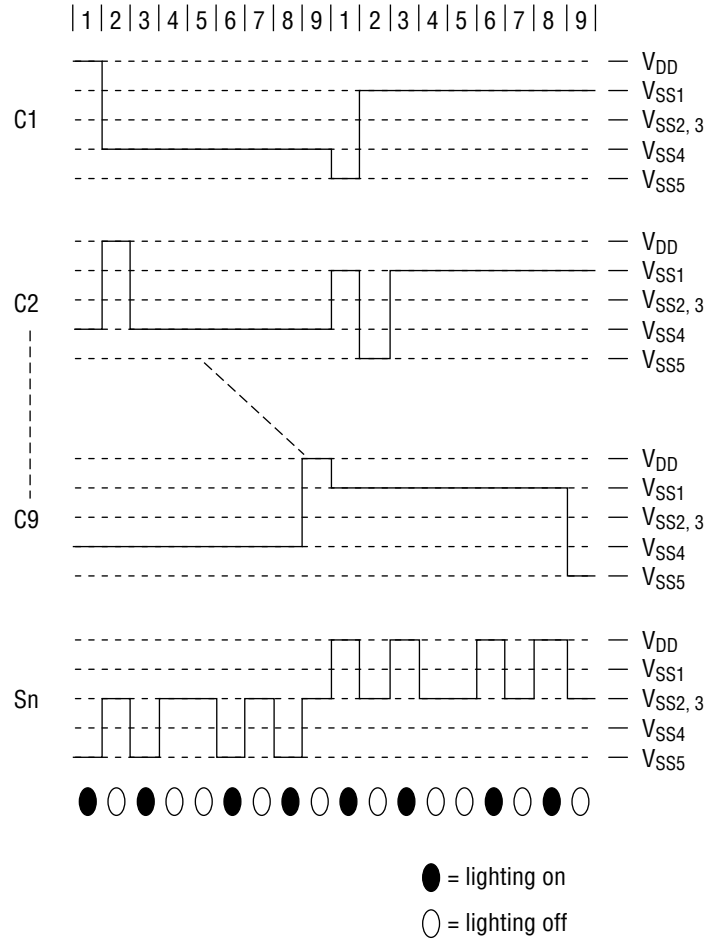
*1 After the required commands and display data are entered, perform busy detection based on the SO pin status. When it is confirmed that the status has been changed from BUSY (SO="L") to NON-BUSY (SO="H"), enter the next data.
If busy detection is not performed, wait for 10 master oscillation clocks when used at 1/17 duty or for 20 master oscillation clocks when at 1/9 duty, then enter the next data.

Waveforms Applied to LCD

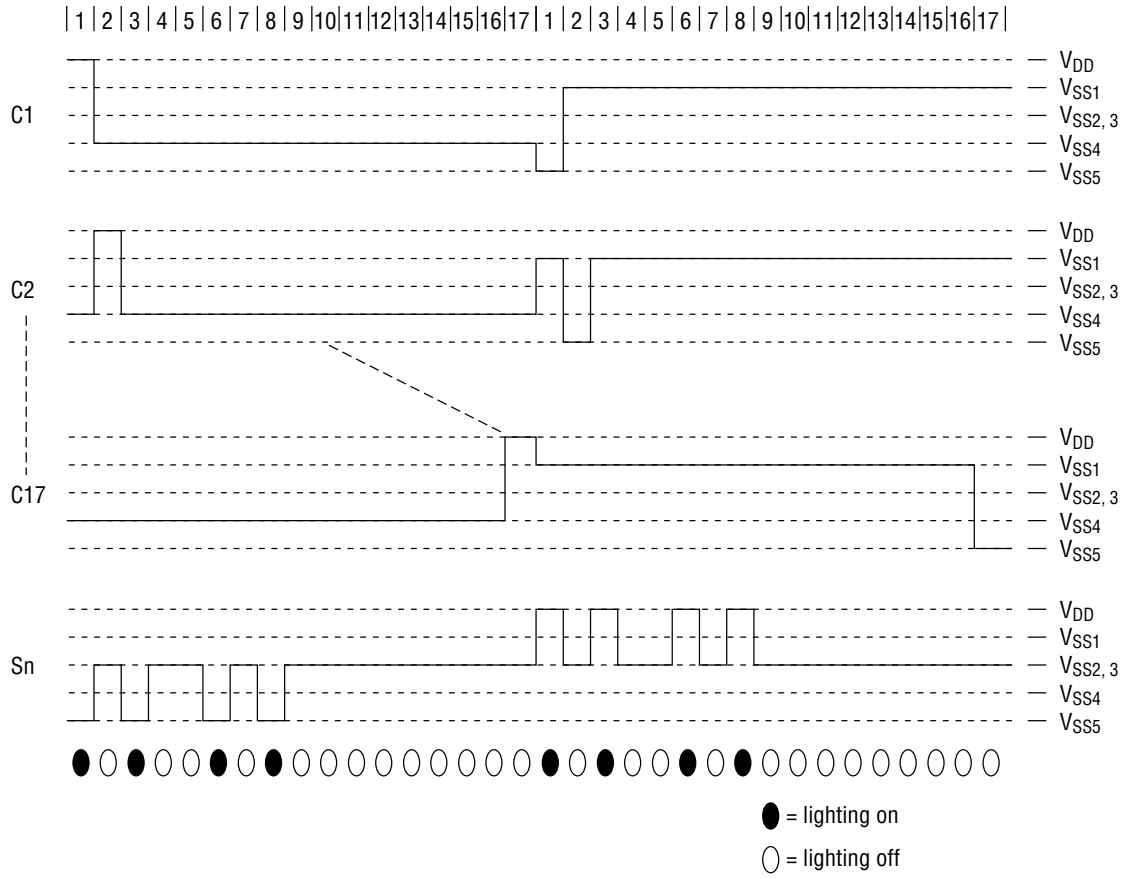
1/17 duty (1/5 bias)



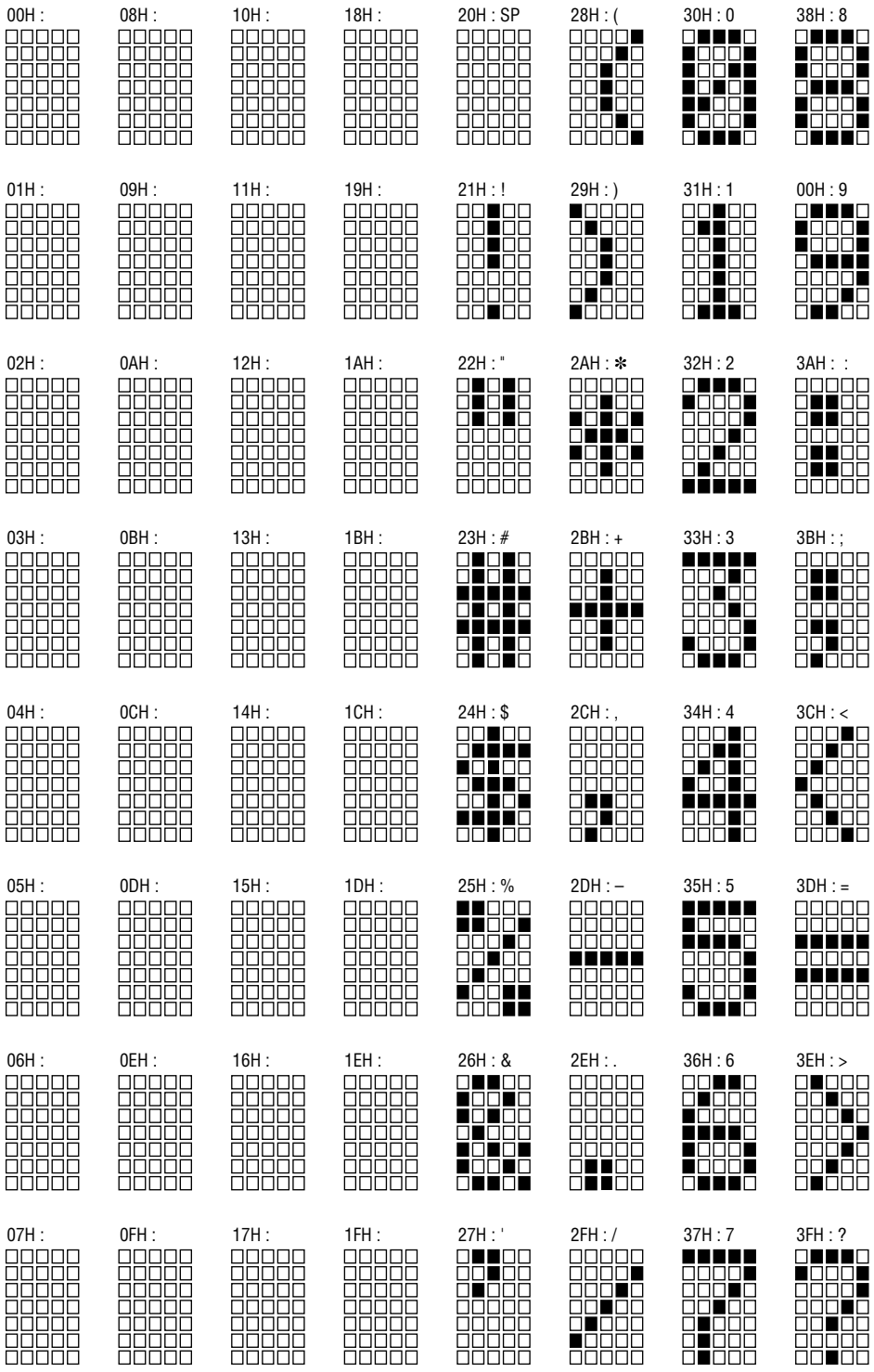
1/9 duty (1/4 bias)



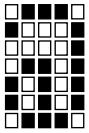
1/17 duty (1/4 bias)



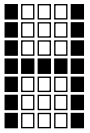
Codes and Character Fonts of Code -01



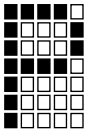
40H : @



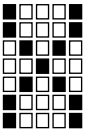
48H : H



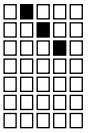
50H : P



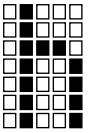
58H : X



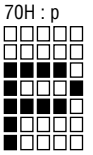
60H : `



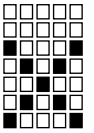
68H : h



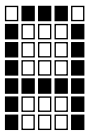
70H : p



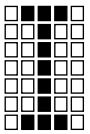
78H : x



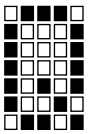
41H : A



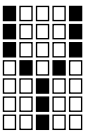
49H : I



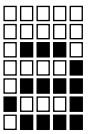
51H : Q



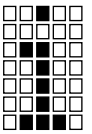
59H : Y



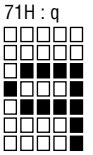
61H : a



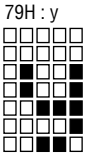
69H : i



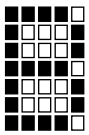
71H : q



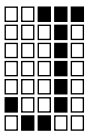
79H : y



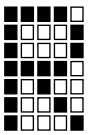
42H : B



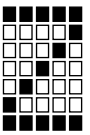
4AH : J



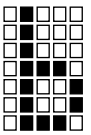
52H : R



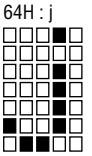
5AH : Z



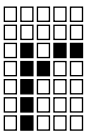
62H : b



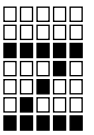
64H : j



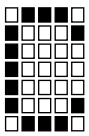
72H : r



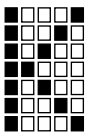
7AH : z



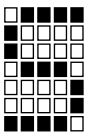
43H : C



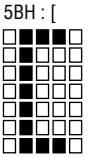
4BH : K



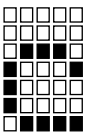
53H : S



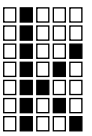
5BH : [



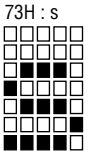
63H : c



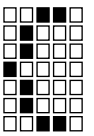
6BH : k



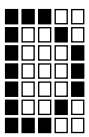
73H : s



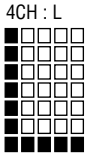
7BH : {



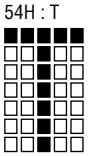
44H : D



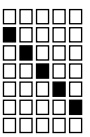
4CH : L



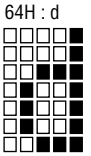
54H : T



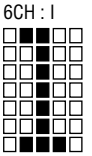
5CH : \



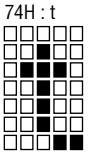
64H : d



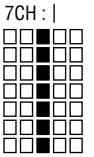
6CH : l



74H : t



7CH : |



45H : E

4DH : M

55H : U

5DH :]

65H : e

6DH : m

75H : u

70H : }

46H : F

4EH : N

56H : V

5EH : ^

66H : f

6EH : n

76H : v

7EH : ~

47H : G

4FH : O

57H : W

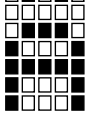
5FH : _

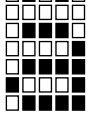
67H : g

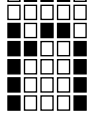
6FH : o

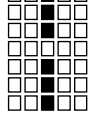
77H : w

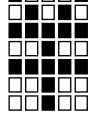
7FH : £

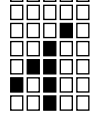
8ØH : Ä


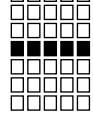
88H : ä


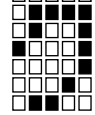
9ØH : n̄


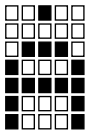
98H : ¦


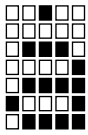
AOH : ¥


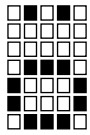
A8H : ｨ


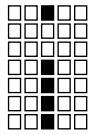
BOH : —


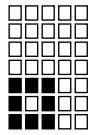
B8H : ｸ


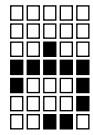
81H : Å


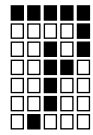
89H : å


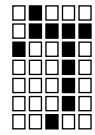
91H : ö


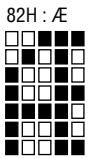
99H : ¡


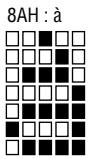
A1H : 。


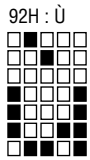
49H : ｳ


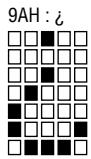
B1H : ｱ


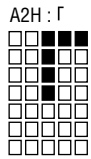
B9H : ｹ


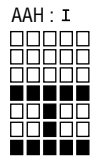
82H : Æ


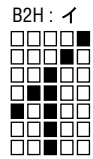
8AH : à


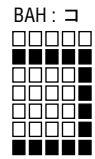
92H : Ù


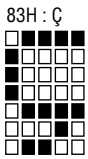
9AH : ¿


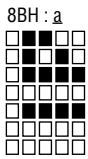
A2H : 「


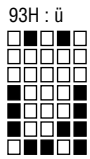
AAH : ｪ


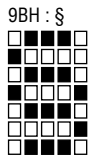
B2H : ｲ


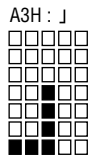
BAH : ｺ


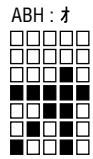
83H : Ç


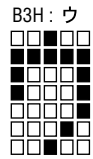
8BH : a̲


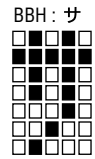
93H : ü


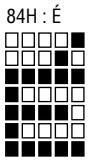
9BH : §


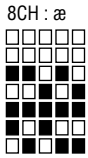
A3H : 」


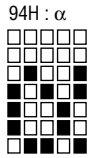
ABH : ｫ


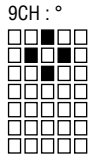
B3H : ｳ


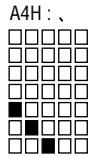
BBH : ｻ


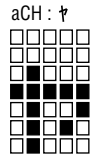
84H : É


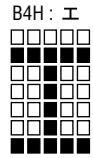
8CH : æ


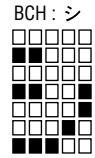
94H : α


9CH : °


A4H : 、


aCH : ｬ


B4H : ｴ


BCH : ｼ


85H : Ń

8DH : ç

95H : β

9DH : ¨

A5H : ・

ADH : ｭ

B5H : ｵ

BDH : ｽ

86H : Ö

8EH : é

96H : Ø

9EH : º

A6H : ヲ

AEH : ｮ

B6H : カ

BEH : セ

87H : Ü

8FH : è

97H : ø

9FH : ¢

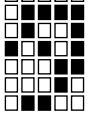
27H : ア

2FH : ｯ

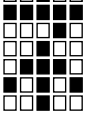
37H : キ

3FH : ソ

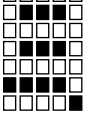
C0H : タ



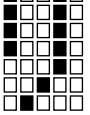
C8H : ネ



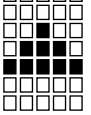
D0H : ミ



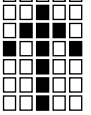
D8H : リ



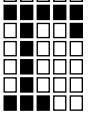
E0H : ▲



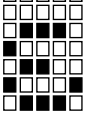
E8H : ↑



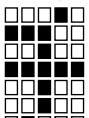
F0H : Γ



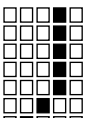
F8H : ε



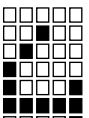
C1H : チ



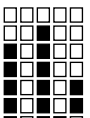
C9H : ノ



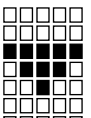
D1H : ム



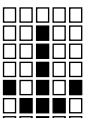
D9H : ル



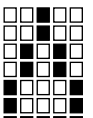
E1H : ▼



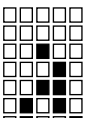
E9H : ↓



F1H : △



F9H : λ



C2H : ツ

CAH : ハ

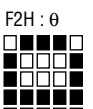
D2H : メ

DAH : レ

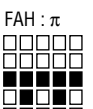
E2H : 千

EAH : 月

F2H : θ



FAH : π



C3H : テ

CBH : ヒ

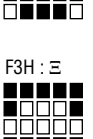
D3H : モ

DBH : ロ

E3H : 万

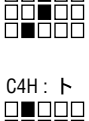
EBH : 日

F3H : Ξ

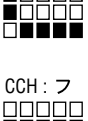


FBH : σ

C4H : ト



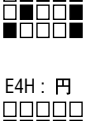
CCH : フ



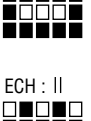
D4H : ヤ

DCH : ワ

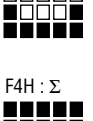
E4H : 円



ECH : ॥



F4H : Σ



FCH : ü

C5H : ナ

CDH : ベ

D5H : ユ

DDH : ン

E5H : 〒

EDH : Ⅲ

F5H : Φ

FDH :

C6H : ニ

CEH : ホ

D6H : ヨ

DEH : ゛

E6H : →

EEH : ≡

FEH : Ψ

FEH :

C7H : ヌ

CFH : マ

D7H : ラ

DFH : °

E7H : ←

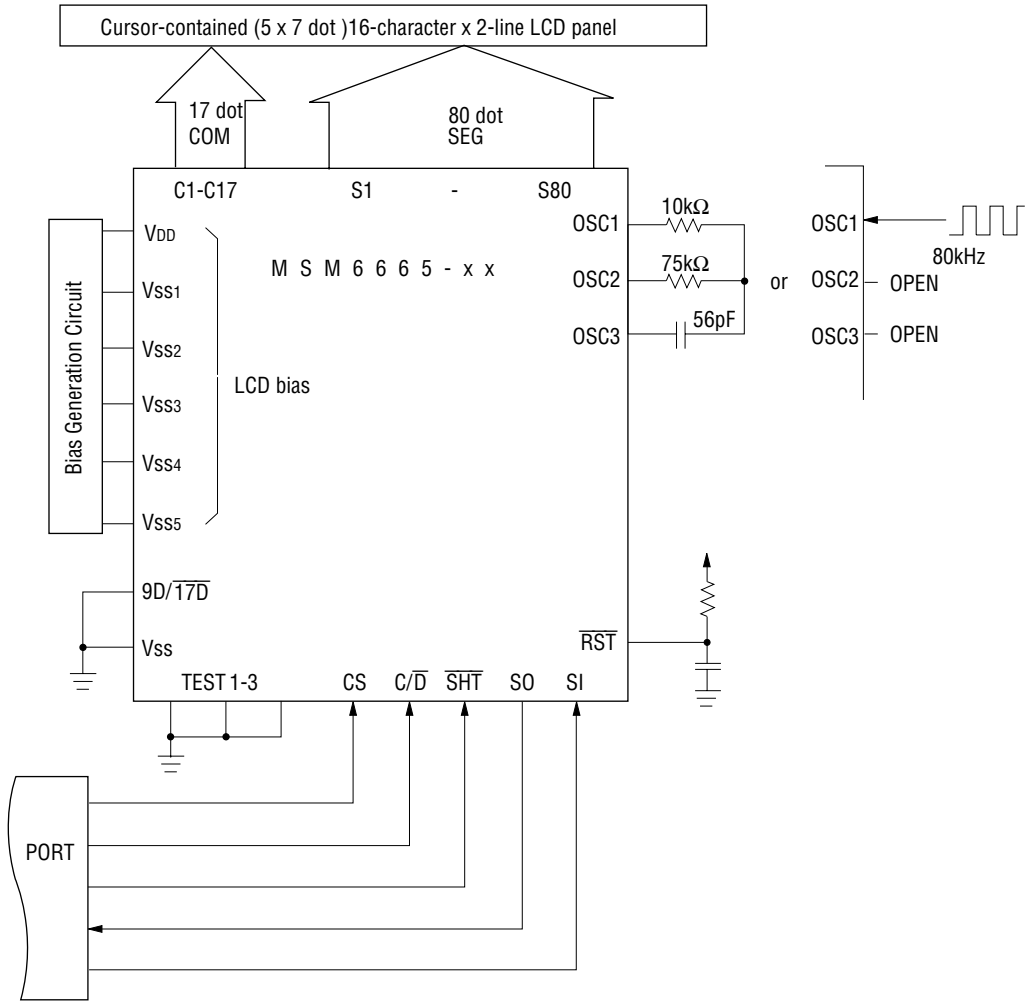
EFH : ≡

F7H : Ω

FFH : ■

APPLICATION CIRCUIT

Example : 1/17 duty, 1/5 bias

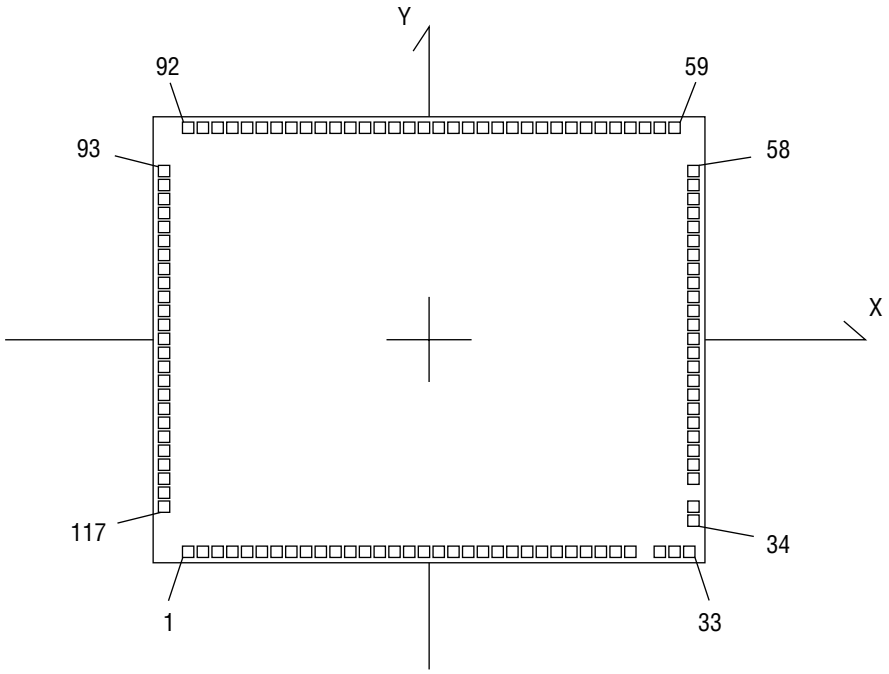


PAD CONFIGURATION

Pad layout

Chip size : 6.05 × 4.98mm

Passivation film etched hole : 110 × 110μm



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)
1	C15	–2486	–2332
2	C14	–2336	–2332
3	C13	–2186	–2332
4	C12	–2036	–2332
5	C11	–1886	–2332
6	C10	–1736	–2332
7	C9	–1586	–2332
8	C8	–1436	–2332
9	C7	–1286	–2332
10	C6	–1136	–2332
11	C5	–986	–2332
12	C4	–836	–2332
13	C3	–686	–2332
14	C2	–536	–2332
15	C1	–386	–2332
16	V_{SS}	–227	–2332
17	V_{SS5}	–67	–2332
18	V_{SS4}	83	–2332
19	V_{SS3}	233	–2332
20	V_{SS2}	383	–2332

Pad No.	Pad Name	X (μm)	Y (μm)
21	V_{SS1}	533	–2332
22	CS	683	–2332
23	C/$\overline{D}$	833	–2332
24	SI	983	–2332
25	$\overline{SHT}$	1133	–2332
26	9D/$\overline{17D}$	1283	–2332
27	$\overline{RST}$	1433	–2332
28	SO	1583	–2332
29	V_{DD}	1733	–2332
30	OSC1	1891	–2332
31	OSC2	2308	–2332
32	OSC3	2789	–2332
33	TEST1	2659	–2332
34	TEST2	2870	–1797
35	TEST3	2870	–1647
36	S80	2870	–1347
37	S79	2870	–1197
38	S78	2870	–1047
39	S77	2870	–897
40	S76	2870	–747

Pad No.	Pad Name	X (μm)	Y (μm)
41	S75	2870	–567
42	S74	2870	–447
43	S73	2870	–297
44	S72	2870	–147
45	S71	2870	3
46	S70	2870	153
47	S69	2870	303
48	S68	2870	453
49	S67	2870	603
50	S66	2870	753
51	S65	2870	903
52	S64	2870	1053
53	S63	2870	1203
54	S62	2870	1353
55	S61	2870	1503
56	S60	2870	1653
57	S59	2870	1803
58	S58	2870	1953
59	S57	2482	2332
60	S56	2332	2332
61	S55	2182	2332
62	S54	2032	2332
63	S53	1882	2332
64	S52	1732	2332
65	S51	1582	2332
66	S50	1432	2332
67	S49	1282	2332
68	S48	1132	2332
69	S47	982	2332
70	S46	832	2332
71	S45	682	2332
72	S44	532	2332
73	S43	382	2332
74	S42	232	2332
75	S41	82	2332
76	S40	–68	2332
77	S39	–218	2332
78	S38	–368	2332
79	S37	–518	2332
80	S36	–668	2332

Pad No.	Pad Name	X (μm)	Y (μm)
81	S35	–818	2332
82	S34	–968	2332
83	S33	–1118	2332
84	S32	–1268	2332
85	S31	–1418	2332
86	S30	–1568	2332
87	S29	–1718	2332
88	S28	–1868	2332
89	S27	–2018	2332
90	S26	–2168	2332
91	S25	–2318	2332
92	S24	–2468	2332
93	S23	–2870	1803
94	S22	–2870	1653
95	S21	–2870	1503
96	S20	–2870	1353
97	S19	–2870	1203
98	S18	–2870	1053
99	S17	–2870	903
100	S16	–2870	753
101	S15	–2870	603
102	S14	–2870	453
103	S13	–2870	303
104	S12	–2870	153
105	S11	–2870	3
106	S10	–2870	–147
107	S9	–2870	–297
108	S8	–2870	–447
109	S7	–2870	–597
110	S6	–2870	–747
111	S5	–2870	–897
112	S4	–2870	–1047
113	S3	–2870	–1197
114	S2	–2870	–1347
115	S1	–2870	–1497
116	C17	–2870	–1647
117	C16	–2870	–1797

Pin and Pad Correspondence

The symbol for each chip pad and package pin is equal, but the numbers for each pad and pin are not equal.

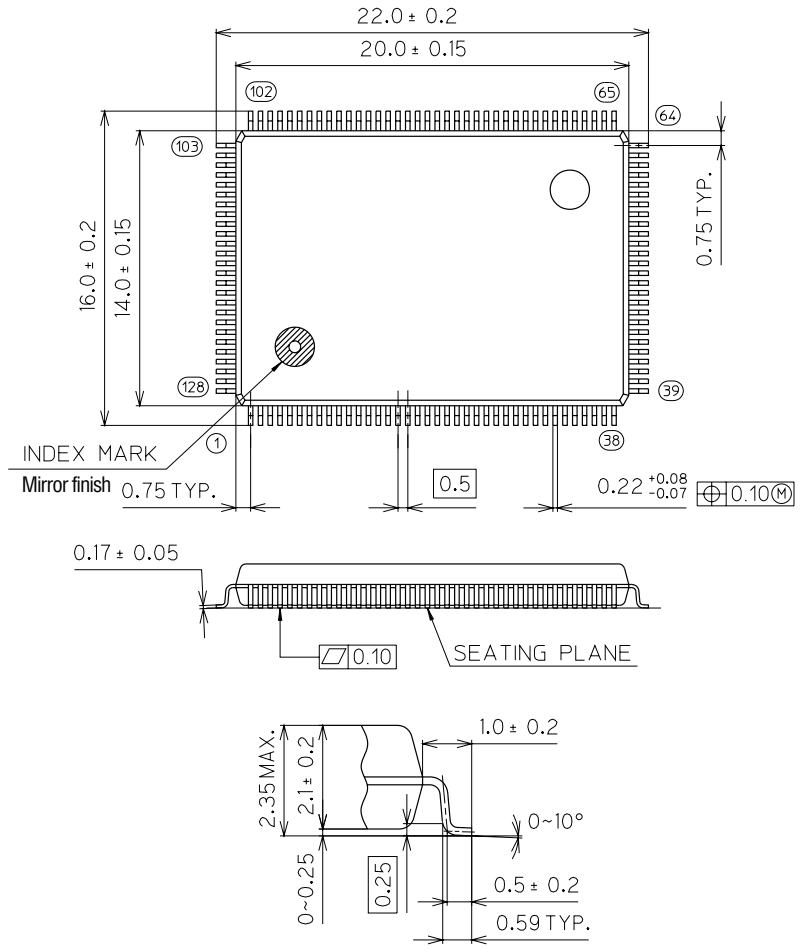
If both chips and packaged devices are used, the number for each chip pad should be corresponded to the number for each package pin according to each symbol listed in the table below.

Symbol	Chip Pad	Package Pin	Symbol	Chip Pad	Package Pin	Symbol	Chip Pad	Package Pin	Symbol	Chip Pad	Package Pin
C15	1	65	OSC2	31	100	S55	61	3	S25	91	37
C14	2	66	OSC3	32	101	S54	62	4	S24	92	38
C13	3	67	TEST1	33	102	S53	63	5	S23	93	39
C12	4	68	TEST2	34	103	S52	64	6	S22	94	40
C11	5	69	TEST3	35	104	S51	65	7	S21	95	41
C10	6	70	S80	36	106	S50	66	8	S20	96	42
C9	7	71	S79	37	107	S49	67	9	S19	97	43
C8	8	72	S78	38	108	S48	68	10	S18	98	44
C7	9	73	S77	39	109	S47	69	11	S17	99	45
C6	10	74	S76	40	110	S46	70	12	S16	100	46
C5	11	75	S75	41	111	S45	71	14	S15	101	47
C4	12	76	S74	42	112	S44	72	15	S14	102	48
C3	13	78	S73	43	113	S43	73	17	S13	103	49
C2	14	79	S72	44	114	S42	74	18	S12	104	50
C1	15	81	S71	45	115	S41	75	19	S11	105	51
V_{SS}(GND)	16	82	S70	46	116	S40	76	20	S10	106	52
V_{SS5}	17	83	S69	47	117	S39	77	21	S9	107	53
V_{SS4}	18	84	S68	48	118	S38	78	22	S8	108	54
V_{SS3}	19	85	S67	49	119	S37	79	24	S7	109	55
V_{SS2}	20	86	S66	50	120	S36	80	25	S6	110	56
V_{SS1}	21	88	S65	51	121	S35	81	27	S5	111	57
CS	22	89	S64	52	122	S34	82	28	S4	112	58
C/$\overline{D}$	23	91	S63	53	123	S33	83	29	S3	113	59
SI	24	92	S62	54	124	S32	84	30	S2	114	60
$\overline{SHT}$	25	93	S61	55	125	S31	85	31	S1	115	61
9D/$\overline{17D}$	26	94	S60	56	126	S30	86	32	C17	116	62
$\overline{RST}$	27	95	S59	57	127	S29	87	33	C16	117	63
SO	28	96	S58	58	128	S28	88	34	–	–	–
V_{DD}	29	97	S57	59	1	S27	89	35	–	–	–
OSC1	30	98	S56	60	2	S26	90	36	–	–	–

PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).