



PCF87852

Bluetooth baseband controller

Rev. 01 — 23 April 2004

Preliminary data

1. General description

The PCF87852 combines the Bluetooth™ protocol stack, Link Controller (LC), Link Manager (LM), and Host Controller Interface (HCI) firmware of the Bluetooth system specification in a single IC with embedded software. Together with an RF module, a few external components and an antenna it forms a Bluetooth system. In most cases this module will be attached to a host, for example a GSM baseband controller or a PC processor. The PCF87852 may also be used for embedded Bluetooth applications by running the upper software layers also from the on-chip memory. Together with an external voice codec a Bluetooth headset application can be realized.

The industry standard ARM7TDMI™ microcontroller with low power consumption is integrated together with ROM memory and SRAM. There are no provisions for external controllers to directly access on-chip data memory. Communication with an external host, for example a PC, GSM or PDA, is handled via the HCI.

Industry standard interfaces such as I²C-bus™, PCM and IOM® are supported by on-chip hardware. Additionally, a UART interface is available that can be used as the Bluetooth host controller interface.

The Bluetooth controller consists of a number of functional blocks that operate under control of the embedded microcontroller. The microcontroller has access to these blocks via the AMBA System Bus (ASB) and the VLSI Peripheral Bus (VPB).

The PCF87852 is designed to be used together with an RF IC as low-cost, low-power, radio-based cable replacement or wireless link. This link will be the basis for PCs, telephones, PDAs and peripherals to communicate together on an ad-hoc basis. It will replace cables and enables a wireless personal network.

The PCF87852 is especially suited for applications without the need for analog voice input or output, e.g. cellular telephones or computing platforms.

2. Features

2.1 Baseband hardware

- Embedded ARM7TDMI microprocessor
- 224 kbytes ROM memory
- 38 kbytes SRAM memory
- 8 kbytes internal data RAM (IRAM) for Bluetooth controller
- Watchdog timer
- Two 32-bit system timers



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- Bluetooth controller including scrambling, CRC generation and checking, FEC encoding and decoding and ciphering according to the “*Specification of the Bluetooth System, Version 1.1*”
- Bluetooth connections supporting:
 - ◆ Maximum 3 active connections (ACL)
 - ◆ One voice connection (SCO).
- CVSD transcoder
- RF interface
- RSSI measurement
- On-chip 1.8 V voltage regulator
- 8-bit D/A and A/D conversion for various purposes; e.g. PA control
- Power-on reset
- System clock crystal oscillator
- Low-power crystal oscillator for a low-frequency clock input
- System clock request signal for control of external clock source
- Microprocessor interfaces including UART, I²C-bus, combined PCM/IOM and general purpose I/O-pins
- Patch mechanism for code updates and corrections.

2.2 Firmware

- Interface drivers
- Bluetooth controller driver
- Link Controller (LC)
- Link Manager (LM)
- Host Controller Interface (HCI)
- L2CAP, RFCOMM and SDP
- Small profiles and application software (i.e Bluetooth headset).

2.3 General

- Core and interface supply: 1.8 V; RF interface supply: 2.7 V to 3.4 V
- Operating temperature range: –40 °C to +85 °C
- Package: LFBGA73 (7 × 7 mm² and 0.5 mm pitch).

3. Applications

- Cell phones and smart phones
- Computing applications (PC, notebook and PDA)
- Cellular accessories (Bluetooth headsets).

4. Quick reference data

Table 1: Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|--------------------|-----------------|-----------------|---------|
| Supplies | | | | | | |
| V_{SS} | ground voltage | | [1] - | 0 | - | V |
| V_{DDCO1} | first core supply voltage | | [2] 1.65 | 1.8 | 1.95 | V |
| V_{DDCO2} | second core supply voltage | | [2] 1.65 | 1.8 | 1.95 | V |
| V_{DDIORF} | RF interface supply voltage | | [2][3][4] 1.65 | 3.0 | 3.6 | V |
| V_{DDIO18} | 1.8 V I/O supply voltage | | [2] 1.65 | 1.8 | 1.95 | V |
| V_{DDIOV} | variable I/O supply voltage | | [2] 1.65 | 3.0 | 3.6 | V |
| V_{DDA} | analog supply voltage | | [2] 1.65 | 1.8 | 1.95 | V |
| V_{DDO} | oscillator supply voltage | | [2][5] 1.65 | 1.8 | 1.95 | V |
| Power consumption^[6] | | | | | | |
| $I_{DD(on)}$ | operating supply current for an active ACL link and continuous DM1 and DH1 mode | $I_{DD} = I_{DDC} + I_{DDA}$; ARM active; $V_{DDC} = V_{DDA} = 1.8$ V | - | 13 | - | mA |
| $I_{DDIORF(tx)}$ | RF interface supply current in transmit mode | $V_{DDIORF} = 3.0$ V | - | 125 | - | μ A |
| $I_{DD(lp)}$ | low-power supply current in low power mode | $I_{DD} = I_{DDC} + I_{DDA}$; ARM off; DCXO off; LPO on (32.768 kHz) | - | 40 | - | μ A |
| $I_{DD(off)}$ | off mode supply current for lowest possible current | $I_{DD} = I_{DDC} + I_{DDA}$; ARM off; clocks off | [7] - | 30 | - | μ A |
| Digital I/O pins | | | | | | |
| I/O pins at V_{DDIORF} | | | | | | |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | V_{DDIORF} | V |
| V_{IL} | LOW-level input voltage | | 0 | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = 4$ mA | $V_{DDIORF} - 0.4$ | - | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 4$ mA | - | - | 0.4 | V |
| I/O pins at V_{DDIO18} | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDIO18}$ | - | V_{DDIO18} | V |
| V_{IL} | LOW-level input voltage | | 0 | - | $0.3V_{DDIO18}$ | V |
| V_{hys} | hysteresis voltage | | - | $0.3V_{DDIO18}$ | - | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = 4$ mA | $V_{DDIO18} - 0.4$ | - | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 4$ mA | - | - | 0.4 | V |
| I/O pins at V_{DDIOV} | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDIOV}$ | - | V_{DDIOV} | V |
| V_{IL} | LOW-level input voltage | | 0 | - | $0.3V_{DDIOV}$ | V |
| V_{hys} | hysteresis voltage | | - | $0.3V_{DDIOV}$ | - | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = 3$ mA | $V_{DDIOV} - 0.4$ | - | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 3$ mA | - | - | 0.4 | V |

[1] Applies to all 0 V ground reference pins: V_{SSIORF} , V_{SSCO1} , V_{SSCO2} , V_{SSIO18} , V_{SSIOV} , V_{SSA} and V_{SSO} .

[2] It must be insured that the supply rise on each of the supply pins from 0 V to 1.1 V is shorter than 5 ms.

- [3] V_{DDIORF} is only tested at 2.7 V to 3.4 V.
- [4] $V_{DDIORF} = V_{DDIOV}$.
- [5] I²C-bus is only functional for voltages between 3.0 V and 3.6 V.
- [6] The power consumptions are very dependent on the software settings and can vary a lot.
- [7] CMOS leakage current. All blocks are disabled except the bias currents of the band gap reference and the power-on reset circuit.

Table 2: Typical power consumption figures of the PCF87852 in combination with BGB101 radio module

| Symbol ^[1] | Domain | Typ | Unit |
|---|------------|-------|------|
| SCO and HV3 packet | [2] 1.80 V | 13.0 | mA |
| | 2.85 V | 12.0 | mA |
| | total P | 57.6 | mW |
| ACL, DM1 or DH1 packets and bidirectional data | [2] 1.80 P | 12.6 | mA |
| | 2.85 V | 10.0 | mA |
| | total P | 51.2 | mW |
| ACL, DM5 or DH5 packet transmit and NULL packet receive | [2] 1.80 V | 12.6 | mA |
| | 2.85 V | 26.0 | mA |
| | total P | 96.8 | mW |
| ACL, DM5 or DH5 packet receive and NULL packet transmit | [2] 1.80 V | 12.6 | mA |
| | 2.85 V | 32.0 | mA |
| | total P | 113.9 | mW |
| ACL, sniff mode and external 32 kHz ($T_{sniff} = 500$ ms) | [3] 1.80 V | 0.32 | mA |
| | 2.85 V | 0.40 | mA |
| | total P | 1.71 | mW |
| ACL, sniff mode and internal 32 kHz ($T_{sniff} = 500$ ms) | [4] 1.80 V | 0.65 | mA |
| | 2.85 V | 0.40 | mA |
| | total P | 2.31 | mW |
| Low power page/inquiry scan and external 32 kHz | [3] 1.80 V | 0.23 | mA |
| | 2.85 V | 0.42 | mA |
| | total P | 1.61 | mW |
| Low power page/inquiry scan and internal 32 kHz | [4] 1.80 V | 0.55 | mA |
| | 2.85 V | 0.42 | mA |
| | total P | 2.19 | mW |

- [1] All measurements performed on sampling basis with HCI firmware loaded in the PCF87852 internal ROM.
- [2] Measurements are done with the 13 MHz oscillator in slave mode.
- [3] Measurements are done with a 32.768 kHz crystal connected to generate the Bluetooth low power clock.
- [4] Measurements are done with a 13 MHz crystal connected and the Bluetooth low power clock derived from the 13 MHz.

5. Ordering information

Table 3: Ordering information

| Type number | Package | | |
|-------------|---------|---|----------|
| | Name | Description | Version |
| PCF87852E | LFBGA73 | plastic low profile fine-pitch ball grid array package; 73 balls; body 7 × 7 × 1.05 mm | SOT751-1 |

6. Block diagram

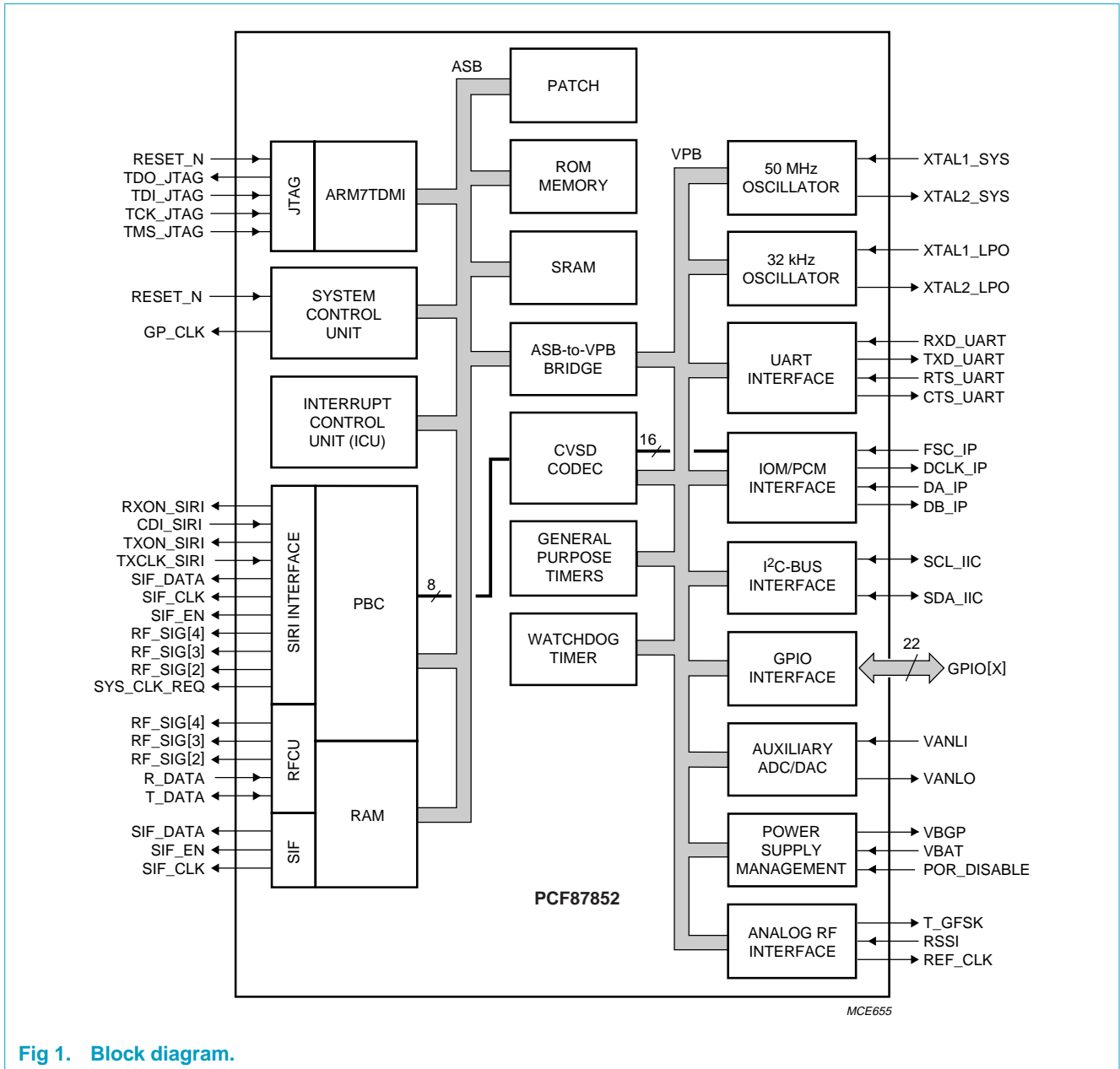


Fig 1. Block diagram.

7. Functional description

The PCF87852 is designed to be used as a low-cost, low-power radio-based cable replacement, or wireless link. This link will be the basis for PCs, telephones, PDAs headsets and peripherals to communicate together on an ad-hoc basis. It is designed to handle the Bluetooth specification.

The PCF87852 is intended to combine the Bluetooth protocol stack, link controller, link manager, HCI Firmware and radio of the Bluetooth system specification in one IC with embedded software. **Figure 2** shows a typical example of the PCF87852 in its environment. Together with few external components and an antenna it forms a Bluetooth system. In most cases this system will be attached to a host, for example a GSM baseband controller or a PC processor.

The industry standard ARM7TDMI microcontroller with low power consumption per MHz is integrated. There is a ROM memory and a static RAM on-chip. There are no provisions for external controllers to directly access on-chip data memories. Communication with an external host, for example a PC, GSM or PDA, is handled via the HCI.

The PCF87852 is able to run the complete Bluetooth application up to HCI.

A number of industry standard interfaces such as IOM/PCM, I²C-bus, and UART are supported by on-chip hardware to act as possible host interfaces.

The Bluetooth link controller consists of a number of functional blocks that operate under control of the embedded microcontroller. The microcontroller has access to these blocks via the AMBA System Bus (ASB) and VLSI Peripheral Bus (VPB).

Figure 1 shows the various blocks and their interconnections.

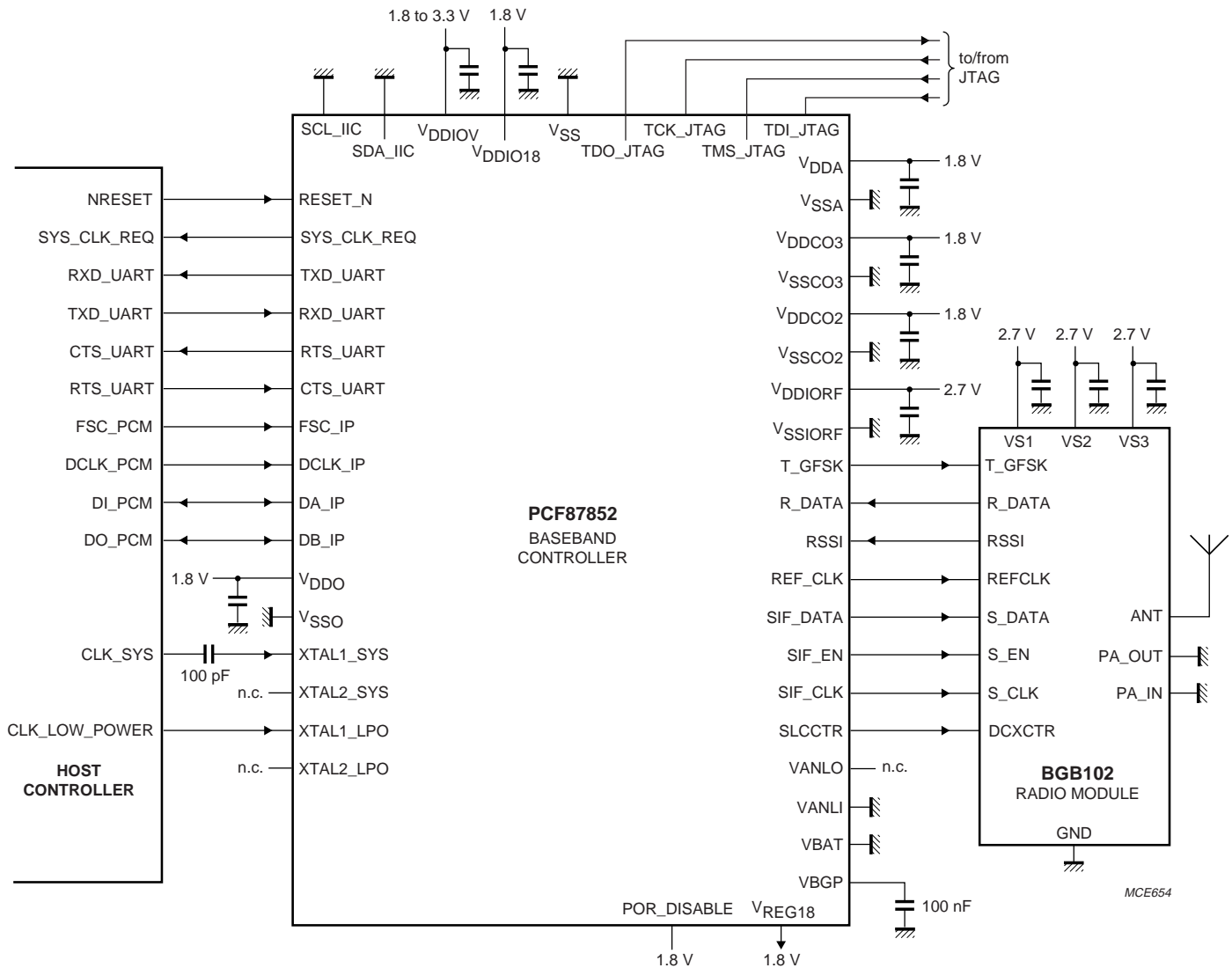


Fig 2. Application example of hosted Bluetooth system with PCF87852 and BGB102 (or BGB101) RF module.

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|----------------------------------|-------------------------------------|----------|-----------------|------|
| V_{DDC} | core supply voltage | | -0.5 | +2.5 | V |
| V_{DDIORF} | RF interface supply voltage | | -0.5 | +4.6 | V |
| V_{DDIO18} | 1.8 V I/O supply voltage | | -0.5 | +2.5 | V |
| V_{DDIOV} | variable I/O supply voltage | | -0.5 | +4.6 | V |
| V_{DDA} | analog supply voltage | | -0.5 | +2.5 | V |
| V_{DDO} | oscillator supply voltage | | -0.5 | +2.5 | V |
| V_I | input voltage on any pin | with respect to ground (V_{SS}) | [1] -0.5 | $V_{DDX} + 0.5$ | V |
| I_I | input DC current through any pin | | - | 100 | mA |
| P_{tot} | total power dissipation | | - | 200 | mW |
| T_{amb} | ambient temperature | | -40 | +85 | °C |
| T_{stg} | storage temperature | | -40 | +125 | °C |

[1] V_{DDX} represents the supply voltage of the functional block associated with the pin.

9. Revision history

Table 5: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|-----------------------------------|
| 01 | 20040423 | - | Preliminary data (9397 750 12161) |

10. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2][3]} | Definition |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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