RC5050

Programmable DC-DC Converter for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V
- 85% efficiency typical
- 1% output accuracy
- Oscillator frequency adjustable from 80KHz to 1MHz
- On-chip Power Good and Enable functions
- Over-Voltage Protection
- Foldback current limiting
- Precision trimmed low TC voltage reference
- 20 pin SOIC package
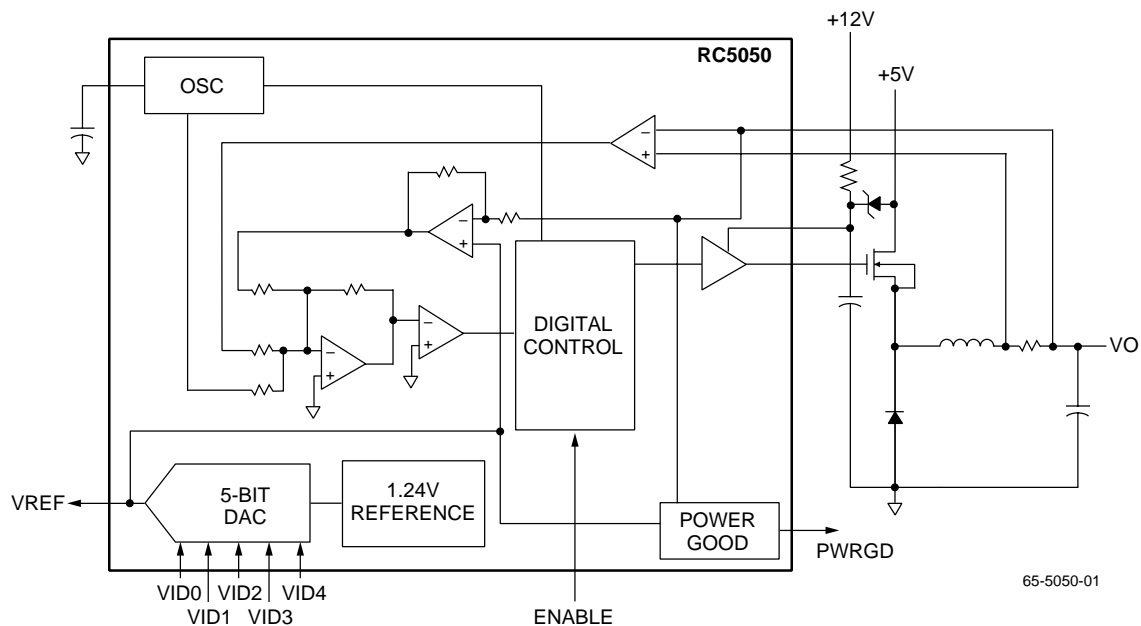- Meets Intel Pentium® II specifications using minimum number of external components

Applications

- Programmable power supply for Pentium II
- Voltage Regulator Module (VRM) for Pentium II processors
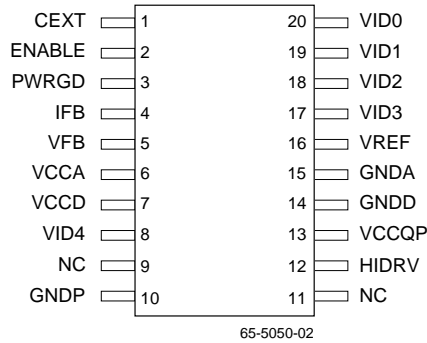- Programmable step-down power supply

Description

The RC5050 is a DC-DC controller IC which provides an accurate, programmable output for all Pentium II CPU applications. The RC5050 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5050 uses a high level of integration to deliver load currents in excess of 15A from a 5V source with minimal external circuitry. Non-synchronous operation allows a low cost solution for most CPU power supply applications. The internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5050 also offers integrated functions including Power Good, Output Enable, over-voltage protection and current limiting.

Block Diagram

65-5050-01

Pin Assignments

```
        CEXT  ┌──┐ 1        20 ┌──┐  VID0
      ENABLE  ┌──┐ 2        19 ┌──┐  VID1
       PWRGD  ┌──┐ 3        18 ┌──┐  VID2
         IFB  ┌──┐ 4        17 ┌──┐  VID3
         VFB  ┌──┐ 5        16 ┌──┐  VREF
        VCCA  ┌──┐ 6        15 ┌──┐  GNDA
        VCCD  ┌──┐ 7        14 ┌──┐  GNDD
        VID4  ┌──┐ 8        13 ┌──┐  VCCQP
          NC  ┌──┐ 9        12 ┌──┐  HIDRV
        GNDP  ┌──┐ 10       11 ┌──┐  NC
```

65-5050-02

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator Capacitor Connection**. Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable**. Open collector/TTL input. Logic LOW will disable output. A 10KΩ internal pull-up resistor assures correct operation if pin is left unconnected.
3	PWRGD	**Power Good Flag**. Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±12% of nominal.
4	IFB	**High Side Current Feedback**. Pins 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback**. Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
6	VCCA	**Analog Vcc**. Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
7	VCCD	**Digital Vcc**. Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
8	VID4	**VID4 Input**. A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 on this pin will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.
9, 11	NC	**No Internal Connection**. Connection of these pins to system ground will improve the thermal dissipation characteristics of the package.
10	GNDP	**Power Ground**. Return pin for high currents flowing in pins 12 and 13 (HIDRV and VCCQP). Connect to low impedance ground.
12	HIDRV	**FET Driver Output**. Connect this pin to the gates of N-channel MOSFETs M1 and M2 in Figure 1. The trace from this pin to the MOSFET gates should be < 0.5".
13	VCCQP	**Power Vcc**. This is the power supply for the FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
14	GNDD	**Digital Ground**. Return path for digital logic. This pin should be connected to system ground to minimize ground loops.
15	GNDA	**Analog Ground**. Return path for low power analog circuitry. Connect to system ground to minimize ground loops.
16	VREF	**Reference Voltage Test Point**. This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected.
17–20	VID3–VID0	**Voltage Identification (VID) Code Inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pullup resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages, V_{CCA}, V_{CCD}, V_{CCQP}	13V
Voltage Identification Code Inputs, VID4-VID0	13V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltages, V_{CCA} and V_{CCD}		4.5	5	7	V
Output Driver Supply, V_{CCQP}		8.5		12	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
PWRGD Threshold	Logic HIGH Logic LOW	93 88		107 112	%V_O %V_O
Ambient Operating Temperature		0		70	°C

Electrical Characteristics

(V_{CCA}, V_{CCD} = 5V, V_{OUT} = 2.8V, F_{OSC} = 300 KHz, and T_A = +25°C using Figure 1, unless otherwise specified)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				13		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A			±20		mV
Output Temperature Drift	T_A = 0 to 60°C	•		+10		mV
Load Regulation	I_{LOAD} = 0.8A to 13A	•		-25		mV
Line Regulation	V_{IN} = 4.75 to 5.25V	•		±2		mV
Output Ripple	20MHz BW, I_{LOAD} = 13A			±11		mV

Output Voltage Regulation
    Steady State[1]
    Transient[2]
	V_{OUT} = 2.8V, I_{LOAD} = 0.8 – 15A
	I_{LOAD} = 0.8 to 14.2A, 30A/µs
		•
		•
			2.74
			2.67
				2.80
				2.80
					2.90
					2.93
						V
						V

Short Circuit Detect Threshold		•	100	120	140	mV
Efficiency	I_{LOAD} = 13A, V_{OUT} = 2.8V	•	80	85		%
Output Driver Rise and Fall Time	See Figure 2			50		ns
Turn-on Response Time	I_{LOAD} = 0 to 13A				10	ms
Oscillator Range			80	300	1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF		270	300	330	KHz
Max Duty Cycle	PWM mode		90	95		%

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, output ripple/noise and temperature drift.

2. These specifications assume a minimum of 20, 1µF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed decoupling. For motherboard applications, the PCB layout must exhibit no more than 0.5mΩ parasitic resistance and 1nH parasitic inductance between the converter output and the CPU.

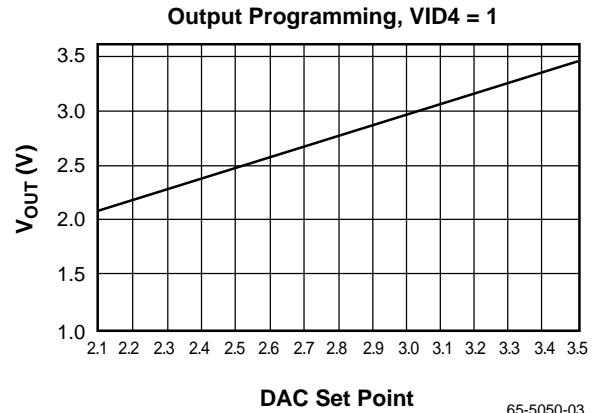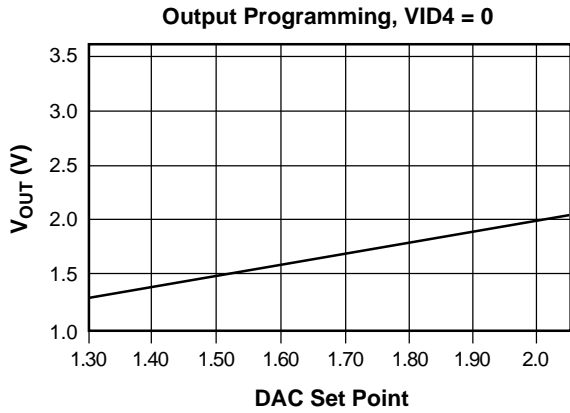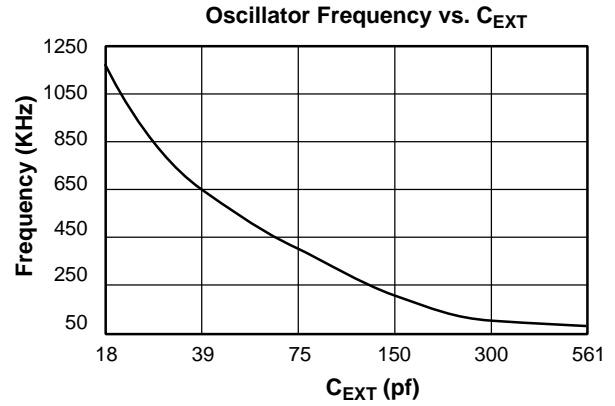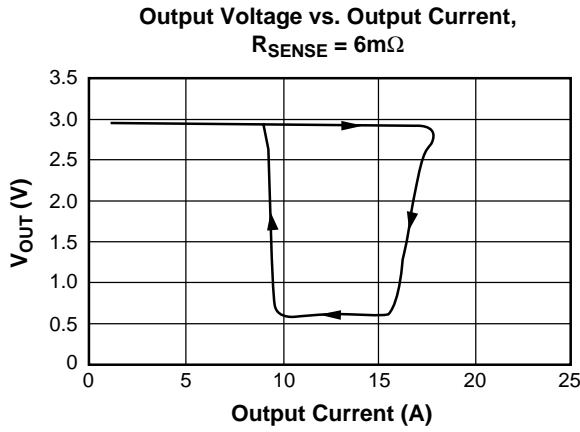**Table 1. Output Voltage Programming Codes**

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

1.   0 = processor pin is tied to GND
     1 = processor pin is open.

Typical Operating Characteristics
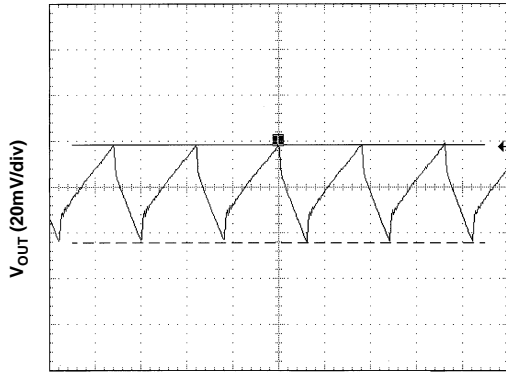
(VCCA, VCCD = 5V, fosc = 280 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

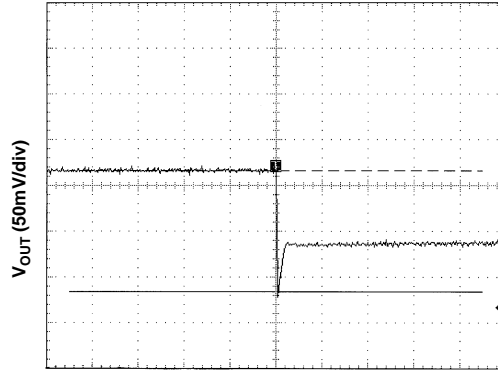**Efficiency vs. Output Current**

Load Regulation, V_{OUT} = 2.8 V

Output Voltage vs. Output Current, R_{SENSE} = 6mΩ

Oscillator Frequency vs. C_{EXT}

Output Programming, VID4 = 0

Output Programming, VID4 = 1
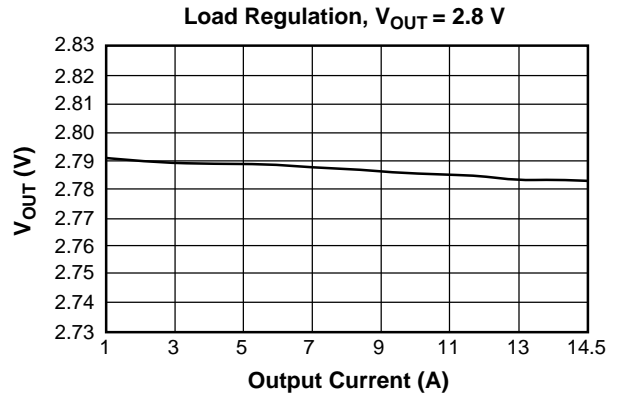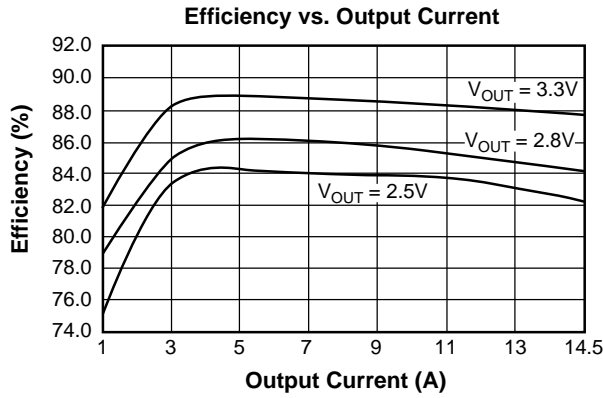
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Typical Operating Characteristics (continued)

Output Ripple, 2.8V @ 13A

V_{OUT} (20mV/div)

Time (2μs/division)

Transient Response, 0.5A to 13A

V_{OUT} (50mV/div)

Time (50μs/division)

Switching Waveforms, 0.5A Load

500mV/div

20mV/div

◄— CEXT pin

◄— HDRV pin
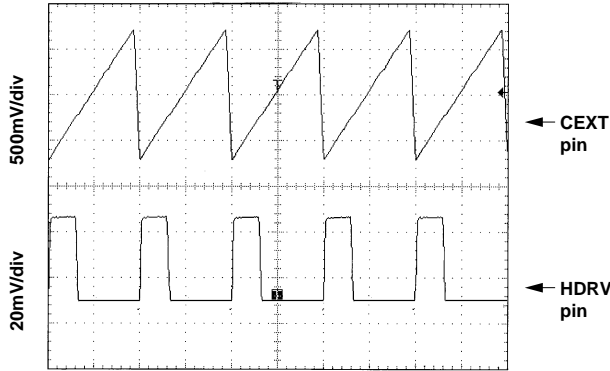
Time (2μs/division)

Switching Waveforms, 13A Load

500mV/div

20mV/div

◄— CEXT pin

◄— HIDRV pin
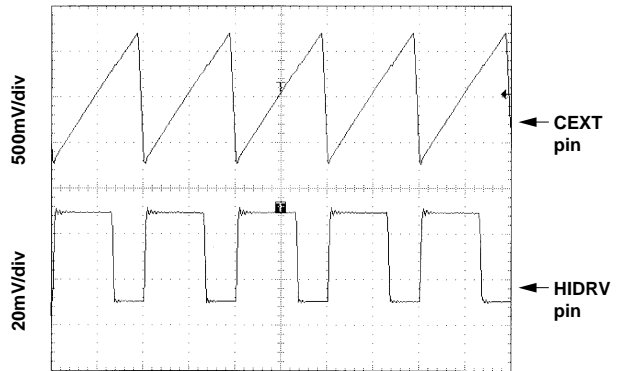
Time (2μs/division)

Output Startup, System Power-up

V_{OUT} (1V/div)

V_{IN} (1V/div)
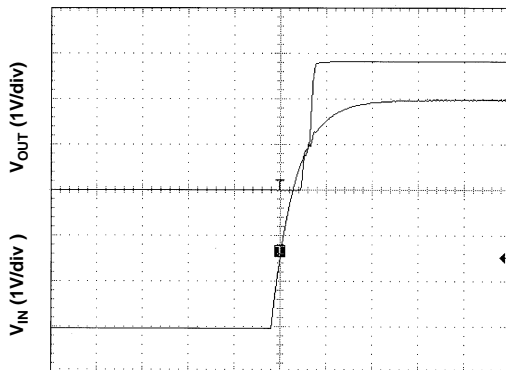
Time (10ms/division)

Output Startup from Re-enable

V_{OUT} (1V/div)

ENABLE (1V/div)

Time (10ms/division)

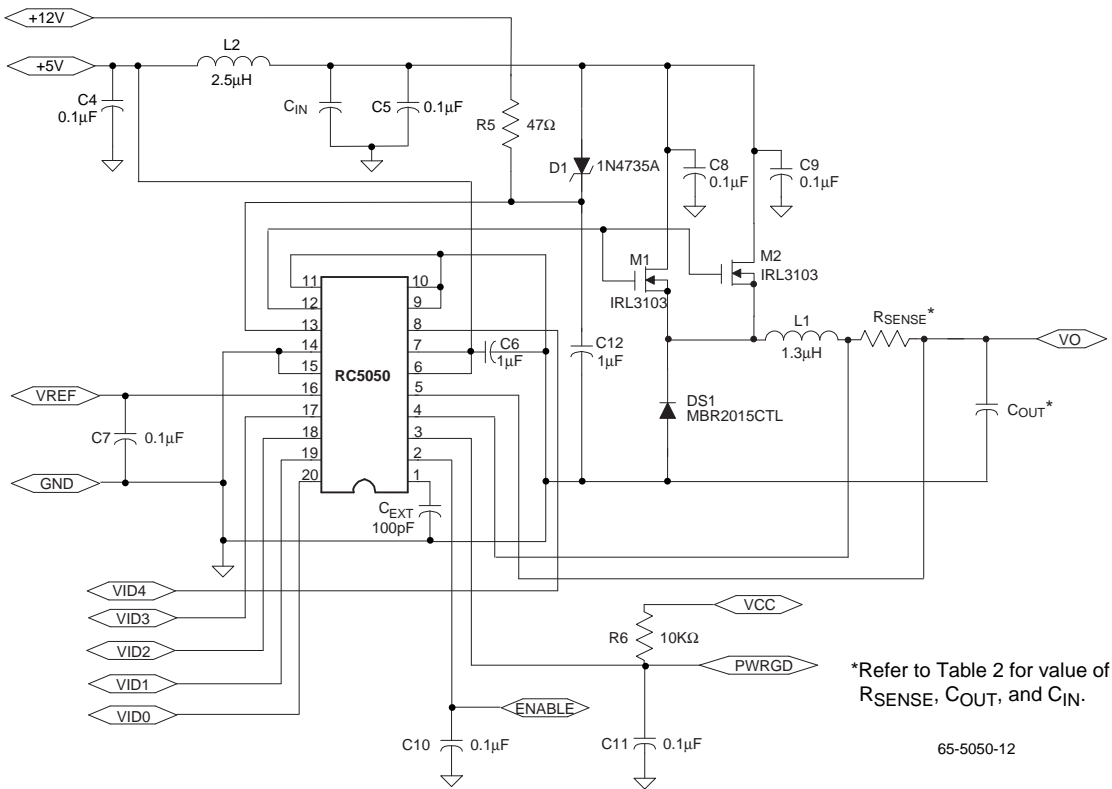65-5050-04
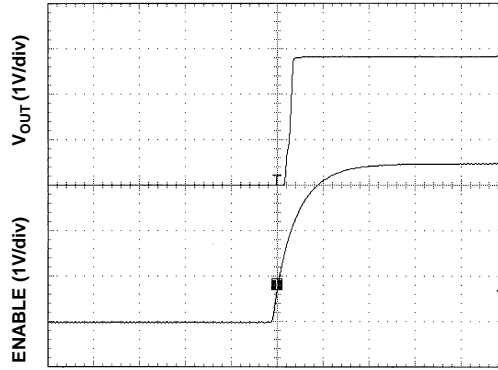
Test Circuit

Figure 1. 15A Application Circuit for Pentium II Processor
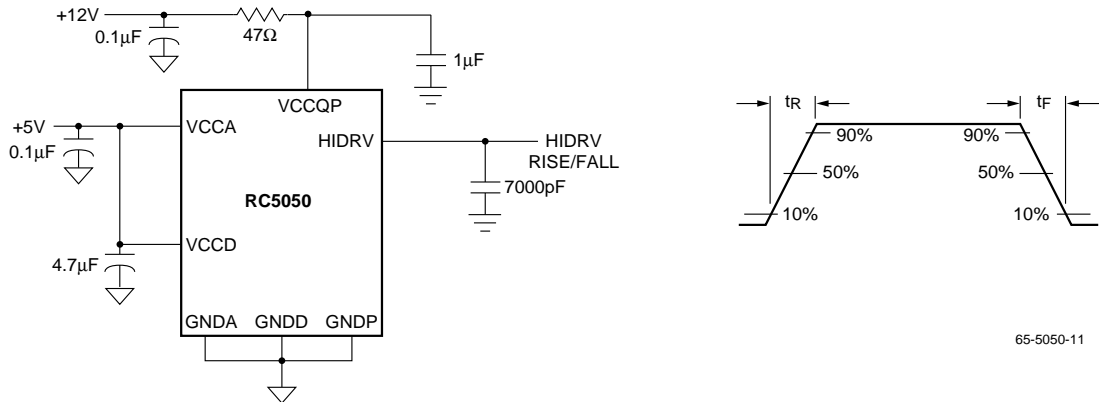

Figure 2. Output Driver Test Circuit

Table 2. Recommended Bulk Capacitors for CPU-based Applications

Application	Output Current	C_{IN}	C_{OUT}	C_{OUT} Maximum ESR	R_{SENSE}
Motorola PowerPC 603/604 Motherboard	7A	2 x 1500µF, 6V Sanyo 6MV1500CX	2 x 1500µF, 6V Sanyo 6MV1500SX	22mΩ	10.5mΩ
Intel Pentium II Klamath Motherboard	14.2	3 x 1200µF, 10V Sayno 10MV1200EG	5 x 1500µF, 6.3V Sanyo 6MV1500GX	9.0mΩ	5.5mΩ
Intel Pentium II Motherboard (All versions including next generation)	15A	3 x 1200µF, 10V Sayno 10MV1200EG	7 x 1500µF, 6.3V Sanyo 6MV1500GX	6.0mΩ	5.0mΩ

Table 3. RC5050 Application Bill of Materials for Intel Pentium II Processors

Reference	Manufacturer Part #	Description	Requirements/Comments
C4, C5, C7–C11	Panasonic ECU-V1H104ZFX	0.1µF 50V capacitor	
Cext	Panasonic ECU-V1H121JCG	100pF capacitor	
C12, C6	Panasonic ECSH1CY105R	1µF 16V capacitor	
C_{IN}	Sanyo 10MV1200EG	1200µF 10V electrolytic capacitor 10mm x 20mm	ESR < 62mΩ See Table 2
C_{OUT}	Sanyo 6MV1500GX	1500µF 6.3V electrolytic capacitor 10mm x 20mm	ESR < 44mΩ See Note 1 and Table 2
DS1	Motorola MBR2015CT	Schottky Diode	V_f < 0.52 at I_f = 10A
D1	1N4735A	6.2V Zener Diode, Motorola	
L1	Skynet 320-8107	1.3µH, 14A inductor DCR ~ 2.5mΩ	See Note 2
L2	Skynet 320-6110	2.5µH, 11A inductor DCR ~ 6mΩ	See Note 3
M1, M2	International Rectifier IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 19mΩ V_{GS} < 4.5V, I_D = 15A See Note 4
R_{SENSE}	Copel AWG#18	5.5mΩ CuNi Alloy Wire Resistor	
R5	Panasonic ERJ-6GEY050Y	47Ω 5% resistor	
R6	Panasonic ERJ-6ENF10.0KV	10KΩ 5% resistor	

Notes:

1. In order to meet the voltage transient requirements for the Intel Pentium II Motherboard application, the equivalent ESR of the output capacitors must not exceed 7.5mΩ. In order to satisfy the specified Output Voltage Regulation requirements for V_{OUT} = 1.8V at 15A for next generation processors, the output capacitors must exhibit no more than 6.0mΩ equivalent ESR for a motherboard application. The use of the capacitors recommended in Table 1 will address this and other voltage specifications without significant added cost, although it is left up to the user to specify the components used. Please refer to Application Bulletin 5 for additional considerations required to meet the Intel Pentium II voltage transient specifications.

2. To optimize a converter for 15A at 1.8V output, f_{SW} = 300 kHz, change the value of L1 to 1.24µH.

3. Inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.

4. For 15A designs using IR3103 MOSFETs, heat sinks with thermal resistance Θ_{SA} < 50°C/W should be used.

Application Information

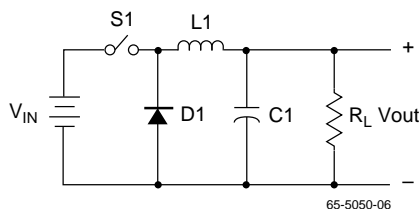## Simple Step-Down Converter

Figure 3. Simple Buck DC-DC Converter

Figure 3 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5050. Referring to Figure 3, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where T_S is the overall switching period and $(T_S - T_{ON})$ is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

where V_{SW} = MOSFET switching loss
$\phantom{where V_{SW}}$ = $I_L \cdot R_{DS,ON}$

The RC5050 Controller

The RC5050 is a programmable DC-DC controller IC. When designed around the appropriate external components, The RC5050 can be configured to deliver more than 14.5A of output current. The RC5050 utilizes both current-mode and voltage-mode control to create an integrated step-down voltage regulator. During heavy loading conditions, the RC5050 functions as a PWM step down regulator. Under light loads, the controller goes into Pulse Frequency Modulation (PFM) or pulse-skipping mode. The controller will sense the load level and switch between the two modes automatically, thus optimizing its efficiency under all conditions.

Main Control Loop

For this discussion, refer to the Block Diagram on page 1 of the data sheet. The control loop of the regulator contains two main sections; the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the point at which the max current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET(s). The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5050 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5050 contains a high current output driver which utilizes high speed bipolar transistors arranged in a push-pull configuration. This driver is capable of delivering 1A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity. The output driver power supply, VCCQP, is derived from an external 12V supply through a 47Ω series resistor. The resulting voltage is sufficient to provide the gate-source voltage to the external MOSFET required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5050 is a precision bandgap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference output is the resulting output from an integrated 5-bit DAC. The DAC is provided in order to allow the DC-DC converter output to be directly programmable via a 5-bit digital input. When the VID4 pin is in the HIGH state, pins VID3–VID0 will scale the output voltage from 2V to 3.5V in 100mV increments. When the VID4 pin is pulled LOW, the output can be programmed from 1.3V to 2.05V in 50mV steps. For guaranteed stable operation under all operating conditions, a 0.1μF decoupling capacitor should be connected to the VREF pin. No load should be imposed upon this pin.

Power Good (PWRGD)

The RC5050 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a constant voltage monitor on the VFB pin. The internal circuitry compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±10% of its nominal setpoint. The Power Good flag provides no other control function to the RC5050.

Output Enable (ENABLE)

Intel specifications state that the DC-DC converter should accept an open collector signal for controlling the output voltage; a logic LOW on the ENABLE pin disables the output voltage. When disabled, the PWRGD output is in the low state.

Upgrade Present

Intel specifications state that the DC-DC converter should accept an open collector signal (UP#), used to indicate the presence of an upgrade processor. The typical state is high (standard processor). When in the low or ground state (OverDrive processor present), the output voltage must be disabled unless the converter can supply the OverDrive processor's power requirements. Because the RC5050 can supply the OverDrive processor requirements, the UP# signal is not required.

Over-Voltage Protection

The RC5050 provides a constant monitor of the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition will be assumed and the RC5050 will disable the output drive signal to the external MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage developed across the sense resistor exceeds the 120 mV comparator threshold voltage, the RC5050 will reduce the output duty cycle to protect the power devices.

The DC-DC converter will return to normal operation after the fault has been removed, for either an over voltage or a short circuit condition.

Oscillator

The RC5050 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (C_{EXT}) is used to preset the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as in choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

Additionally, the efficiency losses due to switching of the MOSFETs will increase as the operating frequency is increased. Therefore, efficiency will be optimized at lower operating frequencies.

Due to the trend of increasing load current at lower supply voltages, an operating frequency of 300 KHz has been chosen to optimize efficiency while maintaining excellent output regulation and transient performance.

Design Considerations and Component Selection

MOSFET Selection

This application requires the use of N-channel, Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 37$ mΩ (lower is better).
- Low gate drive voltage, $V_{GS} \leq 4.5$V.
- Power package with low Thermal Resistance.
- Drain current rating of 20A minimum.
- Drain-Source voltage > 15V

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 4 presents a list of suitable MOSFETs for this application.

Two MOSFETs in Parallel

At higher load currents, it is recommend that two MOSFETs be used in parallel instead of a single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 15A with one MOSFET:

  $$P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle})$$
  $$= (15)^2(0.050*)(2.8+0.4)/(5+0.4-0.35)$$
  $$= 7.1 \text{ W}$$

  With two MOSFETs in parallel:

  $$P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle})$$
  $$= (15/2)^2(0.037*)(2.8+0.4)/(5+0.4-0.35)$$
  $$= 1.3\text{W/FET}$$

  * **Note:** $R_{DS,ON}$ increases with temperature. Assume $R_{DS,ON} = 25$mΩ at 25°C. $R_{DS,ON}$ can easily increase to 50mΩ at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS,ON}$ to rise above the listed maximum value of 37mΩ.

- **No added heat sink required.** With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, no external heat sink is required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.

- **Higher current capability.** With thermal management under control, this on-board DC-DC circuit is able to deliver load currents up to 15A with no performance or reliability concerns.

Table 4. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}(m\Omega)$		Package	Thermal Resistance
			Typ.	Max.		
Fuji 2SK1388	V_{GS}=4V, I_D=17.5A	T_J =25°C	25	37	TO-220	Φ_{JA}=75
		T_J =125°C	37	—		
Siliconix SI4410DY	V_{GS}=4.5V, I_D=5A	T_J =25°C	16.5	20	SO-8 (SMD)	Φ_{JA}=50
		T_J =125°C	28	34		
National Semiconductor NDP706AL	V_{GS}=5V, I_D=40A	T_J =25°C	13	15	TO-220	Φ_{JA}=62.5 Φ_{JC}=1.5
NDP706AEL		T_J =125°C	20	24		
National Semiconductor NDP603AL	V_{GS}=4.5V, I_D=10A	T_J =25°C	31	40	TO-220	Φ_{JA}=62.5
		T_J =125°C	42	54		Φ_{JC}=2.5
National Semiconductor NDP606AL	V_{GS}=5V, I_D=24A	T_J =25°C	22	25	TO-220	Φ_{JA}=62.5
		T_J =125°C	33	40		Φ_{JC}=1.5
Motorola MTB75N03HDL	V_{GS}=5V, I_D=37.5A	T_J =25°C	6	9	TO-263 (D² PAK)	Φ_{JA}=62.5
		T_J =125°C	9.3	14		Φ_{JC}=1.0
Int. Rectifier IRLZ44	V_{GS}=5V, I_D=31A	T_J =25°C	—	28	TO-220	Φ_{JA}=62.5
		T_J =125°C	—	46		Φ_{JC}=1.0
Int. Rectifier IRL3103S	V_{GS}=4.5V, I_D=28A	T_J =25°C	—	19	TO-220	Φ_{JA}=62.5
		T_J =125°C		31		Φ_{JC}=1.0

Note:

1. $R_{DS,ON}$ values at Tj = 125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only.

MOSFET Gate Bias

Figure 4 illustrates how an external 12V supply is used to bias the output driver supply, VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1μF capacitor filter is used to filter the VCCQP supply. This method provides a sufficient gate-to-source bias voltage (V_{GS}) to the MOSFET, and therefore reduces the $R_{DS,ON}$ and the resulting power loss within the MOSFET. Figure 5 illustrates how the $R_{DS,ON}$ decreases dramatically as V_{GS} increases. A 6.2V Zener (D1) is used to clamp the voltage at VCCQP to a maximum of 12V, thus ensuring that the absolute maximum voltage limit of the IC will not be exceeded.
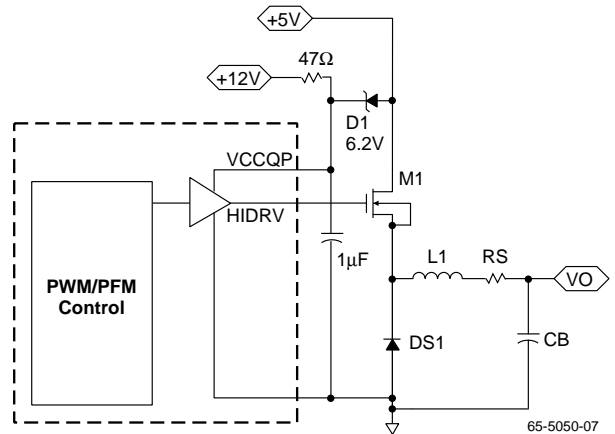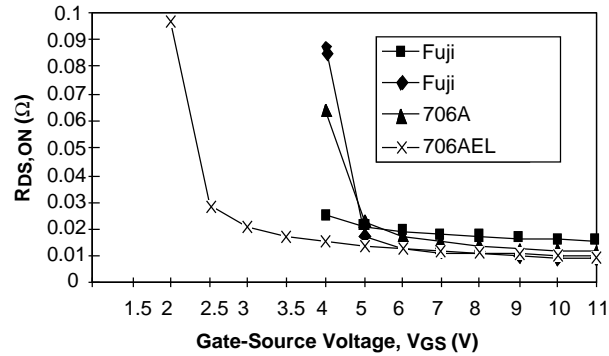

Figure 4. MOSFET Gate Bias Configuration

Figure 5. $R_{DS,ON}$ vs. V_{GS} for Selected MOSFETs

Converter Efficiency

Losses due to parasitic resistance in the switches, inductor coil and sense resistor dominate at high load current levels. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R losses
- Inductor coil losses
- Sense resistor losses
- Gate-charge losses
- Diode-conduction losses
- Transition losses
- Input capacitor losses
- Losses due to the operating supply current of the IC.

The following sections provide details of these dominant loss components.

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the DC coil resistance (R$_l$). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2 \times R_l$.

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed range in order to maximize either ripple or transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{OUT} - V_{IN})}{f} \times \frac{V_{OUT}}{V_{IN}} \times \frac{ESR}{V_r}$$

where:

- V_{IN} = Input Power Supply
- V_{OUT} = Output Voltage
- f = DC/DC converter switching frequency
- ESR = Equivalent series resistance of all output capacitors in parallel
- V_r = Peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{min} = 2Co \times \frac{(V_{IN} - V_{OUT})D_m V_{tb}}{I_{p^2}}$$

where:

- Co = The total output capacitance
- I_p = Peak to peak load transient current
- V_{tb} = The output voltage tolerance budget allocated to load transient
- D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained between L_{min} and L_{max}. Adding margin by increasing L_{max} almost always adds expense since all the variables are predetermined by system performance except for C_O, which must be increased to increase L_{max}. Adding margin by decreasing L_{min} can either be done by purchasing capacitors with lower ESR or by increasing the DC/DC converter switching frequency. The RC5050 is capable of running at high switching frequencies and provides significant cost savings for the newer CPU systems that typically run at high supply current.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Raytheon has implemented a current sense methodology to limit the power delivered to the load in the event of an over-current condition. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has a threshold voltage, nominally 120mV. Table 6 states the limits for the comparator threshold of the Switching Regulator.

Table 6. RC5050 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator V$_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, the designer must pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$$R_{SENSE} = \frac{V_{th}}{I_{SC}}, \text{ where: } I_{SC} = \text{Output short circuit current}$$

$$I_{SC} \geq I_{inductor} = I_{Load, max} + \frac{(I_{pk} - I_{min})}{2}$$

where I_{pk} and I_{min} are peak ripple current and $I_{load, max}$ = maximum output load current

The designer must also take into account the current ($I_{pk} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 6 illustrates the inductor current waveform for the RC5050 DC-DC converter at maximum load.
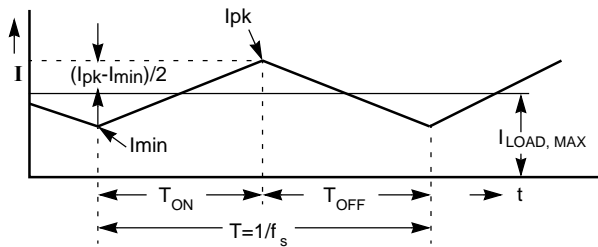

Figure 6. Typical DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_{D})}{(V_{IN} - V_{SW} + V_{D})} \times T$$

where:

- V_{in} = input voltage to converter
- V_{SW} = voltage across the MOSFET
        = $I_{LOAD} \times R_{DS,ON}$
- V_{D} = Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs,
        where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 2.8V, an inductor value of 1.3µH and a switching frequency of 285KHz (using C_{EXT} = 100pF), the inductor current can be calculated as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 2.8)}{1.3 \times 10^{-6}} \times$$

$$\frac{(2.8 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{285 \times 10^{3}} \approx 3A$$

Therefore, for a continuous load current of 14.5A, the peak current through the inductor, I_{pk}, is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load, max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 3 = 17.5A$$

For continuous operation at 14.5A, the short circuit detection threshold must be at least 17.5A.

The next step is to determine the value of the sense resistor. Including tolerance, the sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{3.0 + I_{Load,max}} \times (1 - TF)$$

where TF = Tolerance Factor for the sense resistor.

There are several different types of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various sense resistors.

Table 7. Comparison of Sense Resistors

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Based on the Tolerance in the above table:

- For an embedded PC trace resistor and $I_{load,max} = 14.5A$:

$$R_{SENSE} = \frac{V_{th,min}}{3.0A + I_{Load, max}} \times (1 - TF) =$$

$$\frac{100mV}{3.0A + 14.5A} \times (1 - 29\%) = 4.1m\Omega$$

- For a discrete resistor and $I_{load, max} = 14.5A$:

$$R_{SENSE} = \frac{V_{th,min}}{3.0A + I_{Load, max}} \times (1 - TF) =$$

$$\frac{100mV}{3.0A + 14.5A} \times (1 - 5\%) = 5.4m\Omega$$

For user convenience, Table 8 lists the recommended values for sense resistor values at various load currents using an embedded PC trace resistor or discrete resistor.

Table 8. R~sense~ for Various Load Currents

$I_{Load,max}$ (A)	R~SENSE~ PC Trace Resistor (mΩ)	R~SENSE~ Discrete Resistor (mΩ)
10.0	5.5	7.3
11.2	5.0	6.7
12.4	4.6	6.2
13.9	4.2	5.6
14.0	4.2	5.6
14.5	4.1	5.4

RC5050 Short Circuit Current Characteristics

The RC5050 has a short circuit current characteristic that includes a foldback function with hysteresis that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output using a sense resistor value of 6mΩ is presented in the Typical Operating Characteristics section, page 5. The converter performs with a typical voltage regulation characteristic until the voltage across the resistor exceeds the internal short circuit comparator threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, DS1. DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. A vital selection criteria for DS1 is that it exhibits a very low forward voltage drop, as this parameter will directly impact the regulator efficiency as the output voltage is reduced. Table 9 presents several suitable Schottky diodes for this application. Note that the diode MBR2015CTL has a very low forward voltage drop. This diode is most ideal for applications where output voltages below 2.8V are required.

Table 9. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips PBYR1035	$I_F = 20A; T_j=25°C$ $I_F = 20A; T_j=125°C$	< 0.84V < 0.72V
Motorola MBR2035CT	$I_F = 20A; T_j=25°C$ $I_F = 20A; T_j=125°C$	< 0.84V < 0.72V
Motorola MBR1545CT	$I_F = 15A; T_j=25°C$ $I_F = 15A; T_j=125°C$	< 0.84V < 0.72V
Motorola MBR2015CTL	$I_F = 20A; T_j=25°C$ $I_F = 20A; T_j=150°C$	< 0.58V < 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5050. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET(s). Low "ESR" capacitors are best suited for this type of application and incorrect selection can influence the converter's overall performance. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

where:
- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads.

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

where:
- ΔV is the maximum voltage deviation due to load transients
- ΔT is the reaction time of the power source (Loop response time of the RC5050), approximately 2µs
- I_O is the output load current.

For I_O = 12.2A (0.8 to 13A) and ΔV = 100mV, the bulk capacitance required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{12.2 \times 2\mu s}{100mV - 12.2A \times 7.5m\Omega} = 3200\mu F$$

Input Filter

It is recommended that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and also to limit the inrush current into the input capacitors during power up. An inductor value of around 2.5µH is recommended, as illustrated below.
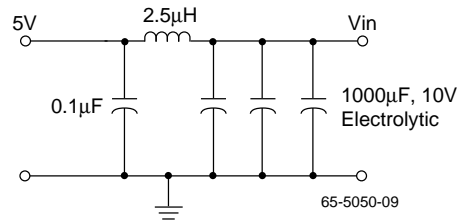
PCB Layout Guidelines and Considerations

PCB Layout Guidelines

1. Placement of the MOSFETs relative to the RC5050 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5050 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET(s). This noise will radiate all over the board and will be very difficult to suppress, especially when the oscillator frequency is increased.

   Figure 7 depicts an example of proper placement of the MOSFETs in relation to the RC5050 as well as an example of incorrect placement of the MOSFETs.

   In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5050. That is to say, traces that connect to pins 12 and 13 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.
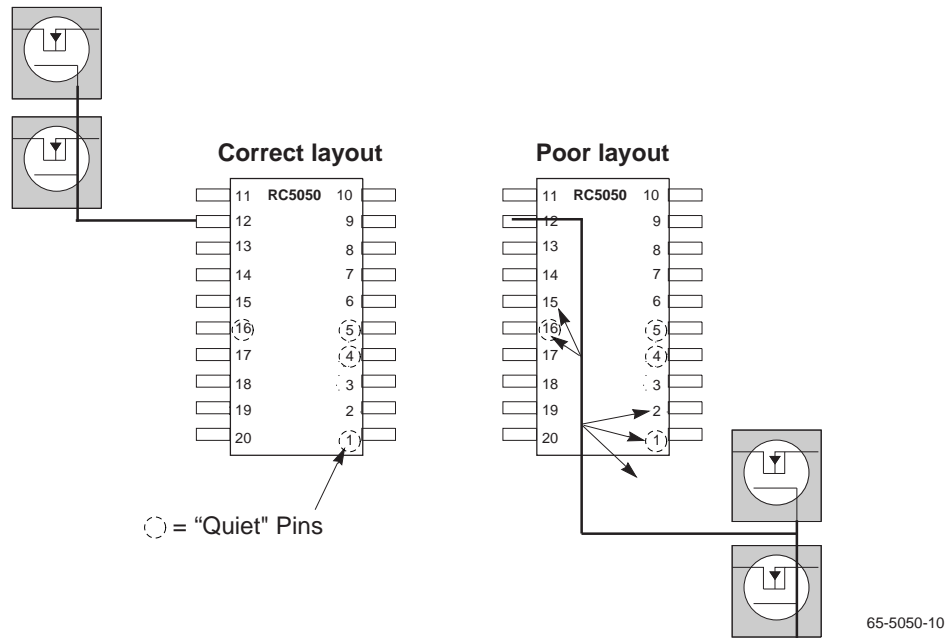
Figure 7. Examples of Good and Bad MOSFET Layout

2. Place decoupling capacitors (0.1μF) as close to the RC5050 pins as possible. Extra lead length on these capacitors will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help to add isolation between pins.

4. The CEXT timing capacitor should be surrounded with a ground trace if possible. The placement of a ground or power plane underneath the capacitor will also provide further noise isolation. This will help to shield the oscillator from the noise on the PCB. This capacitor should be placed as close to pin 1 as possible.

5. Group the MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Also place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1μF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

6. The traces that run from the RC5050 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5050 feedback input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer and use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

PC Board Layout Checklist

- **Bypass Capacitor near Vref pin.**
  This pin should be adequately bypassed with a 0.1μF capacitor.
- **Bypass Capacitors for VCC (5V).**
  A 0.1μF should be placed right next to the VCC pin of the controller.
- **Bypass Capacitors for Power MOSFET.**
  A 0.1μF cap should be placed at the drain connection of each power MOSFET.
- **5V Connection to the controller IC.**
  Each VCC pin on the IC should be connected to the 5V power plane through its own via.
- **Power MOSFET Gate Drive Trace.**
  – The gate drive trace should be routed on one layer only.
  – The controller IC and the power FET should be oriented in such a way as to minimize the trace length of the gate drive trace (< 1 inch).
  – The gate drive trace routing should stay away from the quiet analog section of the RC50XX controller IC. (i.e. keep away from Vref, IFB, VFB, and CEXT.)
- **Bulk Capacitance.**
  – The input bulk capacitance needs to be located less than 1" from the drain of the power MOSFET. We recommend the following guidelines for the amount of bulk input capacitance:
    • For an output load of <10A use 2 X 1500μF caps.
    • For an output load of >10A use 3 X 1500μF caps.
  – The output bulk capacitors should be located as close to the CPU socket as possible. We recommend the following guidelines for the amount of bulk output capacitance:
    • For Pentium Pro use 4 X 1500μF.
    • For P55C MMX Pentium/ AMD K6 use 2X 1500μF.
    • For Pentium II use 7 X 1500μF.

- **Inductor Location.**
  The inductor should be located near to the Source of the Power MOSFET. The ideal condition would be to use an internal power plane to connect the Source of the power MOSFET, the inductor, and the flyback schottky diode together.
- **Sense Resistor.**
  – The sense resistor should be located next to the inductor.
  – The two traces that run from the sense resistor to the RC50XX controller IC should be minimum width traces and be run parallel to each other. We recommend these sense resistor values:
    - For Pentium Pro use 0.006Ω.
    - For P55C MMX Pentium/ AMD K6 use 0.007Ω.
    - For Pentium II use 0.006Ω.
- **Ground Plane.**
  The RC50XX controller IC have a continuous ground plane running underneath the entire chip area. Each of the IC ground pins should have a separate via connection down into the ground plane.
- **Input Filter.**
  In many high current DC-DC converter designs, it is advisable to add an input inductor in order to create an input filter. An inductor on the order of 1-3uH is usually all that is required to perform the filter. When this component is added to the circuit, it is important that the RC50XX controller IC receive its VCC power from the system side of the input inductor and not the "dirty" side of the inductor. (ie the side that is connected to the power MOSFET drains)

- **To Minimize Electromagnetic Interference (EMI).**
  – Avoid long ground connections. Connect directly to the ground plane.
  – Use a star ground, where all grounds are connected to one point.
  – Use good quality inductors such as torrids or pot cores. Avoid rod inductors.
  – Route the high current carrying traces as power planes where possible.
  – Keep sensitive low-level signals away from the active switching components. Try to route them using the ground plane as a shield.

## Example of a PC Motherboard Layout and Gerber File

A reference design for motherboard implementation of the RC5050 along with the Layout Gerber File and Silk Screen are presented below. The actual PCAD Gerber File can be obtained from a Raytheon Electronics local Sales Office or from Marketing at 650-966-7734.

RC5050 Evaluation Board

Raytheon Electronics provides an evaluation board for the purpose of verifying the system level performance of the RC5050. The evaluation board serves as a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your local Sales Office or Raytheon Electronics Marketing department at 650-966-7734 for an evaluation board.
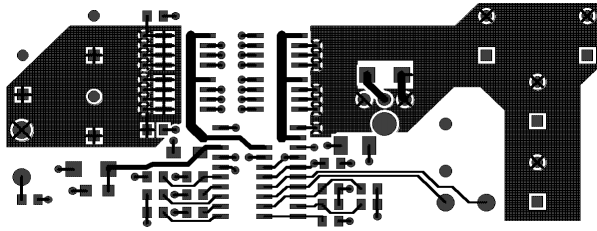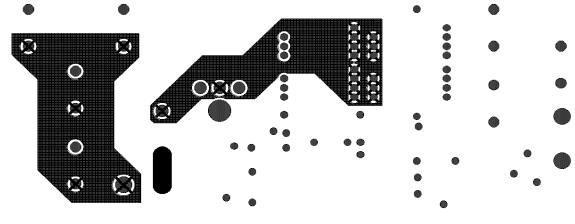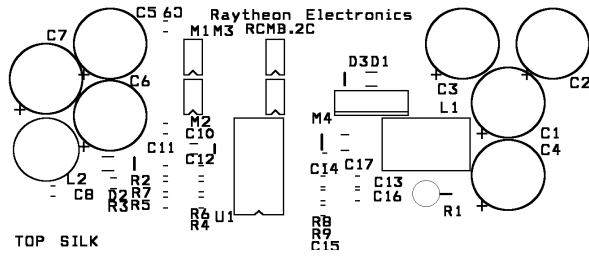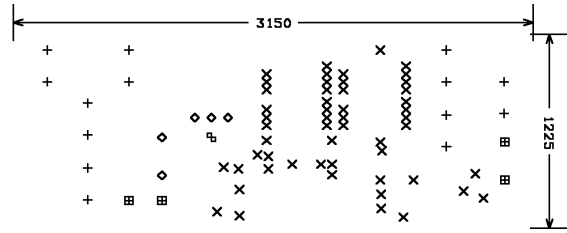
TOP
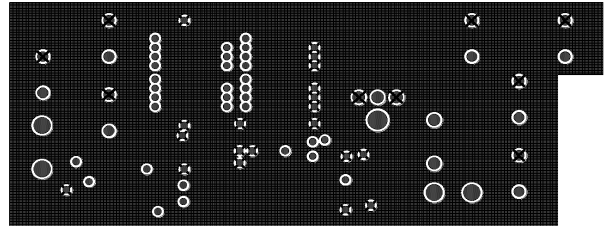
GND
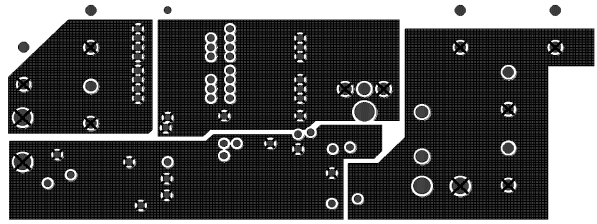
POWER

BOTTOM

TOP SILK

Mechanical Dimensions – 20 Lead SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.