

**FULL AUTOMATIC MULTISTANDARD CHROMA
DECODER WITH EMBEDDED CHROMA DELAY LINE**

ADVANCE DATA

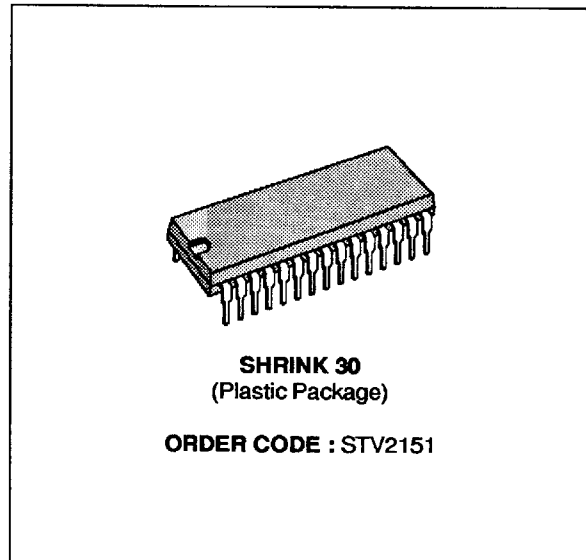
- COLOR DECODER FOR STANDARDS :
 - SECAM
 - PAL B,G
 - NTSC 3.58
 - PAL M
 - NTSC 4.43
- TWO MODES OF SELECTION OF THE STANDARDS, SELECTED BY BUS :
 - Automatic sequential selection mode on SECAM/PAL B, G with NTSC 3.58 selected by 60Hz bit only
 - BUS forced standard selection mode for : SECAM/PAL B, G / NTSC 3.58 / PAL M / NTSC 4.43
- AUTOMATIC STANDARD RECOGNITION
- INTEGRATED CHROMA DELAY LINES IN BASE BAND
- COLOR SUB-CARRIER REGENERATION WITH XTAL (4.43 and 3.58)
- AGC FOR SECAM
- HUE CONTROL ± 30 deg FOR NTSC
- S-VHS INPUT (Bus Selection)
- AUTO ALIGNED CHROMA FILTERS
- INTEGRATED AND ADJUSTMENT FREE TRAP FILTERS
- BIDIRECTIONAL BUS INFORMATION :
 - Input Data : Standard bits
50/60Hz Bit
Auto Mode for Standard
Forced Killer Mode
Killer On/Off
Bell Filter
Central Frequency
Hue Control Bits
S-VHS Mode
 - Output Data : Selected Standard Bits
Identification Bit

It can process PAL, SECAM and NTSC standards. It is controlled by I²C Bus.

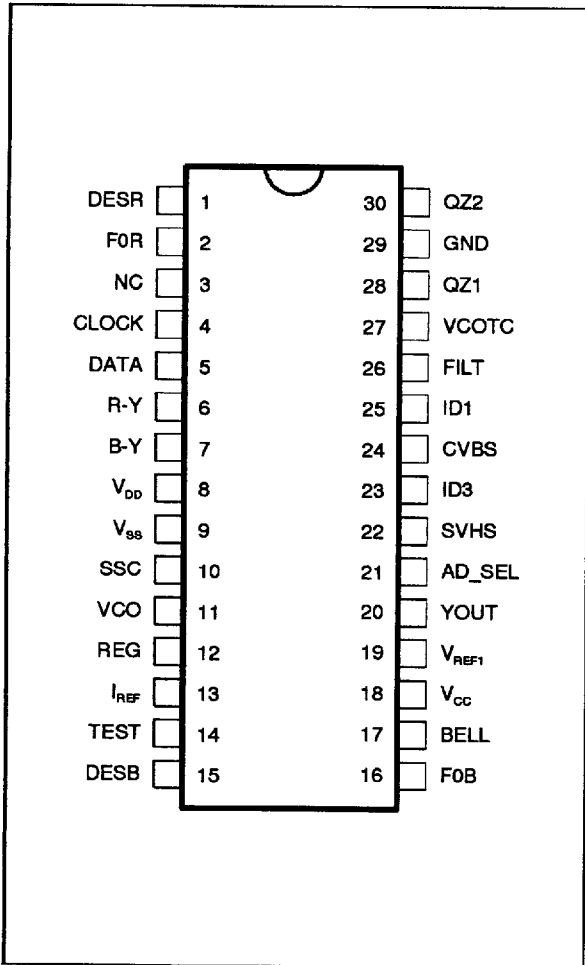
- **Inputs** : one input is dedicated to the CVBS or Y signal. An other one inputs a C signal. An integrated switch, controlled by BUS, allows to chose the right input. According to the application, this operation can be automatically treated by the microprocessor, thanks a standard identification reply available in a I²C Bus register. The synchronisation is done through a Super Sand Castle input.
- **Luminance Path** : depending on the current decoding standard, a colour sub-carrier trap (notch filter), totally integrated and alignment free, can be used or by-passed (BUS control) to deliver the Y output signal.
- **Chroma decoder** : the chroma signal goes first through the band pass filter ("bell filter" for SECAM), which is automatically tuned by the STV2151. It is then directly fit into the multistandard decoder. At least, the demodulated signals are delayed in the integrated base band delay line or led into an adder to deliver the R-Y and B-Y signals. In NTSC, the hue control allows a typical phase shift of $\pm 30^\circ$.

DESCRIPTION

The STV2151 integrates in a single chip every circuitry to deliver the Y, R-Y, B-Y signals starting from a CVBS or Y/C signals.



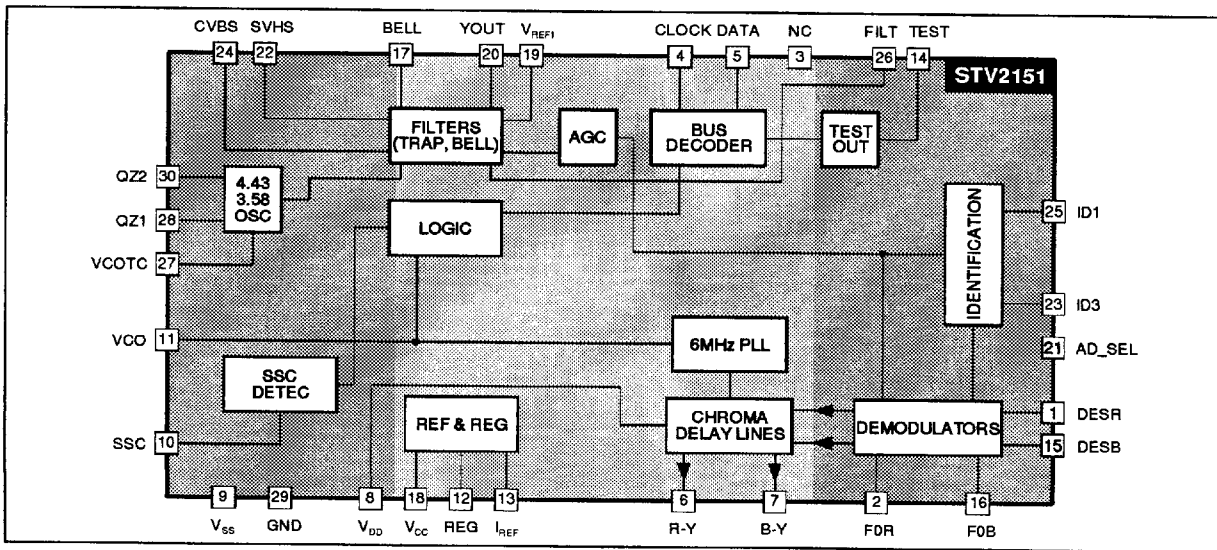
PIN CONNECTIONS



PIN DESCRIPTION

Pin N°	Symbol	Function
1	DESR	Red De-emphasis
2	FOR	For Capacitor Memory
3	NC	
4	CLOCK	Clock Input I ² C Bus
5	DATA	Data Input I ² C Bus
6	R-Y	Output of R-Y Signal
7	B-Y	Output of B-Y Signal
8	V _{DD}	Supply of the Digital Part
9	V _{SS}	Ground of Digital Part
10	SSC	Super-sand-castle Input
11	V _{CO}	6MHz PLL Filter
12	REG	Supply Regulation
13	I _{REF}	Current Reference
14	TEST	Test Output
15	DESB	Blue De-emphasis
16	FOB	F0b Capacitor Memory
17	BELL	RLC Input for Bell Filter
18	V _{CC}	Supply of the Analog Part
19	VERF1	Internal Voltage Reference
20	YOUT	Luminance Output
21	AD_SEL	Address Selection
22	SVHS	SVHS Input
23	ID3	Criteria C3 Output
24	CVBS	CVBS Input
25	ID1	Criteria C1 Output
26	FILT	Trap Filter Capacitor Memory
27	VCOTC	4.43/3.58 Oscillator Filter
28	QZ1	Crystal 3.58MHz
29	GND	Ground of Analog Part
30	QZ2	Crystal 4.43MHz

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Standard Selection

Two ways selected by BUS (bit FSTD) :

- Selection by BUS (BUS mode) bits BS2, BS4, 60Hz.
- Selection by an internal sequence (auto mode).

When the circuit is set to "auto mode" the internal sequence is : PAL / SECAM.

When the circuit is set to "BUS mode" the following standards can be selected : PAL B,G / SECAM / NTSC 3.58 / PAL M / NTSC 4.43.

Current Standard Information

This information is always available on the BUS by the 3 bits : IS10, IS11, IS12.

Standard Identification

The identification bit (bit IDENT) is set to 1 if the incoming signal standard corresponds to the selected standard.

Color Killer

The killer signal controls the suppression of the color at the outputs of the circuit (blanking) and the trap filter bypassing. If the killer is high, there is no color signal (B&W) and no trap filter in the luminance path (mode SVHS). If the killer is low, there are colors and the trap filter is in operation.

Two modes for the killer selected by BUS (bit FKILL) :

- Auto killer mode (FKILL = 0).
- Forced killer mode (FKILL = 1).

In "auto killer mode" the killer signal depends on the ident signal :

- IDENT = 0 killer high → B&W
- IDENT = 1 killer low → color

In "forced killer mode" the killer signal depends on the BUS bit :

- MKILL = 0 killer low → color
- MKILL = 1 killer high → B&W

"Bell" and Band Pass Filter

An internal loop, using the 4.43MHz Xtal oscillator as reference, locks the central frequency of the chroma filter on the frequency depending on the standard. The Q is automatically switched to the right value.

In SECAM, the center frequency can be shifted by BUS by step of 7kHz from 0 to 100kHz.

It is possible to stop the automatic bell filter calibration by bus.

Trap Filter

Integrated biquad filters are used to perform the trap filters. These filters are adjustment-free using also the 4.43MHz/3.58MHz Xtal oscillator reference.

In SECAM, PAL B/G, and NTSC the IC uses two trap filters in series. In SECAM the first one is centered on 4.1MHz and the second one on 4.43MHz. In PAL the first one is centered on 4.43MHz and the second one on 4.8MHz.

In NTSC the first one is centered on 3.58MHz and the second one on 3.87MHz.

Baseband Delay Line

The circuit includes a double baseband delay line in a switched capacitors technology. The delay is automatically adjusted to the line duration by a PLL using the super-sand-castle signal as reference.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T _{stg}	Storage and Junction Temperature	-40 to 150	°C
T _{oper}	Operating Temperature	0 to 70	°C
R _{th(j-a)}	Thermal Resistance Junction-ambient	60	°C/W

2151-01.TBL

ELECTRICAL CHARACTERISTICS

Symbol	Pin N°	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL CONDITIONS							
		Voltage Supply			12		V
		Burst Gate Pulse			4		µs
		Standard Color Bar Patterns					
		T _{amb}			25		°C
AD_SEL	21	Address Selection	1000101 1000111	3	0	V _{CC} 0.5	V V

SUPPLY SECTION

V _{CC}	18	Main Supply Section	V _{supply} = 12V	7.4	7.7	8	V
I _{CC}	18	Main Supply Current	V _{CC} = V _{reg}			45	mA
V _{DD}	8	MOS Supply Section	V _{supply} = 12V		7		V
I _{DD}	8	MOS Supply Current	V _{CC} = V _{reg}			15	mA
IRM	12	Maximum Current by Pin REG				3.5	mA

CHROMINANCE C

C _{ppm}	22	Peak to Peak Amplitude	Referred on burst period (blue lines in SECAM)	15	150	300	mV
Ze22	22	Input Impedance		4	7		kΩ

CVBS INPUT

YC	24	Peak to Peak Amplitude	Standard bar pattern 75%		500	700	mV
SC	24	Subcarrier Amplitude	Referred on burst period (blue lines in SECAM)	15	150	300	mV
Ze24	24	Input Impedance		4	6.8		kΩ

B-Y/R-Y OUTPUT SIGNALS

R-Y	6	R-Y Amplitude	Color bar pattern 75% Burst amplitude 150mV Burst gate duration 4µs	0.7	1	1.41	V
B-Y	7	B-Y Amplitude		0.84	1.2	1.7	V
Tr1	6 / 7	R-Y B-Y Rising Time PAL G Mode	Color bar pattern 75% PAL G		600	700	nS
Tr2	6 / 7	R-Y B-Y Rising Time SECAM Mode	Color bar pattern 75% SECAM		650	1000	nS
Tr3	6 / 7	R-Y B-Y Rising Time PAL M & NTSC 3.58 Mode	Color bar pattern 75% PAL M & NTSC 3.58		850	1000	nS
FRHF0	6 / 7	Residual HF Signal at F0	Color bar pattern 75% Burst amplitude 150mV All standards			15	mV _{PP}
FRHF20	6 / 7	Residual HF Signal at 2F0				15	mV _{PP}
FRHF3	6 / 7	Residual HF Signal at 3MHz				15	mV _{PP}
BOFF	6 / 7	Blanking Offset	All standards	-20		20	mV
RBYRY	6 / 7	Ratio B-Y/R-Y	Nominal input	1.14	1.2	1.26	
DG	6 / 7	Differential Gain of the Delay Line	SECAM mode color bar pattern 75%	-6		6	%
DCUVP	24/6/7	Delay between CVBS and B-Y/R-Y in PAL Mode			520		nS
DCUVS	24/6/7	Delay between CVBS and B-Y/R-Y in SECAM Mode			500		nS

2151-02.TBL

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Pin N°	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	--------	-----------	-----------------	------	------	------	------

GENERAL CONDITIONS (Continued)

DCUVN	24/6/7	Delay between CVBS and B-Y/R-Y in NTSC Mode			520		nS
DCYS	24/20	Delay between CVBS and Y in SECAM Mode			90		nS
DCYP	24/20	Delay between CVBS and Y in PAL Mode			90		nS
DCYN	24/20	Delay between CVBS and Y in NTSC Mode			90		nS

BELL FILTER

F0		Tuning Frequency	Nominal value	-20	4286	+20	kHz
DF		Maximum BUS Shift	Shift of the central frequency compared with the nominal value		+100		kHz
ST		Minimum Shift Step			7		kHz
QB		Quality Coefficient	Width external resistor 8.2k Ω	14	16	18	

BAND PASS FILTER

F0PB		F0 PAL 4.43		-100	4433	+100	kHz
F0N1		F0 NTSC 4.43		-100	4433	+100	kHz
F0PM		F0 PAL 3.58		-100	3579	+100	kHz
F0N2		F0 NTSC 3.58		-100	3579	+100	kHz
Q		Quality Coefficient		2.5	3.0	3.5	

ACC

GD		Gain Dynamic		-6		+20	dB
REFV	24/22	0 dB Reference Voltage	Burst amplitude on standard PAL bar pattern 75%		150		mV _{PP}
AREG	6 / 7	Amplitude Regulation	Burst amplitude at the input changing from 15 to 300mV _{PP} on PAL bar pattern. Measured on output R-Y/B-Y.	-3	0	+3	dB
INTC		Internal Time Constant		5		8	mS

HUE CONTROL

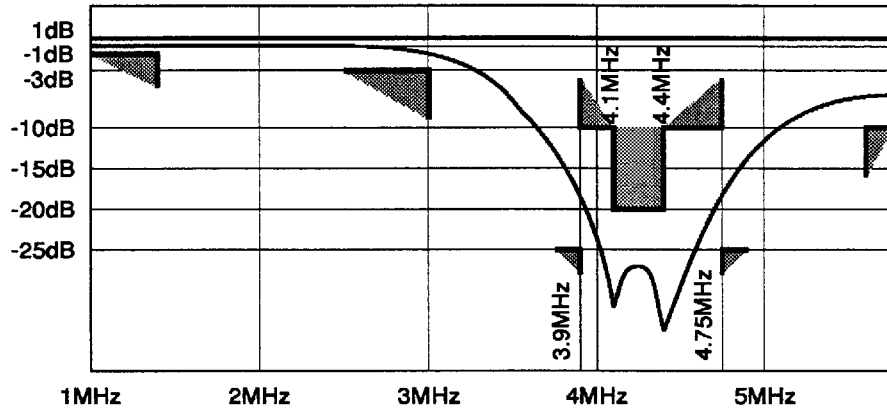
MADP		Maximum Value of Phase Change	BUS controlled	+20	+30	+40	°
MIDP		Minimum Value of Phase Change	BUS controlled	-20	-30	-40	°
MSTP		Maximum Step			1.9		°

VCO FOR PAL

PCR		Positive Catching	f _{q0} = quartz frequency See quartz specification	f _{q0} +450			Hz
NCR		Negative Catching	f _{q0} = quartz frequency See quartz specification	f _{q0} -450		-900	Hz
PH		Phase Hold				0.04	°/Hz
PHO		U axes/f0 Phase Offset		-5		7	°
QER		Quadrature Error		-5		5	°

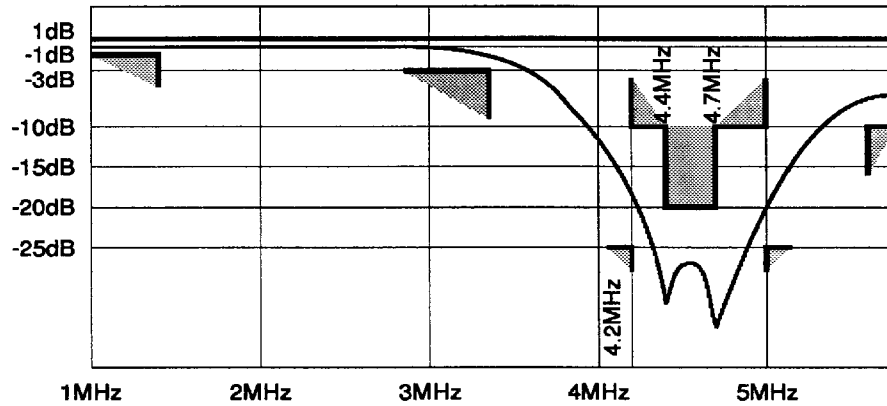
2151-03.TBL

Figure 1 : SECAM Trap Filter Frequency Response
 (Maximum group delay time at 3.9MHz : 240ns (typical 220ns))



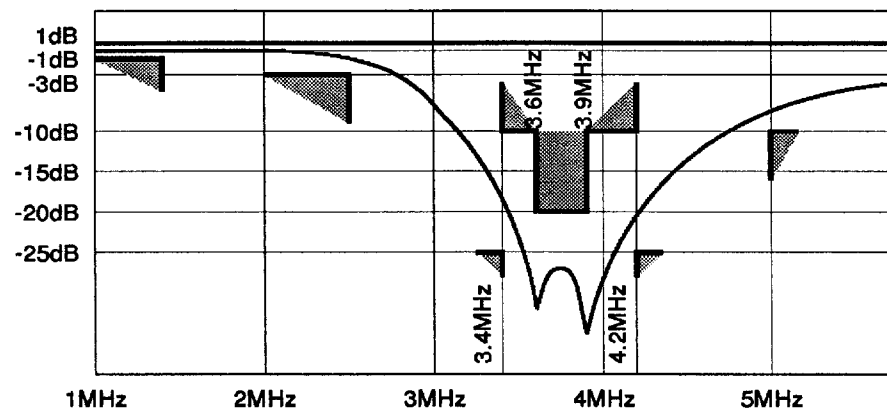
2151-04.EPS

Figure 2 : PAL Trap Filter Frequency Response
 (Maximum group delay time at 3.9MHz : 240ns (typical 220ns))



2151-05.EPS

Figure 3 : NTSC 3.58 Trap Filter Frequency Response



2151-06.EPS

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Pin N°	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DEEMPHASIS SECAM							
FD		Cut-off Frequency		-15%	85	+15%	kHz
ATT		Attenuation		-9	-9.54	-10	dB
TDR		Temperature Drift		-2%		+2%	

TRAP FILTER

SFR	20	SECAM Frequency Response	See Figure 1				
PFR	20	PAL Frequency Response	See Figure 2				
NFR	20	NTSC Frequency Response	See Figure 3				
ZOT	20	Output Impedance	CVBS or SVHS mode			400	Ω
YG	20	Y Output Gain	Referred to CVBS input signal $F_{req} < 1\text{MHz}$	-1	0	1	dB
YOFF	20	Y Output DC Offset in SVHS	Referred to CVBS mode			0.2	V
YDC	20	Y Output DC Level		2	2.5	4	V

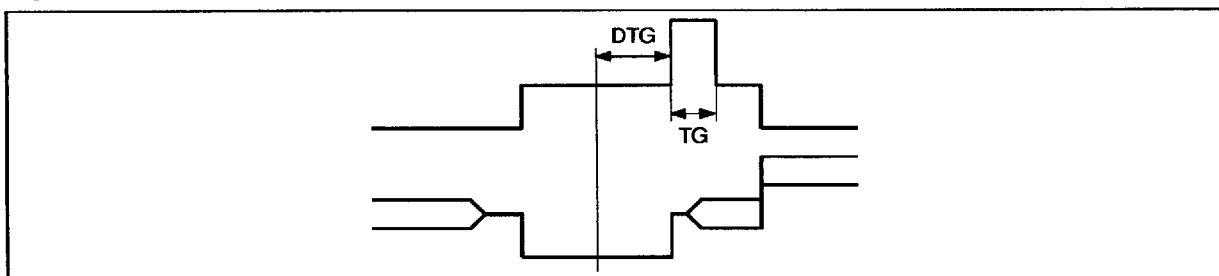
SUPER SAND CASTLE DETECTOR

FR	10	Blanking Threshold		0.5	0.75	0.9	V
LR	10	Line Threshold		1.6	1.8	1.9	V
BG	10	Burst Gate Threshold		3.2	3.5	3.8	V
FBD	10	Frame Blanking Duration		1.3		1.5	ms
TG	10	Burst Gate Duration	See Figure 4	3.7	4	4.3	μs
DTG	10	Delay between Middle of Sync Pulse and Leading Edge of the Burst Gate Pulse		2.5		3.1	μs

CRYSTAL DATA

		Frequency Tolerance	At 25°C			30	ppm
		Frequency Tolerance	From 0 to 70°C			50	ppm
		F0 for PAL G and NTSC 4.43	Serial mode	4.433619			MHz
		F0 for PAL M	Serial mode	3.575611			MHz
		F0 for NTSC 3.58	Serial mode	3.579545			MHz

2151-03.TBL

Figure 4

2151-07.EPS

I²C BUS INTERFACE DESCRIPTION

The 2-wires serial interface of the I²C bus uses a clock line (CLOCK) and a data line (DATA). Both lines work bidirectionally.

The I²C bus protocol prescribes a full-byte transmission.

In this I²C bus circuit the first byte after the start condition is used to transmit only the IC-address (7 bits) and read/write-bit.

- WRITE MODE : R/W = 0

In write mode the second byte contains the sub-address of the addressed latch and the third byte the data belonging to it.

Two modes are possible :

- Stopping the transmission by sending the stop-condition.
- Incrementing the sub-address by sending one or more additional data bytes.

- READ MODE : R/W = 1

In read mode the second and third byte contain information from the IC.

I²C BUS FORMAT

IC-ADDRESS STV2151										SUB-ADDRESS							DATA											
S	1	0	0	0	1	a	1	R/W	A	s1	s2	X	X	X	X	X	X	A	d8	d7	d6	d5	d4	d3	d2	d1	A	E
1ST BYTE										2ST BYTE							3RD BYTE											

S : Start

A : Acknowledge

E : End/stop

a : 0 or 1 according to Pin 21 biasing

s1, s2 : Sub addresses

All transmission with MSB first.

INPUT BYTES

R/W = 0

SUB-ADDRESS								DATA							
S1	S2	X	X	X	X	X	X	d8	d7	d6	d5	d4	d3	d2	d1
0	0	X	X	X	X	X	X	BT4	BT3	BT2	BT1	BS2	60HZ	BS4	1
0	1	X	X	X	X	X	X	FKILL	MKILL	HC5	HC4	HC3	HC2	HC1	BELLEN
1	0	X	X	X	X	X	X	FSTD	FSVHS	SHB3	SHB2	SHB1	SHB0	1	1
2ST BYTE								3RD BYTE							

Bus Controlled Adjustment

Symbol	Pin N°	Parameter	BUS Setting
HC1..HC5		Hue Control	HC1 : LSB HC5 : MSB
SHB0.. SHB3		Bell Filter Shift	SHB0 : LSB SHB3 : MSB

Bus Controlled Switches

Symbol	Pin N°	Parameter	BUS Setting
FSTD		Standard Selection Mode	Auto mode : FSTD = 0 Manual mode : FSTD = 1
FKILL		Killer Mode	Auto by ident bit : FKILL = 0 Forced by MKILL : FKILL = 1
MKILL		Killer Status	B&W : MKILL = 0 Color : MKILL = 1
SVHS		CVBS / SVHS Selection	CVBS mode : SVHS = 0 SVHS mode : SVHS = 1
BS2 60Hz BS4		Standard Selection Bits	See Table 1
bt1 bt2 bt3 bt4	14	Test pin Selection Bits	See Table 3
BELLEN		Bell Filter Calibration on/off	BELLEN = 1 → calibration refresh BELLEN = 0 → no calibration refresh

STANDARD SELECTION**Table 1 : Input Bits**

	BS2	60Hz	BS4
SECAM	0	0	0
PAL BG	1	0	0
NTSC 3.58	0	1	0
PAL M	0	1	1
NTSC 4.43	1	1	1

Table 2 : Output Bits

	IS10	IS11	IS12
SECAM	0	0	0
PAL BG	1	0	0
NTSC 3.58	0	1	0
PAL M	0	1	1
NTSC 4.43	1	1	1

Table 3 : Test Pin

	BT1	BT2	BT3	BT4
High Impedance	0	0	0	0
V = 7V±0.5V, Z0 < 2kΩ	1	1	1	1

STV2151

OUTPUT BYTES

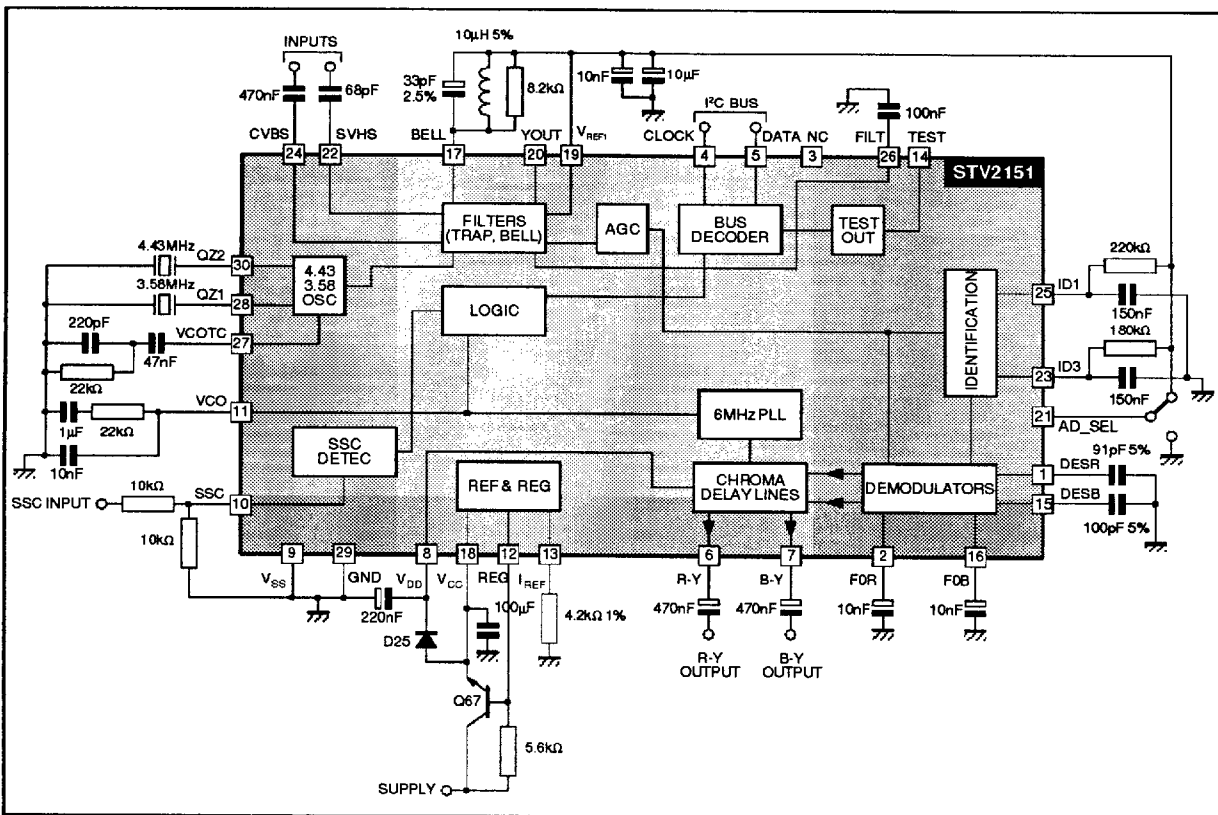
R/W = 1

DATA							
d8	d7	d6	d5	d4	d3	d2	d1
IDENT	IS10	IS11	IS12	X	X	X	X
2ST BYTE							

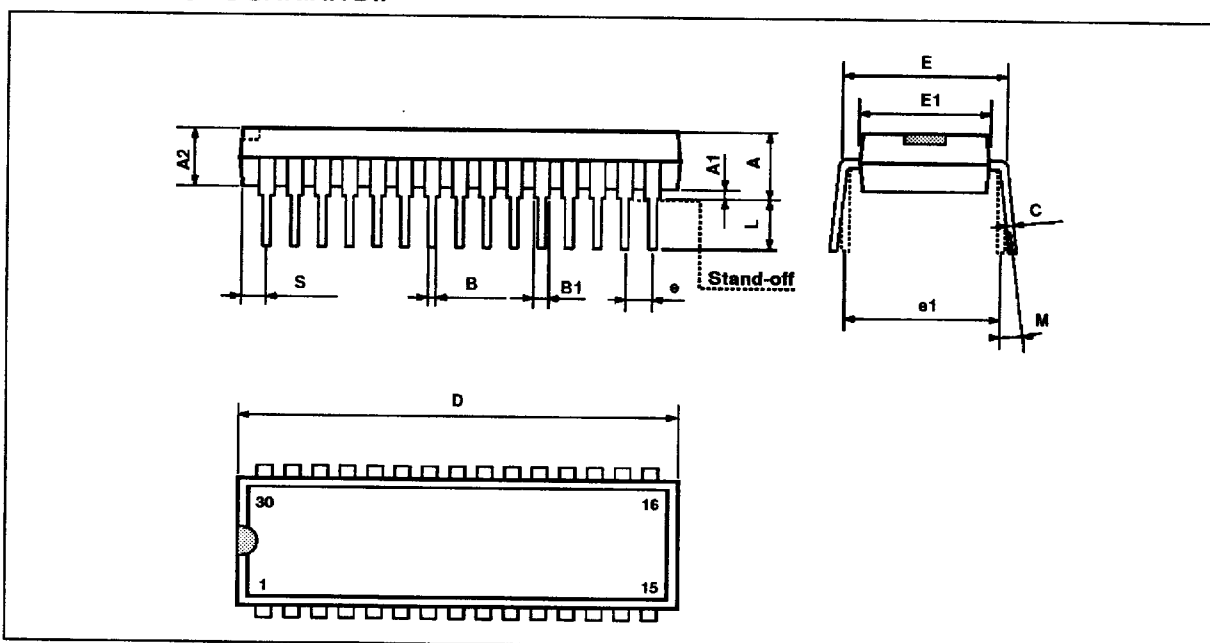
RECOMMENDED BIT CONFIGURATIONS DURING INITIALIZATION

BT1 = 0	SVHS = 0	FKILL = 0	FSTD = 0
BT2 = 0		MKILL = 0	BELLEN = 1
BT3 = 0	HC1 = 0		SHBO = 0
BT4 = 0	HC2 = 0		SHB1 = 0
BS2 = not def	HC3 = 0		SHB2 = 0
60Hz = 0	HC4 = 0		SHB3 = 0
BS4 = not def	HC5 = 1		

TYPICAL APPLICATION



2151-02EPS

PACKAGE MECHANICAL DATA
30 PINS - PLASTIC SHRINK DIP


PMSDIP30.EPS

SDIP30.TBL

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.78			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0° (min.), 15° (max.)					
S	0.31			0.012		

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No licence is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1995 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of μ C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips μ C Patent. Rights to use these components in a μ C system, is granted provided that the system conforms to the μ C Standard Specifications as defined by Philips.

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.