SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$	0,15 to 1	V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

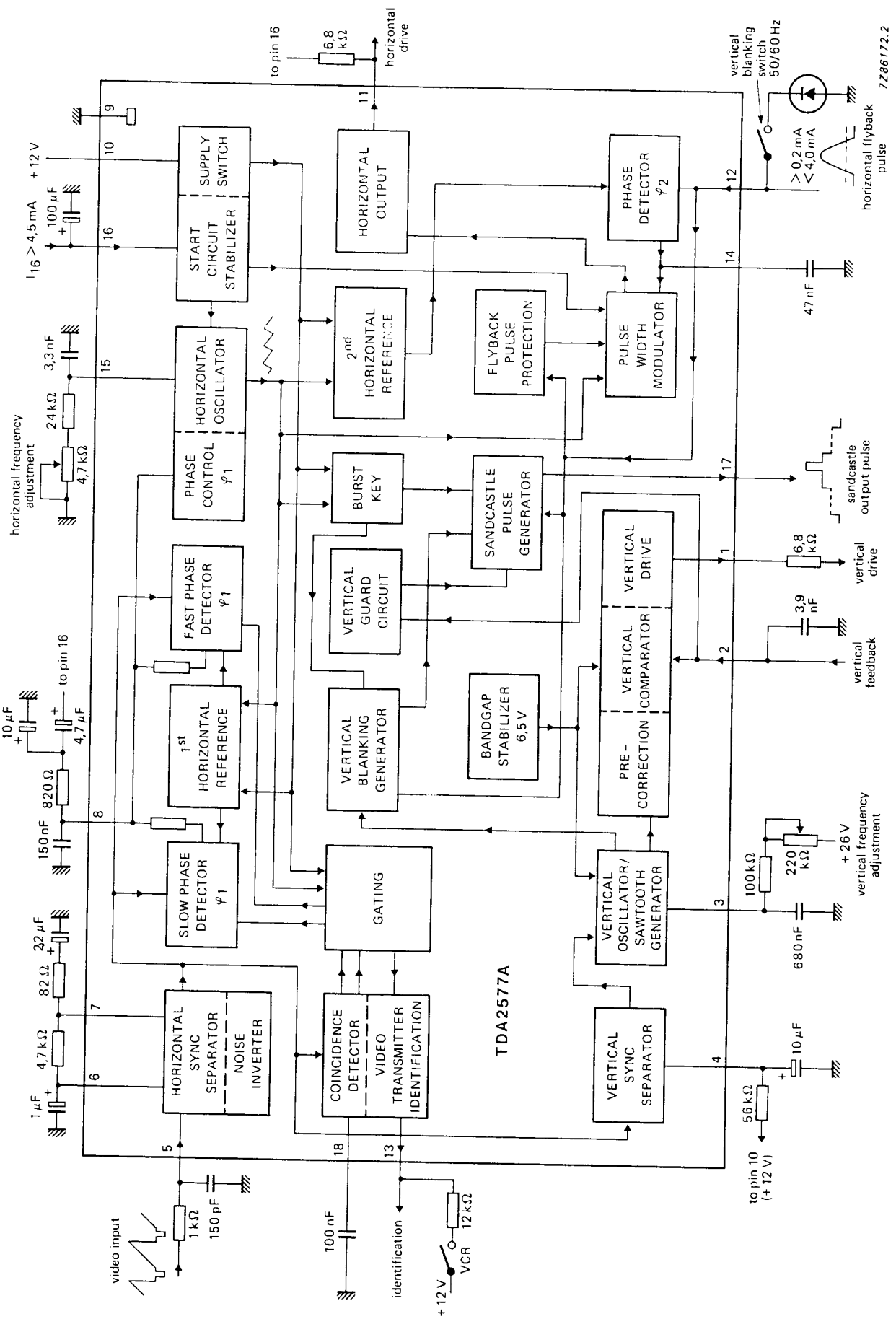

Fig. 1 Block diagram.

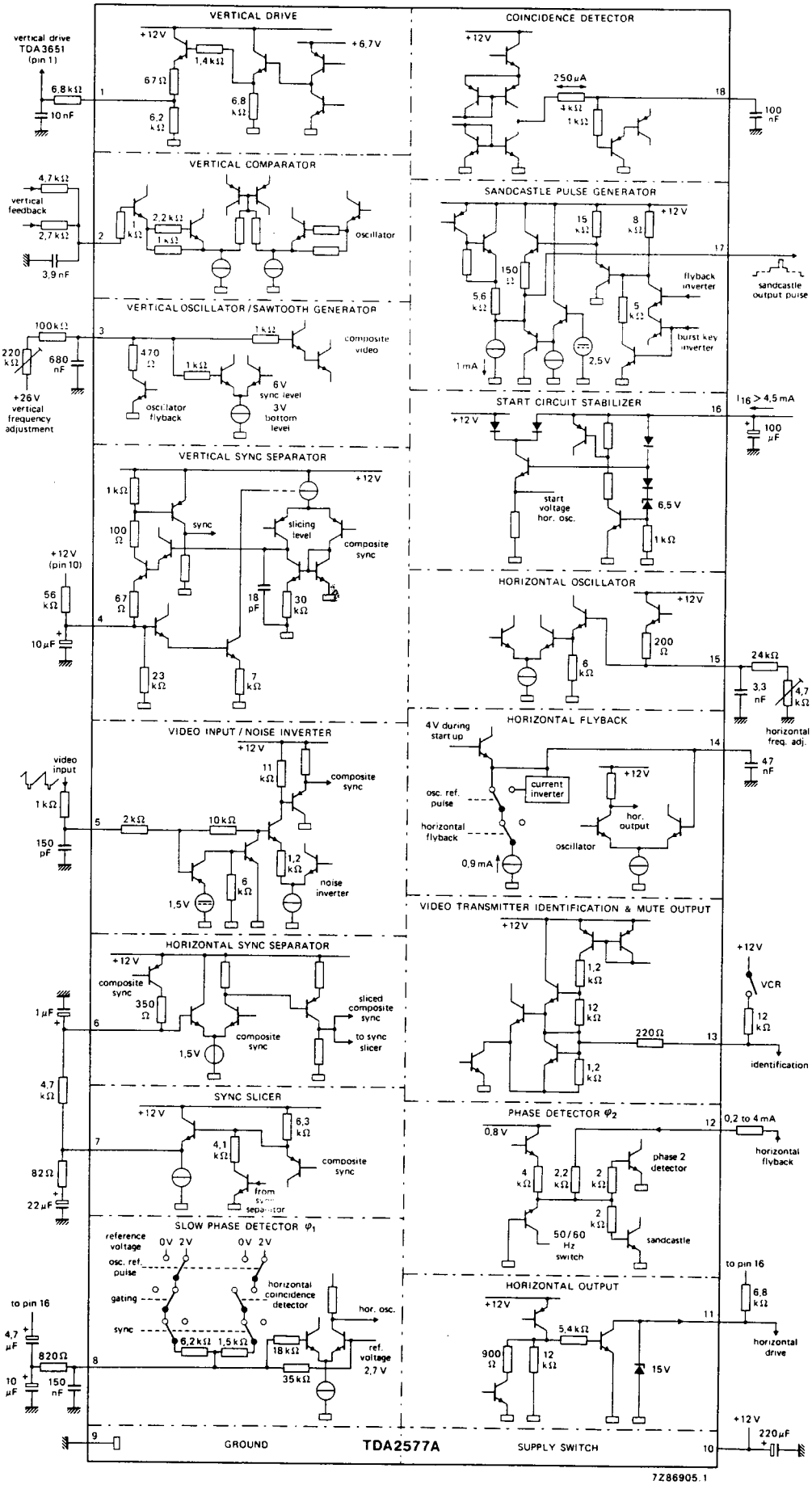

Fig. 2 TDA2577A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,1 W
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 65 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50 K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8 mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7 V
			8,0 to 9,5 V
Supply current (pin 10)	I_{10}	typ.	55 mA
		<	70 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
			10 to 13,2 V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1 V
			1,5 to 3,75 V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6 V
			0,15 to 1 V
Slicing level		typ.	50 %
			35 to 65 %
Delay between video input and detector output	t_1	typ.	0,35 µs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7 V
		<	1 V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800 Hz
Catching range	Δf	typ.	± 800 Hz
			±600 to ± 1100 Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse			
for slow time constant		typ.	1 kHz/µs
for fast time constant		typ.	2,75 kHz/µs

Second control loop (horizontal output to flyback; pin 14)			
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400 μs/μs
Control range	t_d		1 to 50 μs
Controlled edge	negative		
Phase adjustment (via 2nd control loop; pin 14)			
Control sensitivity		typ.	25 μA/μs
Maximum permissible control current	$\pm I_{14}$	<	60 μA
Horizontal oscillator (pin 15)			
Frequency (no sync)	f_{osc}	typ.	15 625 Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ)	Δf_{osc}	<	4 %
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 % 8 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Horizontal output (pin 11)			
Output voltage; high level	V_{11-9}	<	13,2 V
Voltage at which protection starts	V_{11-9}		13 to 15,8 V
Output voltage; low level			
start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 V 0,5 V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 V 0,5 V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65 %
Duty factor of output signal without flyback pulse	δ	typ. 	50 % 47 to 57 %
Controlled edge	negative		
Duration of output pulse (see Fig. 3)			$t_d + t_o + 2{,}5$ μs
Sandcastle output pulse (pin 17)			
Output voltage during:			
burst key	V_{17-9}	>	10 V
horizontal blanking	V_{17-9}	typ. 	4,6 V 4,2 to 5 V
vertical blanking	V_{17-9}	typ. 	2,5 V 2 to 3 V
Pulse duration			
burst key	t_p	typ. 	3,7 μs 3,3 to 4,1 μs
horizontal blanking	flyback pulse (see note 3)		
vertical blanking			
for 50 Hz application ($-I_{12}$: 0 to 0,1 mA)			21 lines
for 60 Hz application ($-I_{12}$: typ. 0,2 mA)			17 lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	5,2 μs
			4,8 to 5,6 μs
Delay between the start of the sync and the trailing edge of the burst key	t_2	typ.	8,8 μs
			8,1 to 9,3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ.	3,5 V
			3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1,2 V
			1,0 to 1,4 V
vertical period counter 3 periods fast	V_{18-9}	typ.	0,12 V
			0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1,7 V
			1,5 to 1,9 V
Switching level fast to slow (locking)	V_{18-9}	typ.	5,0 V
			4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8,6 V
			8,2 to 9,0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	>	10 V
		typ.	11 V
Output voltage active (no sync) at I_{13} = 5 mA	V_{13-9}	>	7 V
		typ.	10 V
Output voltage inactive	V_{13-9}	<	0,5 V
		typ.	0,1 V
VCR switching (pin 13)			
Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ.	0,6 mA
			0,4 to 0,8 mA
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Duration of vertical blanking pulse (pin 12)

Required input current (negative)			
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0,2 mA
		> 0,15 to < 0,3	mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	<	0,1 mA
Maximum allowed input current	$-I_{12}$	<	0,4 mA

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	<	4 %
Synchronization range		typ.	22 %
Input current at V_{3-9} = 6 V	I_3	<	2 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1,5 V
Input current at V_{2-9} = 6 V	I_2	<	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	<	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)

switching level low	V_{2-9}	typ.	3 V
			2,7 to 3,3 V
switching level high	V_{2-9}	typ.	5,8 V
			5,4 to 6,3 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

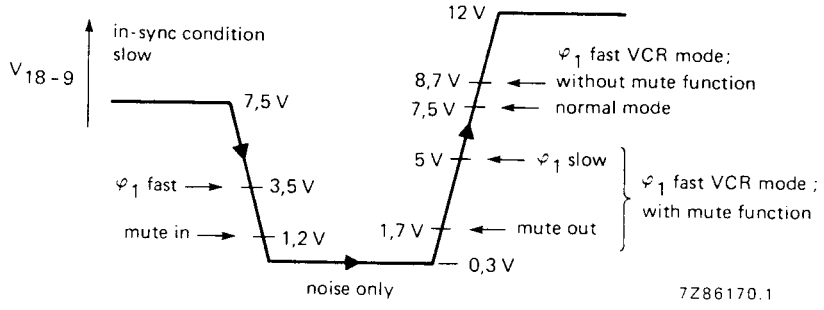

Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,8 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays

in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

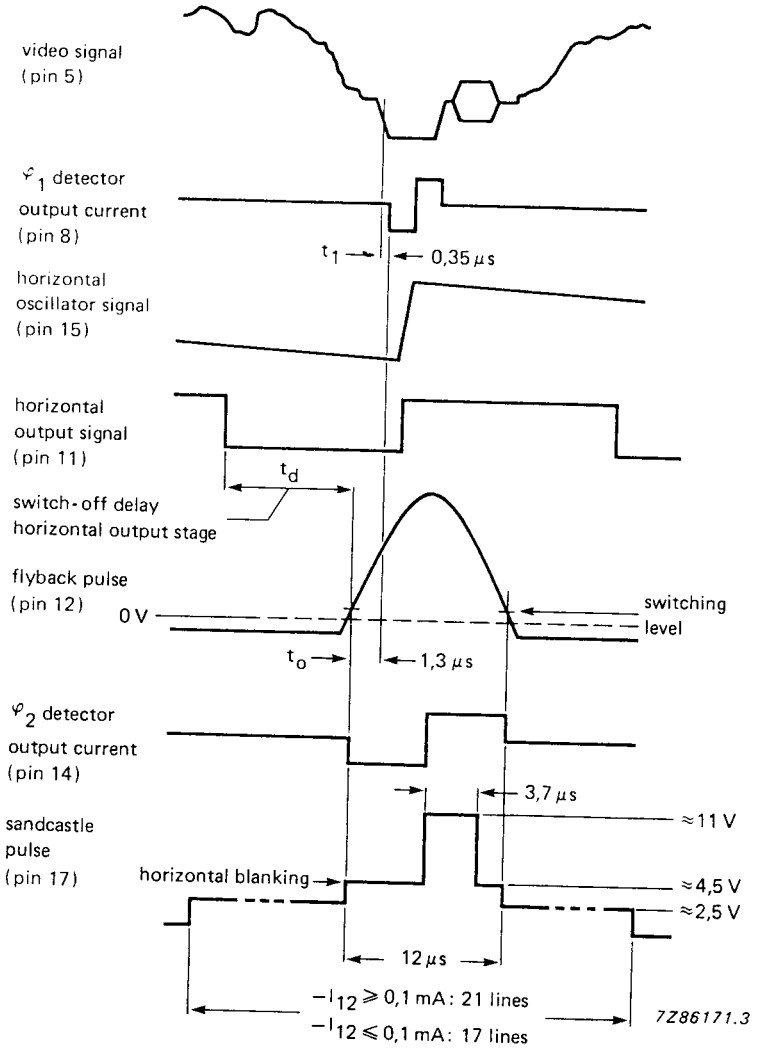

Fig. 4 Timing diagram of the TDA2577A.

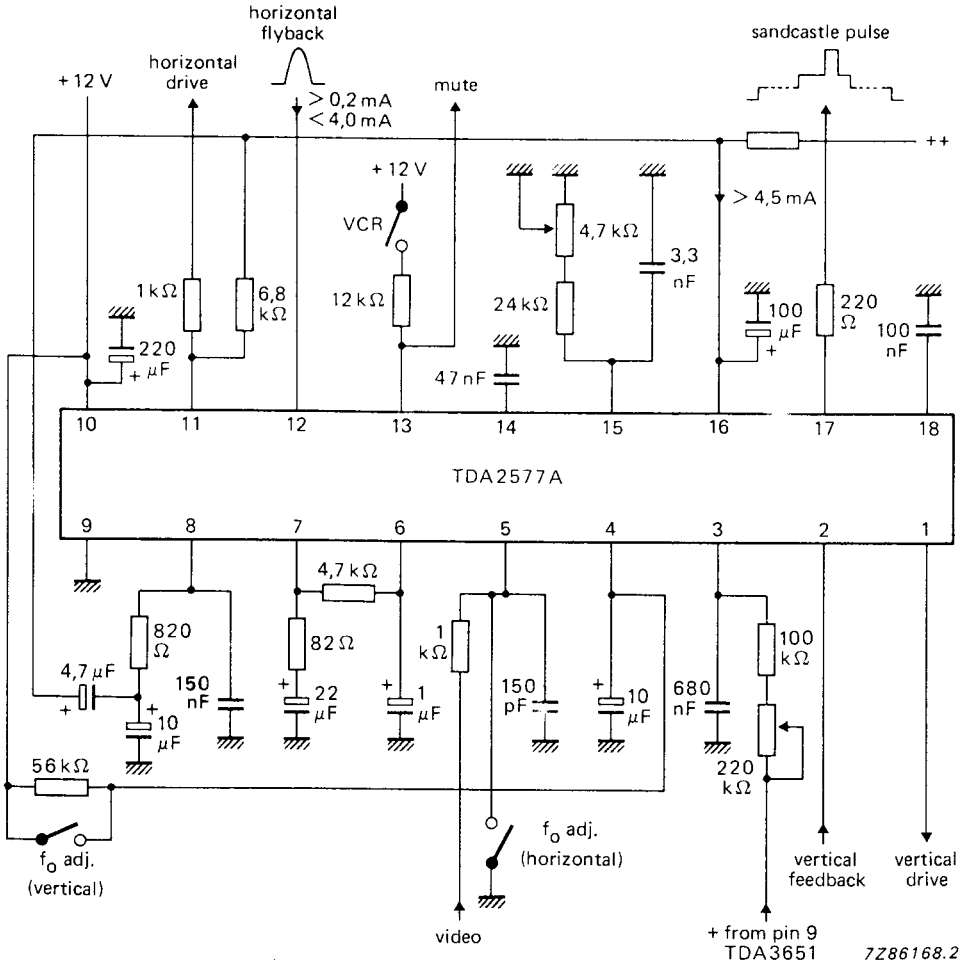

Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

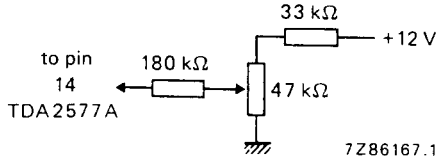

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

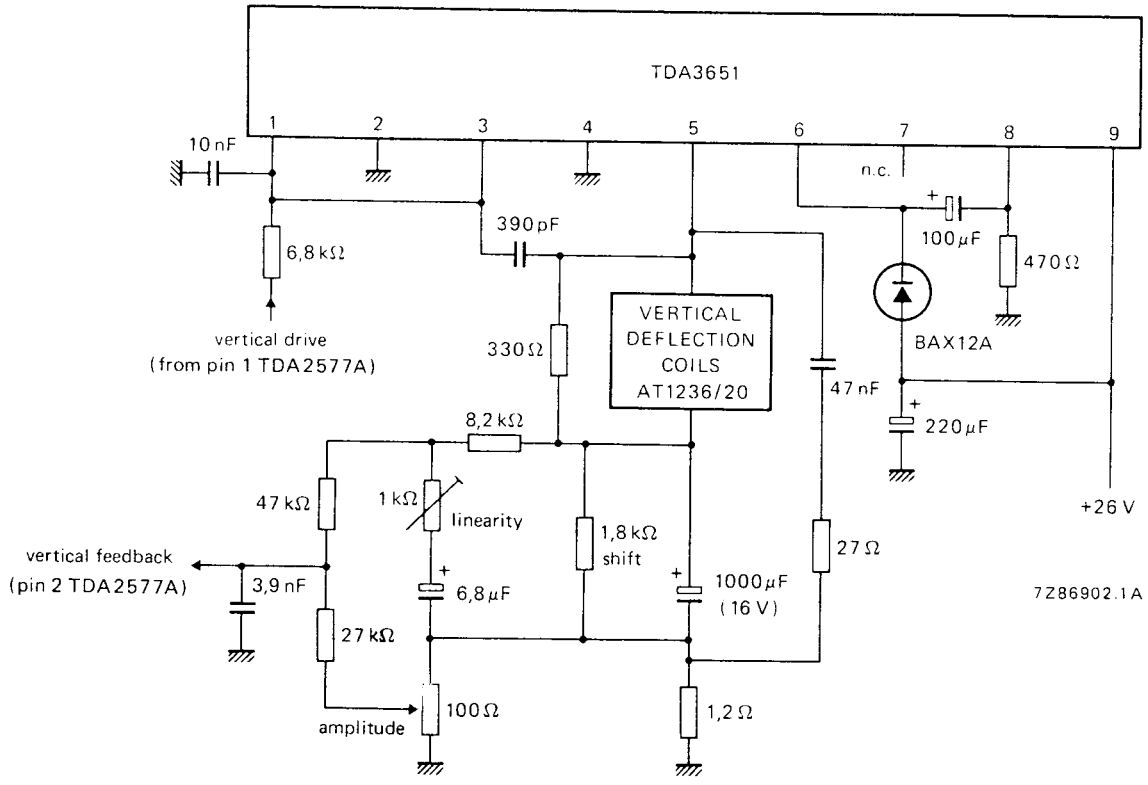

Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).