



## APC5890 DE-COMPRESSION VOICE IC

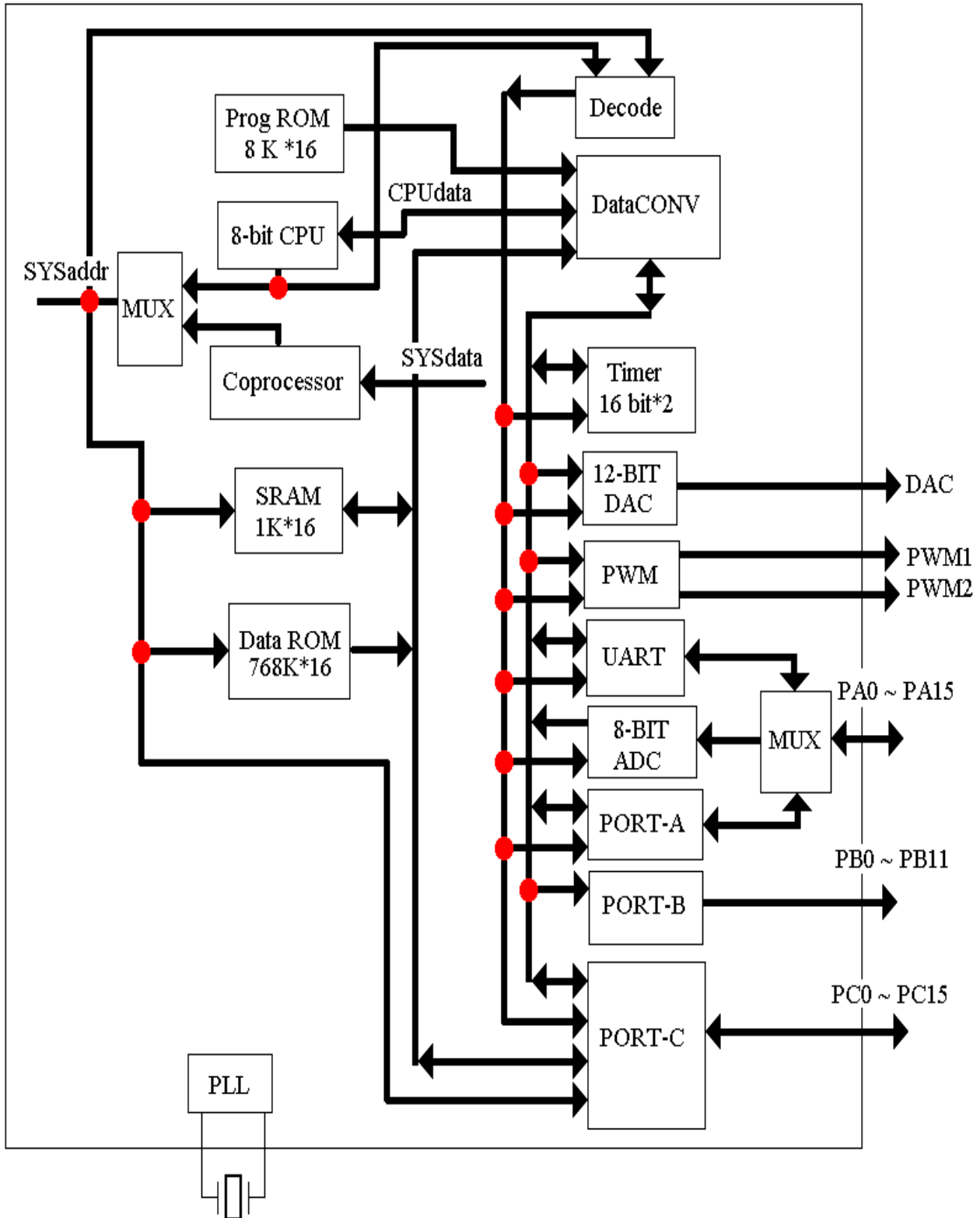
### 1. CHIP FEATURES.

- DUAL OPERATION FREQUENCIES:
  - 32.768 KHz & 0.5 SECOND TIMER INTERRUPT.
  - BUILT-IN PLL CIRCUIT TO GENERATE SYSTEM CLOCK MAX 20MHz.
- BUILT-IN 2KBYTES(1K\*16) RAM.
- ADDRESS UP TO 8MBYTE(4M\*16) RAM OR ROM OR “ROM AND RAM”  
BUILT-IN 16KBYTE(8K\*16) PROGRAM ROM AND **1.5M BYTE(768K\*16) DATA ROM**
- **BUILT-IN DECOMPRESSION ENGINE**  
THE VOICE AND MUSIC DE-COMPRESSON RATE IS AS THE FOLLOWS:
  - 2.25KBIT/SEC - 2.7KBIT/SEC - 3.15KBIT/SEC - 3.6KBIT/SEC - 4.8KBIT/SEC - 6.0KBIT/SEC
  - 7.2KBIT/SEC - 8.4KBIT/SEC - 9.6KBIT/SEC - 10.8KBIT/SEC - 12.0 KBIT/SEC - 13.2 KBIT/SEC
  - 14.4 KBIT/SEC

| DE-COMPRESSON RATE | VOICE DURATION | DE-COMPRESSON RATE | VOICE DURATION |
|--------------------|----------------|--------------------|----------------|
| 2.25 K BIT/SEC     | 91 min.        | 8.4 K BIT/SEC      | 24.38 min.     |
| 2.7 K BIT/SEC      | 75.85 min.     | 9.6 K BIT/SEC      | 21.33 min.     |
| 3.15 K BIT/SEC     | 65.01 min.     | 10.8 K BIT/SEC     | 18.96 min.     |
| 3.6 K BIT/SEC      | 56.89 min.     | 12.0 K BIT/SEC     | 17.07 min.     |
| 4.8 K BIT/SEC      | 42.67 min.     | 13.2 K BIT/SEC     | 15.52 min.     |
| 6.0 K BIT/SEC      | 34.13 min.     | 14.4 K BIT/SEC     | 14.22 min.     |
| 7.2 K BIT/SEC      | 28.44 min.     |                    |                |

- BUILT-IN 12 BITS D/A, 8 BITS ADC.
- I/O PORTS
  - 16 I/O PINS FOR PORT A.
  - 12 OUTPUT FOR PORT B.
  - 16 I/O PINS FOR PORT C.
- TWO 16BITS TIMERS : TIMER\_A AND TIMER\_B.
- WATCHDOG TIMER.
- SLEEP MODE : CRYSTAL & SYSTEM

## 2. BLOCK DIAGRAM.



## 2. PIN DESCRIPTION :

| PIN NAME            | I/O | DESCRIPTION  |
|---------------------|-----|--|
| RESET               | I   | RESET INPUT. ACTIVE LOW.   |
| PWM1,PWM2           | O   | PWM OUTPUT.  |
| DAC                 | O   | OUTPUT FROM D/A CONVERTER.   |
| XOSC1               | I   | CRYSTAL OSCILLATOR INPUT PIN.  |
| XOSC2               | O   | CRYSTAL OSCILLATOR OUTPUT PIN.   |
| CAP                 | I   | CAPACITOR FOR PLL CIRCUIT.   |
| PA0-PA7             | I/O | I/O PORT_A PIN 0 TO 7.<br>ALSO AS EXTERNAL INTERRUPT SOURCE<br>(FALL EDGE TRIGGER).  |
| PA8-PA12            | IO  | I/O PORT_A PIN 8 TO 12.  |
| PA13/ADC            | I/O | I/O PORT_A PIN 13 OR ANALOG SIGNAL INPUT.  |
| PA14                | I/O | I/O PORT_A PIN 14  |
| PA15                | I/O | I/O PORT_A PIN 15  |
| PB0-PB5/BANK3-BANK8 | O   | PORT_B OR EXTERNAL MEMORY BANK SELECT  |
| PB6/EMEMRD          | O   | PORT_B PIN 6 OR EXTERNAL RAM READ<br>(ACTIVE LOW).   |
| PB7/EXTRAM          | O   | PORT_B PIN 7 OR EXTERNAL RAM SELECT PIN<br>(ACTIVE LOW)  |
| PB8/EMEMWRL         | O   | PORT_B PIN 8 OR EXTERNAL RAM LOW BYTE WRITE<br>(ACTIVE LOW).   |
| PB9/EXTIRQ          | I/O | PORT_B PIN 9 OR EXTERNAL IRQ INPUT PIN<br>(RISE EDGE TRIGGER).   |
| PB10/EMEMWRH        | O   | PORT_B PIN 10 OR EXTERNAL RAM HIGH BYTE WRITE<br>(ACTIVE LOW)  |
| PB11/EXTROMCS       | I/O | PORT_B PIN 11 ROM SELECT OR EXTERNAL ROM CHIP<br>SELECT (ACTIVE LOW)   |
| PC/EMEMAD           | I/O | PC: 16 BITS PROGRAMMABLE IO PORTS.<br>EMEMAD: EXTERNAL MEMORY ADDRESS/DATA.<br>IF IT IS ADDRESS THEN<br>EMEMA0~EMEMA12 IS A1~A13.<br>EMEMA13~EMEMA15 IS BANK0~BANK2. |
| ALE                 | O   | EXTERNAL MEMORY ADDRESS LATCH ENABLE.  |
| VDD1-VDD4           | I   | DIGITAL POWER INPUT.   |
| GND1-GND4           | I   | DIGITAL GROUND.  |
| PLLVDD,PLLGND       | I   | POWER AND GROUND FOR PLL CIRCUIT.  |
| DACVDD,DACGND       | I   | POWER AND GROUND FOR DAC CIRCUIT.  |

#### 4. ADDRESS ARRANGEMENT :

1) RAM :

0000-07FF : INTERNAL RAM, 1Kx16.

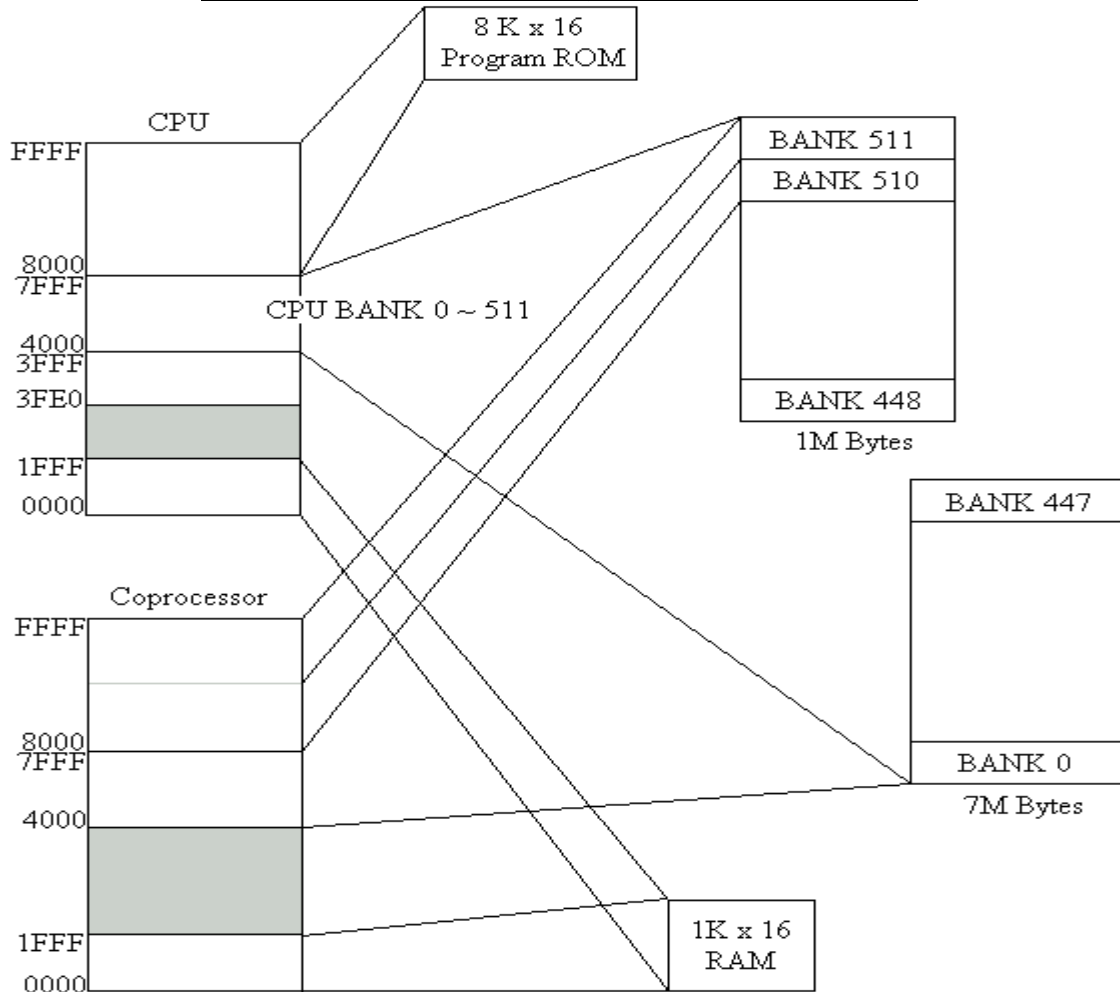
0000-1FFF : EXTERNAL NON-BANK RAM(EXTRAMCS=1), 4Kx16.

2) ROM :

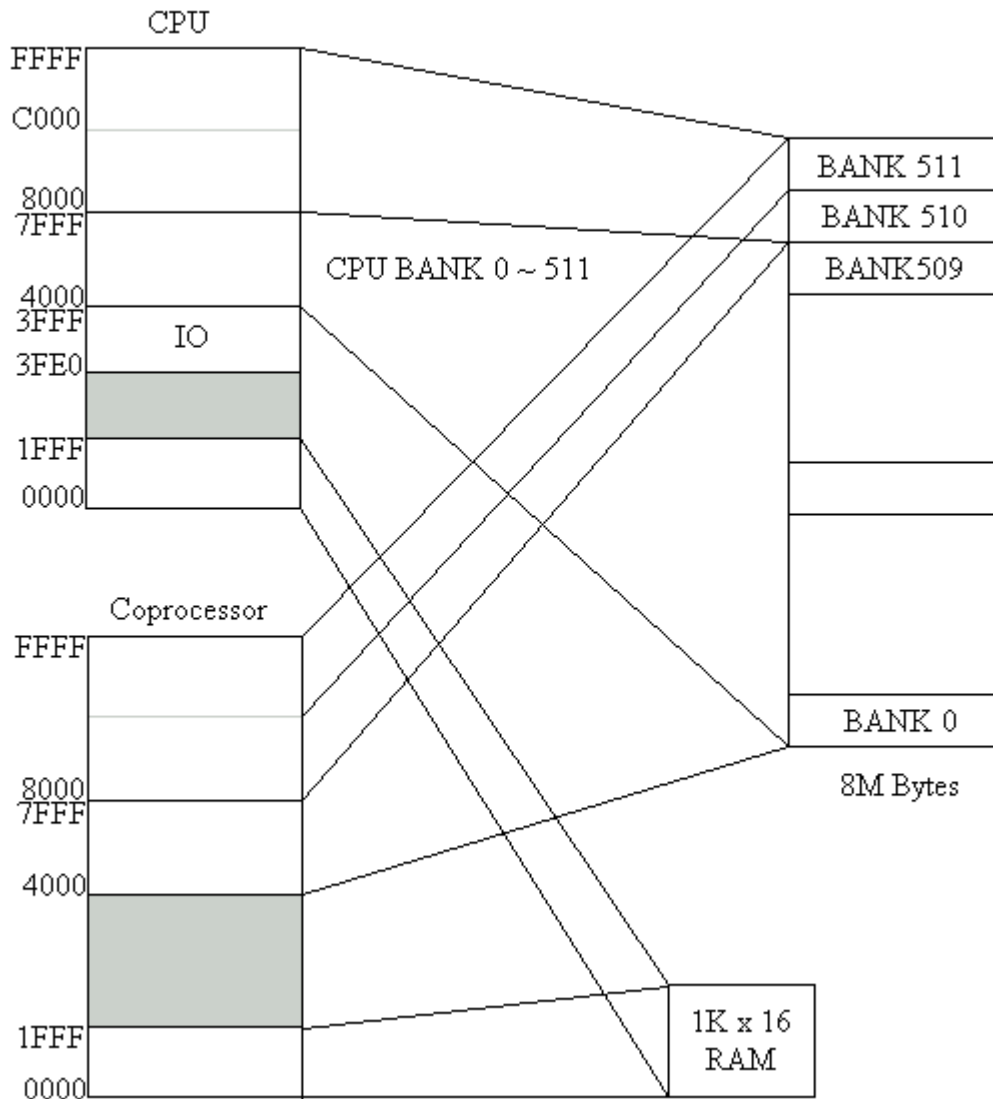
- 4000-7FFF : DATA AREA FOR BANK SELECT, 8Kx16 EACH,  
MAX. TO 64MBIT BANK ROM OR BANK RAM.
- C000-FFFF : FOR SYSTEM PROGRAM OR USER PROGRAM, 8Kx16.
- FFF0, FFF1 : COPROCESSOR OK IRQ VECTOR.
- FFF2, FFF3 : ADC IRQ VECTOR.
- FFF4, FFF5 : NOT USE
- FFF6, FFF7 : TIMER IRQ(FIX\_TIMER IRQ OR TIMER\_A IRQ) VECTOR.
- FFF8, FFF9 : PA[7:0] IRQ VECTOR.
- FFFA, FFFB : TIMER\_B NMI VECTOR.
- FFFC, FFFD : RES VECTOR.
- FFFE, FFFF : EXT IRQ VECTOR.

PRIORITY IS ARRANGED AS RES, NMI, OK\_INT, ADC\_INT, TIMER\_INT, PA\_INT, AND EXT\_IRQ.

**MEMORY MAPPING ( INTERNAL ROM )**



## MEMORY MAPPING ( EXTERNAL ROM )



### 3) Others :

- 3FE0 System Flag. Read only. :

| 3FE0    | 0                       | 1                |                     |
|---------|-------------------------|------------------|---------------------|
| BIT - 0 | NO USE                  | NO USE           |                     |
| BIT - 1 | NO USE                  | NO USE           |                     |
| BIT - 2 | ADC NO ERROR.           | ADC ERROR.       |                     |
| BIT - 3 | TIMER_A INT FLAG        |                  |                     |
|         | TIMER IRQ               | TIMER_A INT FLAG |                     |
|         | 1                       | 1                | ..... TIMER_A INT   |
|         | 1                       | 0                | ..... FIX_TIMER INT |
|         | 1                       | X                | ..... NO TIMER INT  |
| BIT - 4 | NO USE                  |                  |                     |
| BIT - 5 | OK FLAG(COPROCESSOR OK) |                  |                     |

|         |  |                        |
|---------|--|------------------------|
| BIT - 6 |  | COPROCESSOR CARRY.     |
| BIT - 7 |  | TONE0 OR TONE1 ENABLE. |

● **3FE0 System control 0. Write only. :**

| 3FE0    | 0  | 1                            |
|---------|--|------------------------------|
| BIT - 0 | MUST 0 = PA14,PA15 ARE IO PINS(DEFAULT). |                              |
| BIT - 1 | PB9 IS IO PIN(DEFAULT).                  | PB9 IS EXTIRQ PIN.           |
| BIT - 2 | PB7 IS IO PIN(DEFAULT).                  | PB7 IS EXTRAMCS.             |
| BIT - 3 | ADC DISABLE, PA13 IS IO PIN(DEFAULT).    | ADC ENABLE, PA13 IS ADC PIN. |
| BIT - 4 | NO USE(MUST 0)                           |                              |
| BIT - 5 | NO USE(MUST 0)                           |                              |
| BIT - 6 | PWM DISABLE(DEFAULT).                    | PWM ENABLE.                  |
| BIT - 7 | DAC DISABLE(DEFAULT).                    | DAC ENABLE.                  |

● **3FE1 System Control 1. Write only.**

| 3FE1    | 0   | 1                                  |
|---------|---|------------------------------------|
| BIT - 0 | TIMER A CLOCK SELECT 32.768k Hz.(DEFAULT) | TIMER A CLOCK SELECT SYSTEM CLOCK. |
| BIT - 1 | NO USE(MUST 0)                            |                                    |
| BIT - 2 | TIMER A DISABLE.(DEFAULT)                 | TIMER A ENABLE.                    |
| BIT - 3 | TIMER B DISABLE.(DEFAULT)                 | TIMER B ENABLE.                    |
| BIT - 4 | TIMER A INTERRUPT DISABLE.(DEFAULT)       | TIMER A INTERRUPT ENABLE.          |
| BIT - 5 | TIMER B NMI DISABLE.(DEFAULT)             | TIMER B NMI ENABLE.                |
| BIT - 6 | SYSTEM CLOCK = PLL CLOCK(DEFAULT).        | SYSTEM CLOCK = 32768Hz.            |
| BIT - 7 | WATCHDOG TIMER DISABLE.                   | WATCHDOG TIMER ENABLE.(DEFAULT)    |

● **3FE2 System control 2. Write only.**

| 3FE2    | 0   | 1 |
|---------|---|---|
| BIT - 0 | =1 → ENTRY STAND-BY MODE. IN STAND-BY MODE, HOLD CPU. THE NMI AND IRQ WILL WAKE UP THE CPU. |   |

|             |   |
|-------------|---|
| BIT - 1     | =1 → ENTRY SLEEP MODE. IN SLEEP MODE , THE BOTH OF MAIN SYSTEM CLOCK AND 32768Hz WILL BESTOPPED, SO ALL FUNCTION ARE STOPPED AND ONLY EXTERNAL INTERRUPT CAN WAKE UP THIS CHIP  |
| BIT - 3 ~ 2 | 00 : SYSTEM CLOCK = FxOSC/2 X 256(4.19MHz)(DEFAULT).<br>01 : SYSTEM CLOCK = FxOSC/2 X 512(8.38MHz)<br>10 : SYSTEM CLOCK = FxOSC/2 X 768(12.58MHz)   |
| BIT- 7 ~ 4  | 0xxx : FIX-TIMER DISABLE.<br>1000 : FIX-TIMER = 64Hz.<br>1001 : FIX-TIMER = 32Hz.<br>1010 : FIX-TIMER = 16Hz.<br>1011 : FIX-TIMER = 8Hz.<br>1100 : FIX-TIMER = 4Hz.<br>1101 : FIX-TIMER = 2Hz.<br>1110 : FIX-TIMER = 1Hz.<br>1111 : FIX-TIMER = 0.5Hz |

- **3FE3** : PORT\_A[7..0] INTERRUPT ENABLE REGISTER. WRITE ONLY.  
AN '0' IN THIS REGISTER WILL SET THE INTERRUPT FUNCTION OF THE CORRESPONDING PIN OF PORT\_A TO BE ENABLED. THE DEFAULT VALUE FOR EACH BIT IS '1'.
- **3FE4** : PORT\_A[7..0] DATA REGISTER. READ AND WRITE.
- **3FE5** : PORT\_A[7..0] DIRECTION REGISTER. WRITE ONLY.  
AN '1' IN THIS REGISTER WILL SET THE CORRESPONDING PIN OF PORT\_A TO BE OUTPUT.  
THE DEFAULT VALUE FOR EACH BIT IS ZERO.
- **3FE6**: PORT\_B[7..0] DATA REGISTER. WRITE ONLY.
- **3FE7** : CLEAR WATCHDOG TIMER. WRITE ONLY.  
THE WATCHDOG TIMER RESET WILL HAPPEN IF THE PROGRAMMER DO NOT CLEAR THE WATCHDOG TIMER BEFORE WATCHDOG TIMER TIME-OUT.
- **3FE8** VOICE CHANNEL 0 LOW BYTE. WRITE ONLY.  
BIT 2-0 : RESERVED.  
BIT 3: NO USE (MUST 0)  
BIT 7-4: = VOICE CHANNEL 0 LOW NIBBLE BYTE.
- **3FE9** : VOICE CHANNEL 0 HIGH BYTE. WRITE ONLY.  
THE RESOLUTION OF VOICE CHANNEL 0 IS 12 BITS(\$3FE9,\$3FE8 BIT7\_4).

- **3FEA** : BANK REGISTER FOR COPROCESSOR. WRITE ONLY.
  
- **3FEB** : BANK REGISTER MSB BIT FOR COPROCESSOR. WRITE ONLY.  
BANK REGISTER IS 9 BITS REGISTER(\$3FEB BIT0, \$3FEA BIT7-0). THE MEMORY RANGE OF BANK IS FROM \$4000 TO \$7FFF.  
BIT 7-1 : RESERVED.
  
- **3FEC,3FED** : TIMER A DATA OR TONE0 GENERATOR. READ AND WRITE. AFTER TIMER\_A BE ENABLED, THE TIMER WILL START TO COUNT DOWN. WHEN TIMER COUNTS TO ZERO, THE TIMER WILL COUNT FROM THE INITIAL VALUE AND TIMER\_A IRQ WILL BE HAPPEN.  
THE TIME ELAPSE =  $((\$3FED, \$3FEC)+1) / (\text{TIMER A INPUT CLOCK})$ .
  
- **3FEE** : TIMER B LOW BYTE DATA. READ AND WRITE.
  
- **3FEF** : TIMER B HIGH BYTE DATA. READ AND WRITE.  
AFTER TIMER\_B BE ENABLED, THE TIMER WILL START TO COUNT DOWN. WHEN TIMER COUNTS TO ZERO, THE TIMER WILL COUNT FROM THE INITIAL VALUE AND TIMER\_B NMI WILL BE HAPPEN.  
THE TIME ELAPSE =  $((\$3FEF, \$3FEE)+1) / (\text{TIMER B INPUT CLOCK})$ .
  
- **3FF0** : PORT\_A[15..8] DIRECTION REGISTER. WRITE ONLY.  
AN '1' IN THIS REGISTER WILL SET THE CORRESPONDING PIN OF PORT\_A TO BE OUTPUT.  
THE DEFAULT VALUE FOR EACH BIT IS ZERO.
  
- **3FF1** : PORT\_A[15..8] DATA REGISTER. READ AND WRITE.
  
- **3FF2**: PORT\_B[11..8] DATA REGISTER. WRITE ONLY.  
BIT 3-0: PORT\_B PIN 11 TO PIN 8.  
BIT 7-4 : RESERVED.
  
- **3FF4** : BANK REGISTER FOR CPU. WRITE ONLY.
- **3FF5** : BANK REGISTER MSB BIT FOR CPU. WRITE ONLY.  
BANK REGISTER IS 9 BITS REGISTER(\$3FF5 BIT0, \$3FF4 BIT7-0).  
THE MEMORY RANGE OF BANK IS FROM \$4000 TO \$7FFF.  
BIT 1: RESERVED.  
BIT 2: = 1 VOICE0 BUFFER BE TRANSFERRED TO DAC PORT DIRECTLY.(DEFAULT)  
= 0 VOICE0 BUFFER WILL BE TRANSFERRED TO DAC PORT WHEN TIMER\_B NMI HAPPEN.  
BIT 7-3 : RESERVED.



- **3FF6** : PORT\_C[7..0] DATA REGISTER. READ AND WRITE.
- **3FF7** : PORT\_C[15..8] DATA REGISTER. READ AND WRITE.
- **3FF8**: PORT\_C[7..0] DIRECTION REGISTER. WRITE ONLY.  
AN '1' IN THIS REGISTER WILL SET THE CORRESPONDING PIN OF PORT\_C TO BE OUTPUT.  
THE DEFAULT VALUE FOR EACH BIT IS ZERO.
- **3FF9**: PORT\_C[15..8] DIRECTION REGISTER. WRITE ONLY.  
AN '1' IN THIS REGISTER WILL SET THE CORRESPONDING PIN OF PORT\_C TO BE OUTPUT.  
THE DEFAULT VALUE FOR EACH BIT IS ZERO.
- **3FFA** :ADC REGISTER. READ ONLY.  
WHEN THE TIMER B NMI OCCURS, THE A/D CONVERSION PROCESS STARTS AND THE S/H CIRCUIT STOP SAMPLING AND BEGIN HOLDING IT UNTIL THE ADC PROCESS IS FINISHED.  
THE ADC INT WILL GENERATE WHEN ADC PROCESS IS FINISHED.
- **3FFB,3FFC** :.....NO USE
- **3FFD** : .....NO USE
- **3FFE**: VOICE CHANNEL 1 LOW BYTE AND SYSTEM CONTROL 3. WRITE ONLY.

| <b>3FFE</b> | 0                                     | 1                        |
|-------------|---------------------------------------|--------------------------|
| BIT - 0     | SEPARATE MODE FOR DAC OUTPUT(DEFAULT) | MIX MODE FOR DAC OUTPUT. |
| BIT - 1     | SEPARATE MODE FOR PWM OUTPUT(DEFAULT) | MIX MODE FOR PWM OUTPUT  |
| BIT - 2     | NO USE(MUST 0)                        |                          |
| BIT - 3     | NO USE (MUST 0)                       |                          |
| BIT - 7 ~ 4 | VOICE CHANNEL 1 LOW NIBBLE BYTE.      |                          |

- **3FFF** : VOICE CHANNEL 1 HIGH BYTE. WRITE ONLY.  
THE RESOLUTION OF VOICE CHANNEL 1 IS 12 BITS(\$3FFF,\$3FFE BIT7\_4). THIS REGISTER WILL BE TRANSFERRED TO PWM PORT WHILE TIMER\_B NMI HAPPEN IN SEPARATE MODE.

