

CD Digital Signal Processor with Built-in Digital Servo + Shock-proof Memory Controller + Digital High & Bass Boost

Description

The CXD3048R is a digital signal processor LSI for CD players. This LSI incorporates a digital servo, high & bass boost, shock-proof memory controller, 1-bit DAC and analog low-pass filter.

Features

- All digital signal processing during playback is performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

Digital Signal Processor (DSP) Block

- Supports CAV (Constant Angular Velocity) playback
 - Frame jitter free
 - 0.5x to 4x speed continuous playback possible
 - Allows relative rotational velocity readout
- Wide capture range playback mode
 - Spindle rotational velocity following method
 - Supports 1x to 4x speed playback
- Supports variable pitch playback
- The bit clock, which strobes the EFM signal, is generated by the digital PLL.
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
 - C1: double correction, C2: quadruple correction
 - Supported during 4x speed playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and subcode-Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface outputs
- Digital level meter, peak meter
- Bilingual compatible
- VCO control mode
- CD TEXT data demodulation
- Digital Out can be generated from the audio serial input. (also supported after shock-proof and digital bass boost processing, subcode-Q addition function)

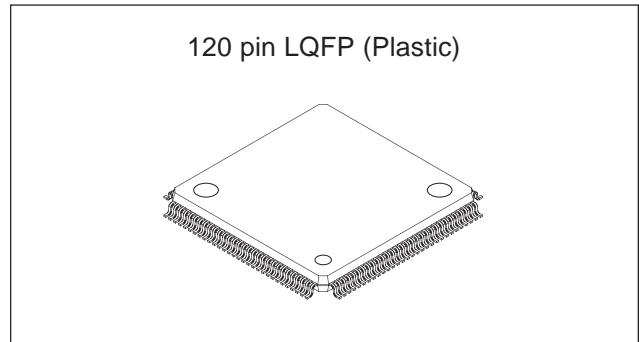
Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment functions
- Surf jump function supporting micro two-axis
- Tracking filter: 6 stages
- Focus filter: 5 stages

Shock-proof Memory Controller Block

- Supports an external 4M-bit/16M-bit DRAM
- Time axis-based data linking
- ADPCM compression method (uncompressed/4 bits/6 bits/8 bits)

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Digital Filter, DAC and Analog Low-pass Filter Blocks

- Digital dynamic bass boost and high boost
 - Bass Boost: 4th-order IIR 24dB/Oct
 - +10dB/+14dB/+18dB/+22dB
 - High Boost: Second-order IIR 12dB/Oct
 - +4dB/+6dB/+8dB/+10dB
- Independent turnover frequency selection possible
 - Bass Boost: 125Hz/160Hz/200Hz
 - High Boost: 5kHz/7kHz
- Digital dynamics (compressor)
 - Volume increased by +5dB at low level
- 8x oversampling digital filter
 - (attenuation: 61dB, ripple within band: ±0.0075dB)
- Digital signal output possible after boost
- Serial data format selectable from (output) 20 bits/18 bits/16 bits (rearward truncation, MSB first)
- Digital attenuation: -∞, -60 to +6dB, 2048 steps (linear)
- Soft mute
- Digital de-emphasis
- High-cut filter

Applications

CD players

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

- Supply voltage V_{DD}, AV_{DD} $V_{SS} - 0.5$ to $+3.5$ V
- Input voltage V_I $V_{SS} - 0.3$ to $V_{DD} + 0.3$ V
- Output voltage V_O $V_{SS} - 0.3$ to $V_{DD} + 0.3$ V
- Storage temperature T_{stg} -55 to $+150$ °C
- Supply voltage difference
 - $AV_{SS} - V_{SS}$ -0.3 to $+0.3$ V
 - $AV_{DD} - V_{DD}$ -0.3 to $+0.3V$ ($AV_{DD} < 1.7V$)
 - $AV_{DD} - V_{DD}$ -0.3 to $+1.0V$ ($AV_{DD} = 1.7$ to $2.7V$)

Recommended Operating Conditions

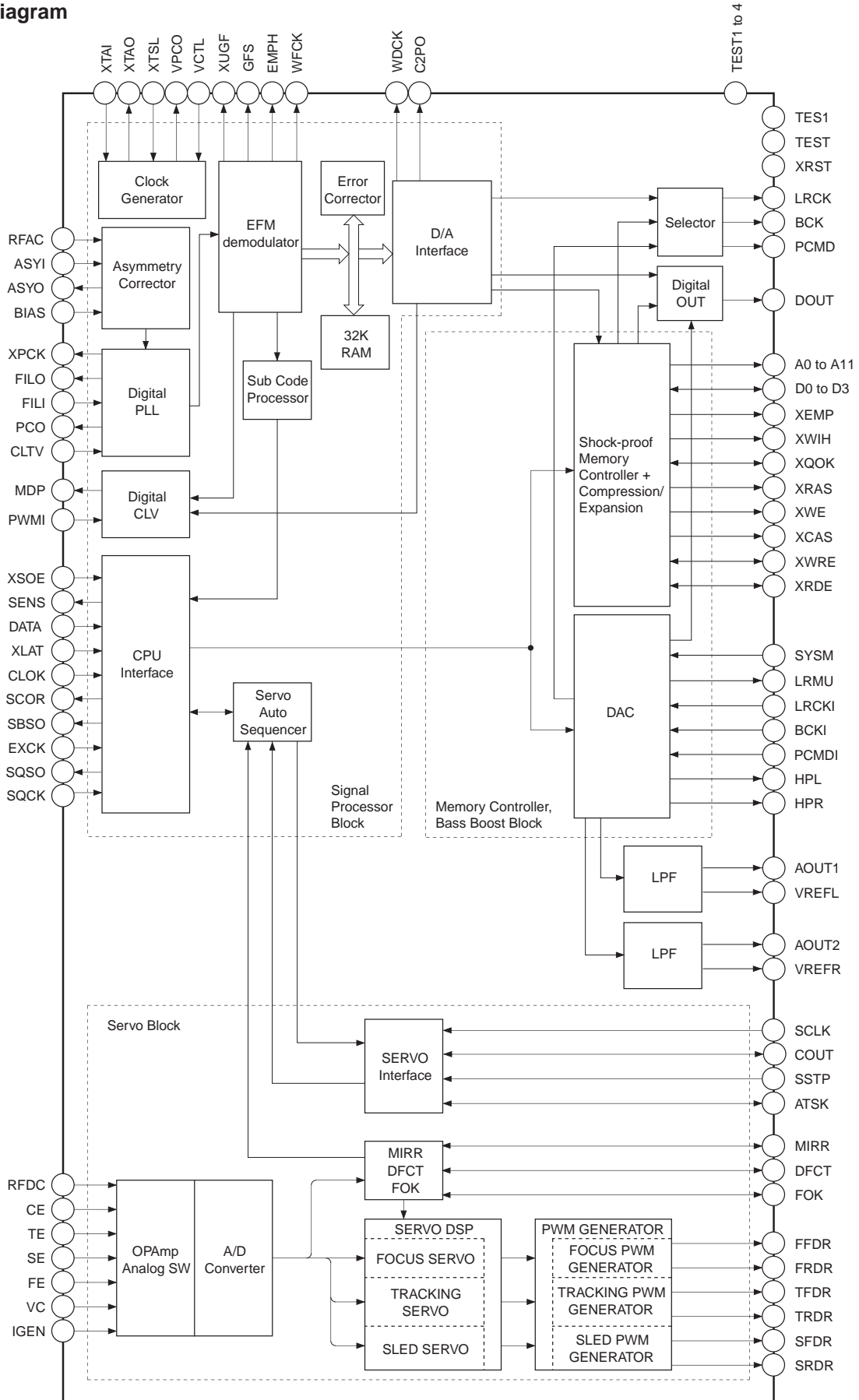
- Supply voltage
 - $V_{DD}, AV_{DD}0, 3, XV_{DD}$ 1.7 to 2.7 V
 - $AV_{DD}1, 2, DV_{DD}$ V_{DD} to 2.7 V
- Operating temperature T_{opr} -20 to $+75$ °C

I/O Pin Capacitance

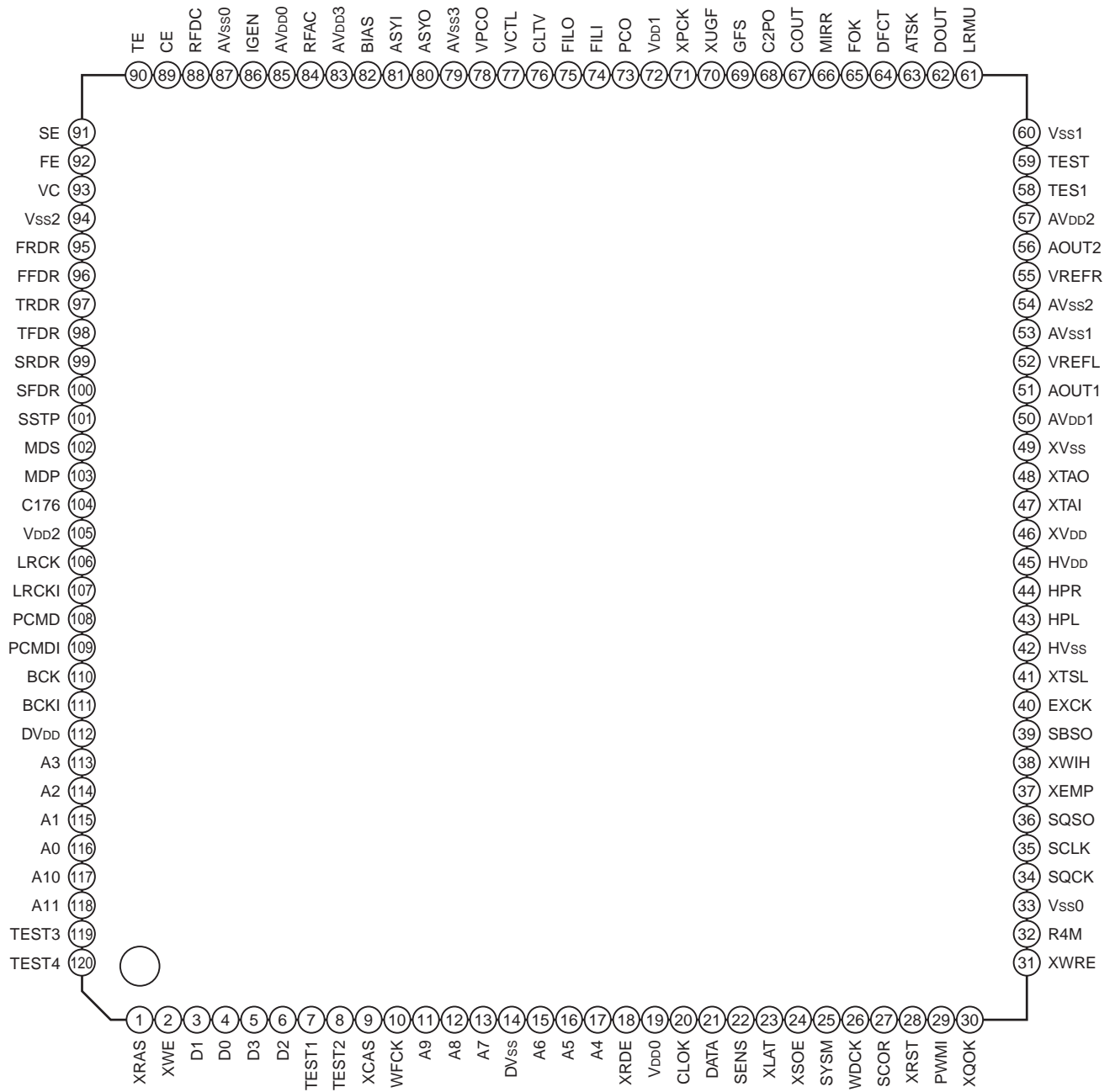
- Input capacitance C_i 7 (max.) pF
- Output capacitance C_o 7 (max.) pF

Note) Measurement conditions $V_{DD} = V_I = 0V$
 $f_M = 1MHz$

Block Diagram



Pin Configuration



Pin Description

| Power supply | Pin No. | Symbol | I/O | Value | Description |
|--------------|---------|------------------|------|---------|--|
| DRAM I/F | 1 | XRAS | O | 1, 0 | DRAM row address strobe signal. |
| | 2 | XWE | O | 1, 0 | DRAM data input enable signal. |
| | 3 | D1 | I/O | 1, 0 | DRAM data bus 1. |
| | 4 | D0 | I/O | 1, 0 | DRAM data bus 0. |
| | 5 | D3 | I/O | 1, 0 | DRAM data bus 3. |
| | 6 | D2 | I/O | 1, 0 | DRAM data bus 2. |
| | 7 | TEST1 | O | | Test pin. Do not connect. |
| | 8 | TEST2 | O | | Test pin. Do not connect. |
| | 9 | XCAS | O | 1, 0 | DRAM column address strobe signal. |
| | 10 | WFCK | O | 1, 0 | WFCK output. XOE is output by switching with the command. |
| | 11 | A9 | O | 1, 0 | DRAM address 9. |
| | 12 | A8 | O | 1, 0 | DRAM address 8. |
| | 13 | A7 | O | 1, 0 | DRAM address 7. |
| | 14 | DVss | — | — | DRAM interface GND. |
| | 15 | A6 | O | 1, 0 | DRAM address 6. |
| | 16 | A5 | O | 1, 0 | DRAM address 5. |
| | 17 | A4 | O | 1, 0 | DRAM address 4. |
| | Digital | 18 | XRDE | I/O | 1, 0 |
| 19 | | V _{DD0} | — | — | Digital power supply. |
| 20 | | CLOCK | I | | Serial data transfer clock input from CPU. SQSO and SENS readout clocks are output by switching with the command. |
| 21 | | DATA | I | | Serial data input from CPU. |
| 22 | | SENS | O | 1, Z, 0 | SENS output to CPU. SQSO data is output by switching with the command. |
| 23 | | XLAT | I | | Latch input from CPU. The serial data is latched at the falling edge. XLAT which is low for 6μs or more is enabled. |
| 24 | | XSOE | I | | Clock input mode switching from CPU. Valid when \$A4 ENXSOE = 1. |
| 25 | | SYSM | I | | Mute input. Muted when high. |
| 26 | | WDCK | O | 1, 0 | Word clock output $f = 2Fs$. GRSCOR is output by switching with the command. |
| 27 | | SCOR | O | 1, 0 | High output when the subcode sync is detected. SCOR, which is interpolated in the IC, is output by switching with the command. |
| 28 | | XRST | I | | System reset. Reset when low. |
| 29 | | PWMI | I | | Spindle motor external control input. |
| 30 | | XQOK | I/O | 1, 0 | Subcode Q OK input. XQOK monitor is output by switching with the command. |
| 31 | | XWRE | I/O | 1, 0 | DRAM write enable signal input. XWRE monitor is output by switching with the command. |

| Power supply | Pin No. | Symbol | I/O | Value | Description |
|--------------|---------|--------|-----|--------|---|
| Digital | 32 | R4M | O | 1, 0 | Microcomputer clock output. R8M and C4M are output by switching with the command. |
| | 33 | Vss0 | — | — | Digital GND. |
| | 34 | SQCK | I | | SQSO readout clock input. |
| | 35 | SCLK | I | | SENS serial data readout clock input. |
| | 36 | SQSO | O | 1, 0 | Subcode Q 80-bit and PCM peak and level data output. CD TEXT data output. |
| | 37 | XEMP | O | 1, 0 | DRAM readout prohibited signal. |
| | 38 | XWIH | O | 1, 0 | Write to DRAM prohibited signal. |
| | 39 | SBSO | O | 1, 0 | Subcode P to W serial output. |
| | 40 | EXCK | I | | SBSO readout clock input. |
| | 41 | XTSL | I | | Crystal selection input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz. |
| H/P | 42 | HVss | — | — | Headphone GND. |
| | 43 | HPL | O | 1, 0 | Lch headphone PDM output. |
| | 44 | HPR | O | 1, 0 | Rch headphone PDM output. |
| | 45 | HVDD | — | — | Headphone power supply. |
| X'tal | 46 | XVDD | | | Master clock power supply. |
| | 47 | XTAI | I | | Crystal oscillation circuit input. The master clock is externally input from this pin. |
| | 48 | XTAO | O | | Crystal oscillation circuit output. |
| | 49 | XVss | | | Master clock GND. |
| Lch | 50 | AVDD1 | — | — | Analog power supply. |
| | 51 | AOUT1 | O | Analog | Lch analog output. |
| | 52 | VREFL | O | Analog | Lch reference voltage. |
| | 53 | AVss1 | — | — | Analog GND. |
| Rch | 54 | AVss2 | — | — | Analog GND. |
| | 55 | VREFR | O | Analog | Rch reference voltage. |
| | 56 | AOUT2 | O | Analog | Rch analog output. |
| | 57 | AVDD2 | — | — | Analog power supply. |
| Digital | 58 | TES1 | I | | Test pin. Normally GND. |
| | 59 | TEST | I | | Test pin. Normally GND. |
| | 60 | Vss1 | — | — | Digital GND. |
| | 61 | LRMU | O | 1, 0 | OR signal output of Lch, Rch "0" detection flag (AND output) and SYSM. Only "0" detection flag is output by switching with the command. |
| | 62 | DOUT | O | 1, 0 | Digital Out output. |
| | 63 | ATSK | I/O | 1, 0 | Anti-shock input/output. |
| | 64 | DFCT | I/O | 1, 0 | Defect signal input/output. |
| | 65 | FOK | I/O | 1, 0 | Focus OK signal input/output. |

| Power supply | Pin No. | Symbol | I/O | Value | Description |
|--------------|---------|-------------------|-----|---------|---|
| Digital | 66 | MIRR | I/O | 1, 0 | Mirror signal input/output. |
| | 67 | COUT | I/O | 1, 0 | Track number count signal input/output. SCOR is output by switching with the command. |
| | 68 | C2PO | O | 1, 0 | C2PO output. MNT3 and GTOP are output by switching with the command. |
| | 69 | GFS | O | 1, 0 | GFS output. MNT2 and XROF are output by switching with the command. |
| | 70 | XUGF | O | 1, 0 | XUGF output. MNT0, RFCK, C4M and QRCVD are output by switching with the command. |
| | 71 | XPCK | O | 1, 0 | XPCK output. MNT1, FSTO and GTOP are output by switching with the command. |
| | 72 | V _{DD1} | — | — | Digital power supply. |
| ASYM | 73 | PCO | O | 1, Z, 0 | Master PLL charge pump output. |
| | 74 | FILI | I | | Master PLL filter input. |
| | 75 | FILO | O | Analog | Master PLL (slave = digital PLL) filter output. |
| | 76 | CLTV | I | | Multiplier VCO1 control voltage input. |
| | 77 | VCTL | I | | Wide-band EFM PLL VCO2 control voltage input. |
| | 78 | VPCO | O | 1, Z, 0 | Wide-band EFM PLL charge pump output. |
| | 79 | AV _{SS3} | — | — | Analog GND. |
| | 80 | ASYO | O | 1, 0 | EFM full-swing output (low = V _{SS} , high = V _{DD}). |
| | 81 | ASYI | I | | Asymmetry comparator voltage input. |
| | 82 | BIAS | I | | Asymmetry circuit constant current input. |
| | 83 | AV _{DD3} | — | — | Analog power supply. |
| A/D | 84 | RFAC | I | | EFM signal input. |
| | 85 | AV _{DD0} | — | — | Analog power supply. |
| | 86 | IGEN | I | | Operational amplifier constant current input. |
| | 87 | AV _{SS0} | — | — | Analog GND. |
| | 88 | RFDC | I | | RF signal input. |
| | 89 | CE | I | | Center servo analog input or E input. |
| | 90 | TE | I | | Tracking error signal input or F input. |
| | 91 | SE | I | | Sled error signal input or B input. |
| Digital | 92 | FE | I | | Focus error signal input or A input. |
| | 93 | VC | I | | Center voltage input. |
| | 94 | V _{SS2} | — | — | Digital GND. |
| | 95 | FRDR | O | 1, 0 | Focus drive output. |
| | 96 | FFDR | O | 1, 0 | Focus drive output. |
| | 97 | TRDR | O | 1, 0 | Tracking drive output. |
| | 98 | TFDR | O | 1, 0 | Tracking drive output. |
| | 99 | SRDR | O | 1, 0 | Sled drive output. |
| | 100 | SFDR | O | 1, 0 | Sled drive output. |

| Power supply | Pin No. | Symbol | I/O | Value | Description |
|--------------|---------|------------------|-----|---------|--|
| Digital | 101 | SSTP | I | | Disc innermost detection signal input. |
| | 102 | MDS | O | 1, Z, 0 | Spindle drive output. |
| | 103 | MDP | O | 1, Z, 0 | Spindle motor servo control output. |
| | 104 | C176 | O | 1, 0 | 176.4kHz output. 88.2kHz for quasi-double speed setting. Low output when XRST = low. |
| | 105 | V _{DD2} | — | — | Digital power supply. |
| DRAM I/F | 106 | LRCK | O | 1, 0 | D/A interface. LR clock output $f = F_s$. |
| | 107 | LRCKI | I | | D/A interface. LR clock input. |
| | 108 | PCMD | O | 1, 0 | D/A interface. Serial data output. (two's complement, MSB first) |
| | 109 | PCMDI | I | | D/A interface. Serial data input. (two's complement, MSB first) |
| | 110 | BCK | O | 1, 0 | D/A interface. Bit clock output. |
| | 111 | BCKI | I | | D/A interface. Bit clock input. |
| | 112 | DV _{DD} | — | — | DRAM interface power supply. |
| | 113 | A3 | O | 1, 0 | DRAM address 3. |
| | 114 | A2 | O | 1, 0 | DRAM address 2. |
| | 115 | A1 | O | 1, 0 | DRAM address 1. |
| | 116 | A0 | O | 1, 0 | DRAM address 0. |
| | 117 | A10 | O | 1, 0 | DRAM address 10. |
| | 118 | A11 | I/O | 1, 0 | DRAM address 11. Write prohibition factor is input by switching with the command. |
| | 119 | TEST3 | O | | Test pin. Do not connect. |
| | 120 | TEST4 | O | | Test pin. Do not connect. |

Notes) • PCMD is a MSB first, two's complement output.

- G_{TOP} is used to monitor the frame sync protection status. (High: sync protection window released.)
- X_{UGF} is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- X_{PCK} is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The G_{FS} signal goes high when the frame sync and the insertion protection timing match.
- R_{FCK} is derived from the crystal accuracy, and has a cycle of 136 μ s.
- C_{2PO} represents the data error status.
- X_{ROF} is generated when the 32K RAM exceeds the ± 28 frame jitter margin.
- C_{4M} is a 4.2336MHz output that changes in CAV-W mode and variable pitch mode.
- R_{8M} is the 8.4672MHz output.
- F_{STO} is the 2/3 frequency-division output of the XTAL pin.
- S_{OUT} is the serial data output inside the servo block.
- S_{OCK} is the serial data readout clock output inside the servo block.
- X_{OLT} is the serial data latch output inside the servo block.

Monitor Pin Output Combinations

| Command bit | | | | Output data | | | | | |
|-------------|------|-------|-------|-------------|------|------|------|------|------|
| MONSEL | SRO1 | MTSL1 | MTSL0 | | | | | | |
| 0 | 0 | 0 | 0 | XUGF | XPCK | GFS | C2PO | COUT | MIRR |
| 0 | 0 | 0 | 1 | MNT0 | MNT1 | MNT2 | MNT3 | COUT | MIRR |
| 0 | 0 | 1 | 0 | RFCK | XPCK | XROF | GTOP | COUT | MIRR |
| 0 | 0 | 1 | 1 | C4M | FSTO | GFS | C2PO | COUT | MIRR |
| 0 | 1 | 0 | 0 | SOUT | SOCK | XOLT | C2PO | COUT | MIRR |
| 1 | — | — | — | QRCVD | GTOP | GFS | C2PO | SCOR | — |

—: don't care

Electrical Characteristics

1. DC Characteristics (V_{DD1} = 2.5 ± 0.2V, V_{DD2} (logic) = 1.8 ± 0.1V, DV_{SS} = V_{SS} = 0V, Topr = -20 to +75°C)

| Item | | | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|------------------------|---------------------------|-----------------------------------|--|------|------|------|------|-----------------|
| Input voltage (1) | High level input voltage | V _{IH} | | 1.7 | | | V | *13, *15 |
| | Low level input voltage | V _{IL} | | | | 0.7 | | |
| Input voltage (2) | High level input voltage | V _{t+} | Schmitt input | 1.7 | | | V | *14 |
| | Low level input voltage | V _{t-} | | | | 0.7 | | |
| | Hysteresis | V _{t+} - V _{t-} | | | 0.4 | | | |
| Output voltage | High level output voltage | V _{OH} | I _{OH} = -4mA | 2.0 | | | V | *12, *13 |
| | Low level output voltage | V _{OL} | I _{OL} = 4mA | | | 0.4 | | |
| Input leak current (1) | | I _I (1) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *15 |
| Input leak current (2) | | I _I (2) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *13 |

(V_{DD} = AV_{DD} = 2.5 ± 0.2V, V_{SS} = AV_{SS} = 0V, Topr = -20 to +75°C)

| Item | | | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|---|---------------------------|-----------------------------------|--|-----------------------|------|-----------------|------|------------------|
| Input voltage (1) | High level input voltage | V _{IH} (1) | | 1.7 | | | V | *1, *2, *3, *4 |
| | Low level input voltage | V _{IL} (1) | | | | 0.7 | | |
| Input voltage (2) | Input voltage | V _{IN} (2) | Analog input | V _{SS} | | V _{DD} | V | *6, *7 |
| Input voltage (3) | High level input voltage | V _{t+} | Schmitt input | 1.7 | | | V | *5 |
| | Low level input voltage | V _{t-} | | | | 0.7 | | |
| | Hysteresis | V _{t+} - V _{t-} | | | 0.4 | | | |
| Output voltage (1) | High level output voltage | V _{OH} (1) | I _{OH} = -4mA | 2.0 | | | V | *2, *8, *10, *15 |
| | Low level output voltage | V _{OL} (1) | I _{OL} = 4mA | | | 0.4 | | |
| Output voltage (2) | High level output voltage | V _{OH} (2) | I _{OH} = -2mA | 2.0 | | | V | *9 |
| | Low level output voltage | V _{OL} (2) | I _{OL} = 2mA | | | 0.4 | | |
| Output voltage (3) | High level output voltage | V _{OH} (3) | I _{OH} = -0.28mA | V _{DD} - 0.5 | | V _{DD} | V | *11 |
| | Low level output voltage | V _{OL} (3) | I _{OL} = 0.36mA | 0 | | 0.4 | | |
| Input leak current (1) | | I _I (1) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *1, *3, *5, *6 |
| Input leak current (2) | | I _I (2) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *2, *4 |
| Input leak current (3) | | I _I (3) | V _{IN} = 0.25V _{DD} to 0.75V _{DD} | -40 | | 40 | μA | *7 |
| Tri-state output leak current (when high impedance) | | I _{OZ} | V _O = V _{SS} or V _{DD} | -10 | | 10 | μA | *10 |

(V_{DD} = AV_{DD} = 1.8 ± 0.1V, V_{SS} = AV_{SS} = 0V, Topr = -20 to +75°C)

| Item | | | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|---|---------------------------|-----------------------------------|--|-----------------------|------|---------------------|------|---------------------|
| Input voltage (1) | High level input voltage | V _{IH} (1) | | 0.65V _{DD} | | | V | *1, *2, *3, *4 |
| | Low level input voltage | V _{IL} (1) | | | | 0.35V _{DD} | | |
| Input voltage (2) | Input voltage | V _{IN} (2) | Analog input | V _{SS} | | V _{DD} | V | *6, *7 |
| Input voltage (3) | High level input voltage | V _{t+} | Schmitt input | 0.65V _{DD} | | | V | *5 |
| | Low level input voltage | V _{t-} | | | | 0.35V _{DD} | | |
| | Hysteresis | V _{t+} - V _{t-} | | | 0.4 | | | |
| Output voltage (1) | High level output voltage | V _{OH} (1) | I _{OH} = -2.4mA | V _{DD} - 0.4 | | V _{DD} | V | *2, *8, *10, *16 |
| | Low level output voltage | V _{OL} (1) | I _{OL} = 2.4mA | 0 | | 0.4 | | |
| Output voltage (2) | High level output voltage | V _{OH} (2) | I _{OH} = -1.4mA | V _{DD} - 0.4 | | V _{DD} | V | *9 |
| | Low level output voltage | V _{OL} (2) | I _{OL} = 1.4mA | 0 | | 0.4 | | |
| Output voltage (3) | High level output voltage | V _{OH} (3) | I _{OH} = -0.28mA | V _{DD} - 0.5 | | V _{DD} | V | *11 |
| | Low level output voltage | V _{OL} (3) | I _{OL} = 0.36mA | 0 | | 0.4 | | |
| Input leak current (1) | | I _I (1) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *1, *3, *5, *6 |
| Input leak current (2) | | I _I (2) | V _{IN} = V _{SS} or V _{DD} | -10 | | 10 | μA | *2, *4 |
| Input leak current (3) | | I _I (3) | V _{IN} = 0.25V _{DD} to 0.75V _{DD} | -40 | | 40 | μA | *7 |
| Tri-state output leak current (when high impedance) | | I _{OZ} | V _O = V _{SS} or V _{DD} | -10 | | 10 | μA | *10 |

Applicable pins

*1 TEST, TES1

*2 COUT, MIRR, DFCT, FOK, XQOK, XWRE, ATSK

*3 SYSM, DATA, XSOE, XTSL

*4 SSTP, PWMI

*5 SQCK, EXCK, XRST, CLOK, SCLK, XLAT

*6 VCTL, FILI, CLTV, ASYI, IGEN, BIAS

*7 RFDC, CE, TE, SE, FE, VC

*8 XEMP, XWIH, SQSO, SBSO, XUGF, XPCK, GFS, C2PO, SCOR, WDCK, SFDR, SRDR, TFDR, TRDR, FFDR, FRDR, ASYO, DOUT, C176

*9 R4M

*10 SENS, MDP, VPCO, PCO, MDS

*11 FILO

*12 A0 to A10, XRAS, XCAS, XWE, WFCK, LRCK, BCK, PCMD

*13 D0 to D3, XRDE, A11

*14 LRCKI, BCKI

*15 PCMDI

*16 HPL, HPR

2. AC Characteristics

(1) XTAI pin

(a) When using self-excited oscillation

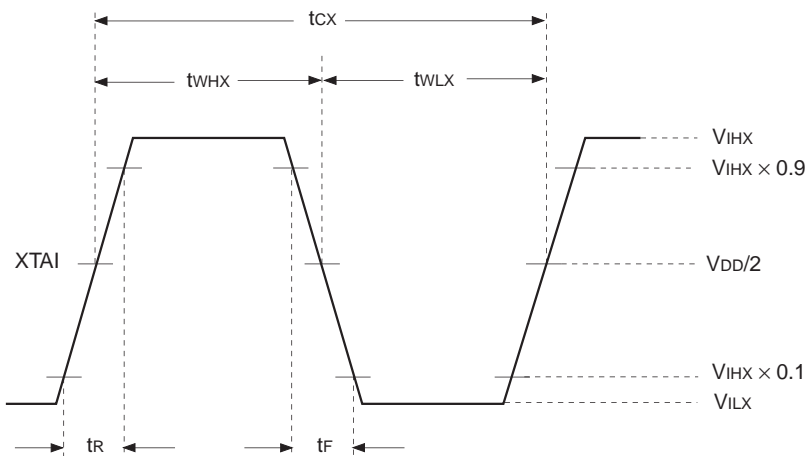
($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|-----------|------|------|------|------|
| Oscillation frequency | f_{MAX} | 7 | | 34 | MHz |

(b) When inputting pulses to XTAI pin

($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|------------|-------------|------|-------------|------|
| High level pulse width | t_{WHX} | 13 | | 500 | ns |
| Low level pulse width | t_{WLX} | 13 | | 500 | ns |
| Pulse cycle | t_{CX} | 26 | | 1000 | ns |
| Input high level | V_{IHx} | $0.7V_{DD}$ | | | V |
| Input low level | V_{ILx} | | | $0.2V_{DD}$ | V |
| Rise time, fall time | t_R, t_F | | | 10 | ns |



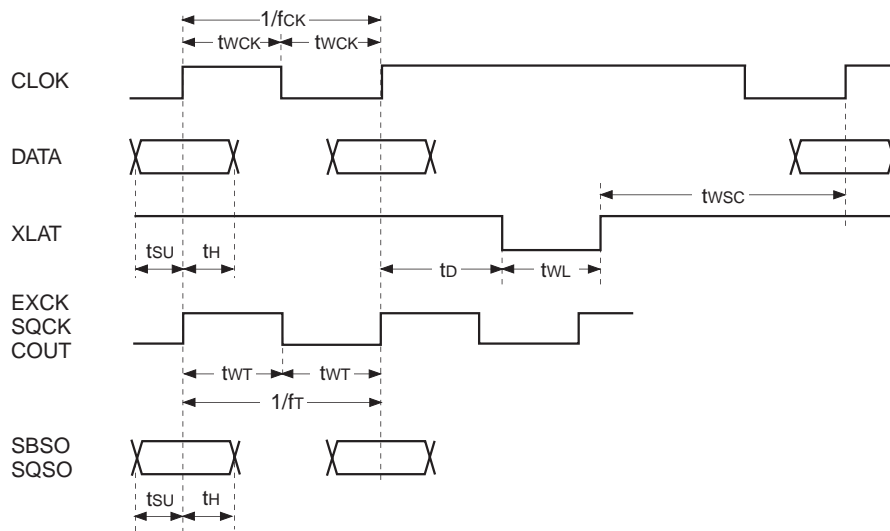
Note) When the pulse is input to the XTAI pin, be sure to input it via the capacitor.

(2) CLOK, DATA, XLAT, SQCK and EXCK pins

($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|------------------|------|------|-------|------|
| Clock frequency | f _{ck} | | | 0.65 | MHz |
| Clock pulse width | t _{wck} | 750 | | 30000 | ns |
| Setup time | t _{su} | 300 | | | ns |
| Hold time | t _h | 300 | | | ns |
| Delay time | t _d | 300 | | 30000 | ns |
| Latch pulse width | t _{wl} | 750 | | | ns |
| EXCK SQCK frequency | f _r | | | 0.65 | MHz |
| EXCK SQCK pulse width | t _{wT} | 750 | | | ns |
| COUT frequency (during input)* | f _r | | | 65 | kHz |
| COUT pulse width (during input)* | t _{wT} | 7.5 | | | μs |

* Only when \$44 and \$45 are executed.

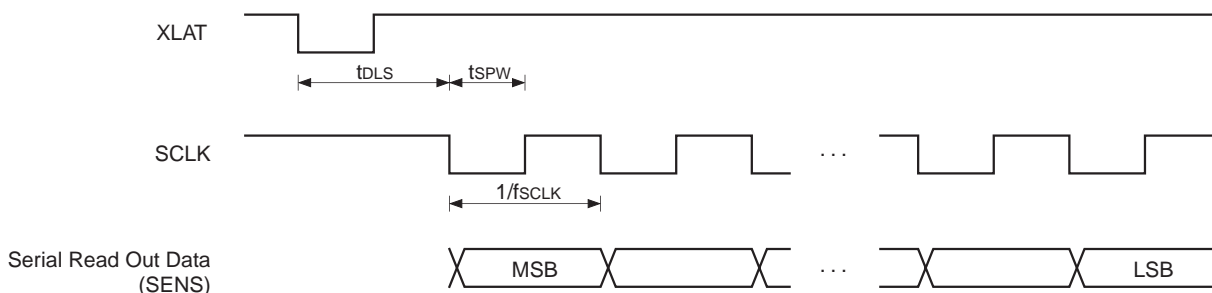


(3) R4M pin (when \$A4X CKOUTSL2 = CKOUTSL1 = 0)

($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------|------------------|------|-----------------|------|------|
| Output frequency | f _{out} | | 4.2336 | | MHz |
| Output duty | D _{out} | | 50 | | % |
| Output amplitude | V _{out} | | V _{DD} | | V |

(4) SCLK pin



($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------|------------|------|------|------|---------|
| SCLK frequency | f_{SCLK} | | | 16 | MHz |
| SCLK pulse width | t_{SPW} | 31.3 | | | ns |
| Delay time | t_{DLS} | 15 | | | μs |

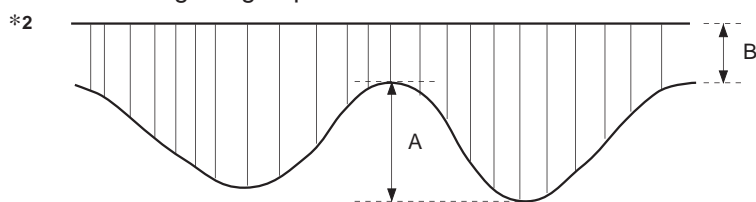
(5) COUT, MIRR and DFCT pins

Operating frequency

($V_{DD} = AV_{DD} = 1.8 \pm 0.1V$ and $2.5 \pm 0.2V$, $V_{SS} = AV_{SS} = 0V$, $Topr = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|----------------------------------|-------------|------|------|------|------|------------|
| COUT maximum operating frequency | f_{COUT} | 40 | | | kHz | *1 |
| MIRR maximum operating frequency | f_{MIRR} | 40 | | | kHz | *2 |
| DFCT maximum operating frequency | f_{DFCTH} | 5 | | | kHz | *3 |

*1 When using a high-speed traverse TZC.



When the RF signal continuously satisfies the following conditions during the above traverse.

- $A = 0.11V_{DD}$ to $0.23V_{DD}$

- $\frac{B}{A + B} \leq 25\%$

*3 During complete RF signal omission.

When settings related to DFCT signal generation are Typ.

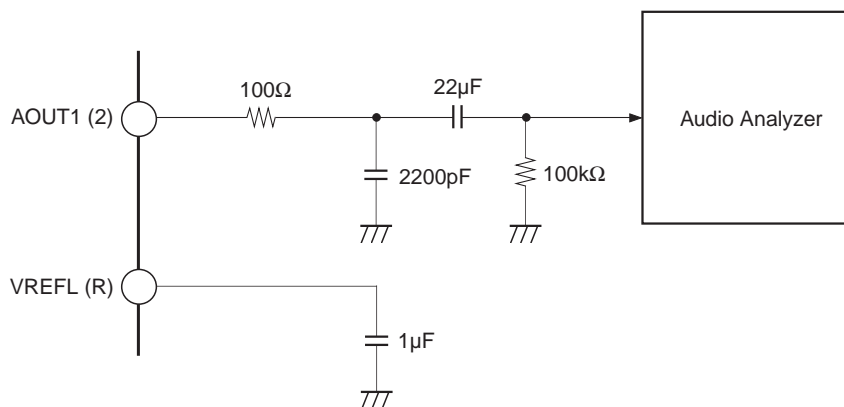
1-bit DAC and LPF Block Analog Characteristics

($V_{DD} = AV_{DD} = 2.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = +25^{\circ}C$)

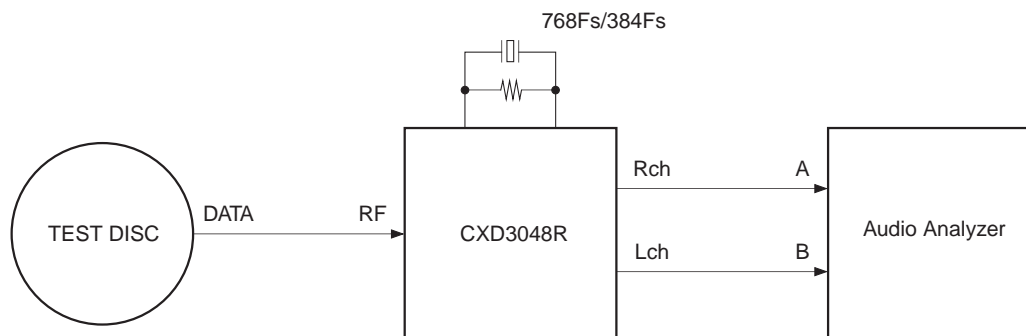
| Item | Symbol | Conditions | Crystal | Min. | Typ. | Max. | Unit |
|---------------------------|--------|---|---------|------|-------|-------|------|
| Total harmonic distortion | THD | 1kHz sine wave, 0dB data, 20kHz LPF | 384Fs | | 0.009 | 0.016 | % |
| | | | 768Fs | | 0.009 | 0.016 | |
| Signal-to-noise ratio | S/N | 1kHz sine wave, 0dB data, AMUT OFF (Using A-weighting filter 20kHz LPF) | 384Fs | 92 | 94 | | dB |
| | | | 768Fs | 92 | 94 | | |

Fs = 44.1kHz in all cases.

The total harmonic distortion and signal-to-noise ratio measurement circuits are shown below.



LPF external circuit diagram (\$A560C400 PDMSEL = 1)



Block diagram of analog characteristics measurement

($V_{DD} = AV_{DD} = 2.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = +25^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Applicable pins |
|----------------------|-------------------|------|------|------|-------------------|-----------------|
| Output voltage | V _{OUT} | 640 | 658 | | mV _{rms} | *1 |
| Load resistance | R _L | 10 | | | kΩ | *1 |
| VREF pin capacitance | C _{VREF} | | 1 | | μF | *2 |

* Measurement is conducted for the above circuit diagrams with the sine wave output of 1kHz and 0dB.

Applicable pins

*1 AOUT1, AOUT2

*2 VREFL, VREFR

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Explanation of abbreviations
 AVRG: Average
 AGCNTL: Auto gain control
 FCS: Focus
 TRK: Tracking
 SLD: Sled
 DFCT: Defect

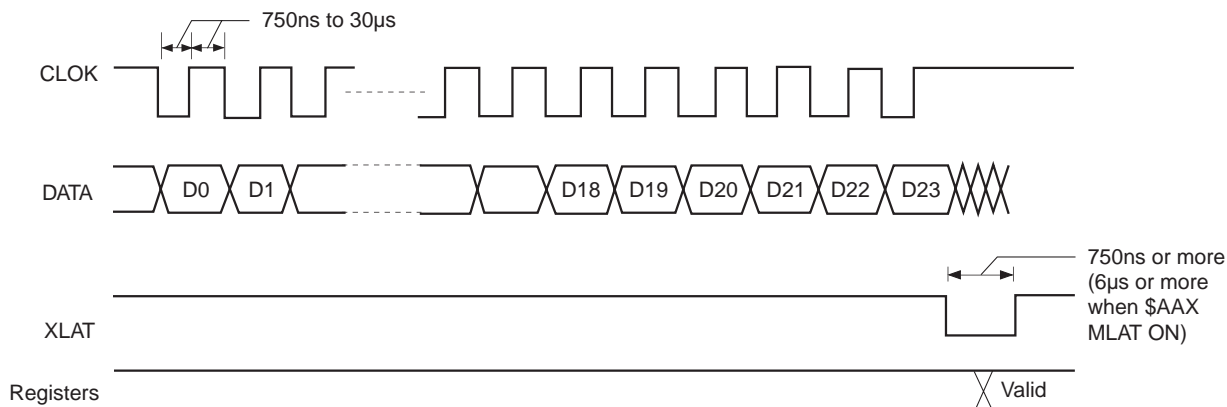
[1] CPU Interface

§1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below. (See 2. AC Characteristics in Electrical Characteristics, for the details of the AC characteristics.)



- The internal registers are initialized by a reset when XRST = 0.

§1-2. CPU Interface Command Table

Total bit length for each register

| Register | Total bit length |
|----------|------------------|
| 0 to 2 | 8 bits |
| 3 | 8 to 24 bits |
| 4 to 6 | 16 bits |
| 7 | 20 bits |
| 8 | 32 bits |
| 9 | 32 bits |
| A | 32 bits |
| B | 28 bits |
| C | 28 bits |
| D | 28 bits |
| E | 20 bits |

Command Table (\$0X to 1X)

| Register | Command | Address D23 to D20 | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | | | |
|----------|------------------|-----------------------|--------|-----|-----|-----|--------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|----|---------------|---|----------------------------------|
| | | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| 0 | FOCUS CONTROL | 0 0 0 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO ON (FOCUS GAIN NORMAL) | |
| | | | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO ON (FOCUS GAIN DOWN) | |
| | | | 0 | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, 0V OUT | |
| | | | 0 | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT | |
| | | | 0 | — | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SEARCH VOLTAGE DOWN |
| | | | 0 | — | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SEARCH VOLTAGE UP |
| 1 | TRACKING CONTROL | 0 0 0 1 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANTI SHOCK ON | | |
| | | | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANTI SHOCK OFF | |
| | | | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | BRAKE ON | |
| | | | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | BRAKE OFF |
| | | | — | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN NORMAL |
| | | | — | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP |
| | | | — | — | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 1 |
| | | | — | — | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 2 |

Command Table (\$2X to 3X)

| Regis- ter | Command | Address | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | | |
|---------------|------------------|------------|-----|--------|-----|-----|-----|--------|-----|-----|-----|--------|----|----|----|--------|----|----|----|--------|----|----|---|---|-------------------|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| 2 | TRACKING CONTROL | 0 0 1 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO OFF | | |
| | | | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO ON | |
| | | | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FORWARD TRACK JUMP | |
| | | | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | REVERSE TRACK JUMP | |
| | | | — | — | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED SERVO OFF |
| | | | — | — | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED SERVO ON |
| | | | — | — | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FORWARD SLED MOVE |
| | | | — | — | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | REVERSE SLED MOVE |
| Regis- ter | Command | Address | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| 3 | SELECT | 0 0 1 1 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL ($\pm 1 \times$ basic value) (default) | | |
| | | | 0 | 0 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL ($\pm 2 \times$ basic value) | | |
| | | | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL ($\pm 3 \times$ basic value) | | |
| | | | 0 | 0 | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL ($\pm 4 \times$ basic value) | |

—: don't care

Command Table (\$340X)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---------------|---------|------------|------------|------------|-----------|-----|-----|-----|--------|-----|-----|---|--------|-----|-----|-----|--|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 0 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K00) SLED INPUT GAIN |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K01) SLED LOW BOOST FILTER A-H |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K02) SLED LOW BOOST FILTER A-L |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K03) SLED LOW BOOST FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K04) SLED LOW BOOST FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K05) SLED OUTPUT GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K06) FOCUS INPUT GAIN |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K07) SLED AUTO GAIN |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K08) FOCUS HIGH CUT FILTER A |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K09) FOCUS HIGH CUT FILTER B |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A |
| 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN | | | | | |

Command Table (\$341X)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---------------|---------|------------|------------|------------|-----------|-----|-----|-----|--------|-----|-----|--|--------|-----|-----|-----|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 0 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K11) FOCUS OUTPUT GAIN |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K12) ANTI SHOCK INPUT GAIN |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K13) FOCUS AUTO GAIN |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K18) FIX |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K19) TRACKING INPUT GAIN |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1A) TRACKING HIGH CUT FILTER A |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1B) TRACKING HIGH CUT FILTER B |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H |
| 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L | | | | | |

Command Table (\$342X)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---------------|---------|------------|------------|------------|-----------|-----|-----|-----|--------|-----|-----|-----------------------------|--------|-----|-----|-----|--|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 1 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K22) TRACKING OUTPUT GAIN |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K23) TRACKING AUTO GAIN |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2E) Not used |
| 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2F) Not used | | | | | |

Command Table (\$343X)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---------------|---------|------------|------------|------------|-----------|-----|-----|-----|--------|-----|-----|---|--------|-----|-----|-----|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 1 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K30) SLED INPUT GAIN (when TGup2 is accessed with SFSK = 1) |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K32) Not used |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN | | | | | |
| 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3F) Not used | | | | | |

Command Table (\$344X)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---------------|---------|------------|------------|------------|-----------|-----|-----|-----|--------|-----|-----|-----------------------------|--------|-----|-----|-----|--|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 1 0 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K41) TRACKING HOLD FILTER A-H |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K42) TRACKING HOLD FILTER A-L |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K43) TRACKING HOLD FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K44) TRACKING HOLD FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K46) TRACKING HOLD INPUT GAIN (when TGup2 is accessed with THSK = 1) |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K47) Not used |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K49) FOCUS HOLD FILTER A-H |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4A) FOCUS HOLD FILTER A-L |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4B) FOCUS HOLD FILTER B-H |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4C) FOCUS HOLD FILTER B-L |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4E) Not used |
| 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4F) Not used | | | | | |

Command Table (\$348X to 3FX)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | | | | |
|---------------|---------|------------|------------|-----------|-----|-----|-----|------------|------------|------------|------------|------------|-------------|------------|-----------|------------|-----------|-----------|-------------|----------------------|-----|--------------------|--|
| | | D23 to D20 | D19 to D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 1 | 0 | 0 | 0 | PGFS 1 | PGFS 0 | PFOK 1 | PFOK 0 | 0 | 0 | 0 | MRS | MRT1 | MRT0 | 0 | 0 | PGFS, PFOK, RFAC | | | |
| | | | | 1 | 0 | 1 | 0 | A/D SEL | COPY EN | EMPH D | CAT b8 | DOU EN1 | DOU DMUT | DOU WOD | WIN EN | DOU EN2 | 0 | 0 | 0 | 0 | DOU | | |
| | | | | 1 | 0 | 1 | 1 | SFBK 1 | SFBK 2 | 0 | 0 | LB1 SN | LB2 SN | LB2 SM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Booster Surf Brake | |
| | | | | 1 | 1 | 0 | 0 | THB ON | FHB ON | TLB1 ON | FLB1 ON | TLB2 ON | 0 | HBST 1 | HBST 0 | LB1S 1 | LB1S 0 | LB2S 1 | LB2S 0 | 0 | 0 | Booster | |
| | | | | 1 | 1 | 1 | 0 | IDF SL3 | IDF SL2 | IDF SL1 | IDF SL0 | 0 | DF SLS | IDFT 1 | IDFT 0 | 0 | 0 | LPDF 0 | INV RFDC | 0 | 0 | DFCT | |
| | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | | | | |
| | | | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | — | FCS Bias Limit | | | |
| | | | | | | | | 0 | 1 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | — | FCS Bias Data | | | |
| | | | | | | | | 0 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 | Traverse Center Data | | | |

—: don't care

Command Table (\$34FX to 3FX) cont.

| Regis- ter | Command | Address 1 | Address 2 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | | | | |
|---------------|---------|------------|-----------|------|------|------|--------|------|------|------|-----------|-----------|-----------|-----------|-----------|------|------|------|--------|---------------|------------|------|--------------------------------------|---------------------------|------|-------|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | |
| 3 | SELECT | 0 0 1 1 | 0 | 1 | 0 | 1 | FT1 | FT0 | FS5 | FS4 | FS3 | FS2 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 | FCS search, AGF | | | |
| | | | 0 | 1 | 1 | 0 | TDZC | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 | TRK jump, AGT | | | |
| | | | 0 | 1 | 1 | 1 | FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGGT | AGV1 | AGV2 | AGHS | AGHT | FZC, AGC, SLD move | | | |
| | | | 1 | 0 | 0 | 0 | VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 | DC measure, cancel | | | |
| | | | 1 | 0 | 0 | 1 | DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Serial data readout | | |
| | | | 1 | 0 | 1 | 0 | 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | FIF ZC | TJD0 | FPS1 | FPS0 | TPS1 | TPS0 | SVDA | SJHD | INBK | MT10 | FCS Bias, Gain, Surf jump / brake | | | |
| | | | | | | | 1 | 0 | 0 | 0 | FPG S1 | FPG S0 | TPG S1 | TPG S0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Gain | |
| | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | UD FZC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FOCUS |
| | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | SRQ1 | SRQ0 | 0 |
| | | | 1 | 0 | 1 | 1 | SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 | 0 | Mirr, DFCT, FOK | | |
| | | | 1 | 1 | 0 | 0 | COSS | COTS | CETZ | CETF | COT2 | COT1 | MOT2 | 0 | BTS1 | BTS0 | MRC1 | MRC0 | 0 | 0 | 0 | 0 | 0 | TZC, COU, Bottom, MIRR | | |
| 1 | 1 | 0 | 1 | SFID | SFSK | THID | THSK | ABEF | TLD2 | TLD1 | TLD0 | SDF6 | SDF5 | SDF4 | SDF3 | 0 | 0 | 0 | 0 | 0 | SLD filter | | | | | |
| 1 | 1 | 1 | 0 | F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | 0 | LKIN | COIN | MDFI | MIRI | XT1D | Filter | | | | | | |
| 1 | 1 | 1 | 1 | 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | FTQ | 1 | SRO1 | 0 | AGHF | ASOT | Clock, others | | | | | | |

Command Table (\$34FX to 3FX) cont.

| Regis- ter | Command | Address 1 | Address 2 | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | |
|---------------|---------|------------|-----------|-----|-----|-----|-----------|-----|-----|-----|--------|-----------|------|------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | SYG3 | SYG2 | SYG1 | SYG0 | FI FZB3 | FI FZB2 | FI FZB1 | FI FZB0 | FI FZA3 | FI FZA2 | FI FZA1 | FI FZA0 | System GAIN |
| | | | | | | | 1 | 0 | 0 | 1 | FSUD | FFS UP | 0 | 1 | 0 | 0 | FFS5 | FFS4 | FFS3 | FFS2 | FFS1 | FFS0 | FOCUS |

Command Table (\$4X to EX)

| Regis- ter | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|---------------|--|---------|----|----|----|------------|----------------|----------------|------|----------------|---------------|-------|-------------|--------|------|------|------|--------|-------------|----|----|
| | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| 4 | Auto sequence | 0 | 1 | 0 | 0 | AS3 | AS2 | AS1 | AS0 | MT3 | MT2 | MT1 | MT0 | LSSL | 0 | 0 | 0 | — | — | — | — |
| 5 | Blind (A, E), Brake (B), Overflow (C, G) | 0 | 1 | 0 | 1 | TR3 | TR2 | TR1 | TR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| 6 | Sled KICK, BRAKE (D), KICK (F) | 0 | 1 | 1 | 0 | SD3 | SD2 | SD1 | SD0 | KF3 | KF2 | KF1 | KF0 | 0 | 0 | 0 | 0 | — | — | — | — |
| 7 | Auto sequence (N) track jump count setting | 0 | 1 | 1 | 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 8 | MODE specification | 1 | 0 | 0 | 0 | CD- ROM | DOUT Mute | DOUT Mute-F | WSEL | VCO SEL2 | ASHS | SOCT0 | VCO SEL1 | KSL3 | KSL2 | KSL1 | KSL0 | 0 | VCO1 CS0 | 0 | 0 |
| 9 | Function specification | 1 | 0 | 0 | 1 | 1 | DSPB ON-OFF | ASEQ ON-OFF | 1 | BiliGL MAIN | BiliGL SUB | FLFC | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

—: don't care

Command Table (\$4X to EX) cont.

| Regis- ter | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | |
|---------------|-------------------------------------|---------|----|----|----|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|---------------|----------------|-------------|---|
| | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | |
| A | Compression setting | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | ADPON | BITSL1 | BITSL0 | 0 | ADP WO | 0 | 0 | 0 | 0 | GRSEL | 0 | 0 | |
| | EFM playability enhancement setting | | | | | 1 | 0 | 1 | 1 | ARDTEN | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Sync expansion specification | | | | | 1 | 1 | 0 | 0 | AVW | 0 | SFP5 | SFP4 | SFP3 | SFP2 | SFP1 | SFP0 | 0 | 0 | 0 | 0 | |
| | Sleep setting | | | | | 1 | 1 | 0 | 1 | ADCPS | DSP SLEEP | DSSP SLEEP | ASYM SLEEP | ESP SLEEP | LPF SLEEP | DSUB SLEEP | ASEQ SLEEP | PCOL | HCAV SLEEP | ERCNT SLEEP | 0 | |
| | Variable pitch setting | | | | | 1 | 1 | 1 | 0 | VARI ON | VARI USE | WTC C2PO | SCSY (sub) | SENS SEL3 | SENS SEL2 | SENS SEL1 | SENS SEL0 | | | | | |
| | Spindle servo setting | | | | | 1 | 1 | 1 | 1 | SYG3 EA | SYG2 EA | SYG1 EA | SYG0 EA | MDP OUTSL1 | MDP OUTSL0 | LPWR2 | 0 | MDS CTL | MDP UP | 0 | MDP CTL4 | |
| B | Traverse monitor counter setting | 1 | 0 | 1 | 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 | Gain DCLV1 | Gain DCLV0 | PCC1 | PCC0 | SFP3 | SFP2 | SFP1 | SFP0 | SRP3 | SRP2 | SRP1 | SRP0 | |
| D | CLV CTRL | 1 | 1 | 0 | 1 | 0 | TB | TP | Gain CLVS | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | VP CTL1 | VP CTL0 | 0 | 0 | |
| E | SPD mode | 1 | 1 | 1 | 0 | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | Gain CAV1 | Gain CAV0 | 0 | INV VPCO | |

Command Table (\$4X to EX) cont.

| Register | Command | Address | Data 1 | Data 2 | Data 3 | Data 4 | Data 5 | | | | Data 6 | | | | Data 7 | | | | | |
|----------|----------------------------|---------|---------|---------|---------|--------|---------|------------|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------|--|
| | | | | | | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | | |
| 8 | MODE specification | 1 0 0 0 | | | | | ERC4 | SCOR SEL | SCSY | SOCT1 | TXON | TXOUT | OUTL1 | OUTL0 | 0 | 0 | OUTL2 | 0 | | |
| 9 | Function specification | 1 0 0 1 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIV4 | 0 | 0 | 0 | | |
| A | AUDIO CTRL | 1 0 1 0 | 0 0 * * | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | | |
| | Signal select | | 0 1 0 0 | | | | EN XSOE | CKOUT SL2 | CKOUT SL1 | SLD BBIN | max C2PO7 | max C2PO6 | max C2PO5 | max C2PO4 | max C2PO3 | max C2PO2 | max C2PO1 | max C2PO0 | | |
| | Bass boost | | 0 1 0 1 | 0 0 1 * | | | | AD3 | AD2 | AD1 | AD0 | setup | 0 | 0 | 0 | | | | | |
| | | | | 0 1 * * | | | | 0 | 1 | 0 | 0 | | | | | | | | | |
| | | | | 1 0 * * | | | | BBST Vup1 | BBST Vup0 | BBST Uth | BBST Lth | | | | | | | | | |
| | | | | 1 1 * 0 | | | | 0 | 0 | 0 | PDM INV | | | | | | | | | |
| | Headphone | | 0 1 1 0 | 0 0 1 * | | | | AD3 | AD2 | AD1 | AD0 | | | | | | | | | |
| | | | | 0 1 * * | | | | 0 | 1 | 0 | 0 | | | | | | | | | |
| | | | | 1 0 * * | | | | BBST Vup1 | BBST Vup0 | BBST Uth | BBST Lth | | | | | | | | | |
| | | | | 1 1 * 0 | | | | 0 | 0 | 0 | PDM INV | | | | | | | | | |
| | Shock-proof memory setting | | 0 1 1 1 | | | | | ADDRST SEL | ADRM0 | 0 | STA SEL | XWI H2 | XWI H1 | SPSL COM | WQR MON | A11 SEL | READ S2 | READ S1 | MON SEL | |
| | DOUT subcode-Q setting | | 1 0 0 1 | * * * * | 0 0 0 0 | | | SubQD3 | SubQD2 | SubQD1 | SubQD0 | | | | | | | | | |

—: don't care

Command Table (\$4X to EX) cont.

| Regis- ter | Command | Address | Data 1 | Data 2 | Data 3 | Data 4 | Data 5 | | | | Data 6 | | | | Data 7 | | | |
|---------------|-------------------------------------|---------|---------|---------|--------|-----------|------------|----------|----------|----------|--------|-------|-------|-------|--------|-------|-------|-------|
| | | | | | | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A | DRAM I/F | 1 0 1 0 | 1 0 0 1 | 1 1 1 0 | | | DRD11 | DRD10 | DRD9 | DRD8 | DRD7 | DRD6 | DRD5 | DRD4 | DRD3 | DRD2 | DRD1 | DRD0 |
| | | | | 1 1 1 1 | | | DADR11 | DADR10 | DADR9 | DADR8 | DADR7 | DADR6 | DADR5 | DADR4 | DADR3 | DADR2 | DADR1 | DADR0 |
| | Compression setting | | 1 0 1 0 | | | ADPCM SEL | ADPCM MUTE | 0 | 0 | 0 | ORMU | 0 | 0 | | | | | |
| | EFM playability enhancement setting | | 1 0 1 1 | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | Sync expansion specification | | 1 1 0 0 | | | | REF SEL2 | SLIM1 | SLIM0 | OV4 | OV3 | OV2 | OV1 | OV0 | | | | |
| | Spindle servo setting | | 1 1 1 1 | | | | MDP CTL3 | MDP CTL2 | MDP CTL1 | MDP CTL0 | | | | | | | | |
| B | Traverse monitor counter setting | 1 0 1 1 | | | | 0 | 0 | MTSL1 | MTSL0 | ASYE | MD2 | 0 | 0 | | | | | |
| C | Spindle servo coefficient setting | 1 1 0 0 | | | | EDC7 | EDC6 | EDC5 | EDC4 | EDC3 | EDC2 | EDC1 | EDC0 | — | — | — | — | |
| D | CLV CTRL | 1 1 0 1 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | |

—: don't care

§1-3. CPU Command Presets

Command Preset Table (\$0X to 34X)

| Regis- ter | Command | Address | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
|---------------|------------------|------------|-----------|-----|-----|-----|-----------|---|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|--|-------------------------------------|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | FOCUS CONTROL | 0 0 0 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, 0V OUT | |
| 1 | TRACKING CONTROL | 0 0 0 1 | 0 | 0 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 1 | |
| 2 | TRACKING MODE | 0 0 1 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO OFF SLED SERVO OFF | |
| Regis- ter | Command | Address | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL ($\pm 1 \times$ basic value) (default) | |
| | | Address 1 | Address 2 | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | 0 0 1 1 | 0 | 1 | 0 | 0 | 0 | See "Coefficient ROM Preset Values Table" | | | | | | | | | | | | | | | KRAM DATA (\$3400XX to \$344FXX) |

—: don't care

Command Preset Table (\$348X to 34FX)

| Regis- ter | Command | Address 1 | Address 2 | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | | | |
|---------------|---------|------------|------------|-----------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|----|------------------|----------------|--------------------|
| | | D23 to D20 | D19 to D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PGFS, PFOK, RFAC | | |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | DOUT | |
| | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Booster Surf Brake |
| | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Booster |
| | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DFCT |
| | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | | | |
| | | | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | FCS Bias Limit | |
| | | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | FCS Bias Data | | |
| | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

—: don't care

Command Preset Table (\$34FX to 3FX) cont.

| Regis- ter | Command | Address 1 | Address 2 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | | | | | |
|---------------|---------|------------|-----------|-----|-----|-----|--------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|---------------|----|----|----------------------------|---|--------------------------------------|------|-------|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | |
| 3 | SELECT | 0 0 1 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | FCS search, AGF | | | | |
| | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | TRK jump, AGT | | | | |
| | | | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | FZC, AGC, SLD move | | | | |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DC measure, cancel | | | | |
| | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Serial data read out | | | | |
| | | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FCS Bias, Gain, Surf jump / brake | | |
| | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Gain | |
| | | | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FOCUS |
| | | | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ASYO |
| | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | MIRR, DFCT, FOK | | | | |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | TZC, COUT, Bottom, MIRR | | | | |
| | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLD filter | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Filter | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Clock, others | | | | | | | |

Command Preset Table (\$34FX to 3FX) cont.

| Regis- ter | Command | Address 1 | Address 2 | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | |
|---------------|---------|------------|-----------|-----|-----|-----|-----------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|-------------|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | System GAIN | |
| | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Command Preset Table (\$4X to EX)

| Regis- ter | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|---------------|--|---------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|
| | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| 4 | Auto sequence | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| 5 | Blind (A, E), Brake (B), Overflow (C, G) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| 6 | Sled KICK, BRAKE (D), KICK (F) | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| 7 | Auto sequence (N) track jump count setting | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | MODE setting | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 9 | Function specification | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

—: dun't care

Command Preset Table (\$4X to EX) cont.

| Regis- ter | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | | | | |
|---------------|-------------------------------|---------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|---|---|---|---|
| | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | | | | |
| A | Audio CTRL | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | | |
| | Signal select | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Bass boost | | | | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Headphone | | | | | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Shock-proof memory setting | | | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Shock-proof memory control | | | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | | | | |
| | DOUT subcode-Q setting | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | DRAM I/F | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Command Preset Table (\$4X to EX) cont.

| Regis- ter | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | |
|---------------|-------------------------------------|---------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|---|
| | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | |
| A | Compression setting | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | EFM playability enhancement setting | | | | | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | |
| | Sync expansion specification | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Sleep setting | | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Variable pitch setting | | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | |
| | Spindle servo setting | | | | | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | |
| B | Traverse monitor counter setting | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| D | CLV CTRL | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| E | SPD mode | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Command Preset Table (\$4X to EX) cont.

| Regis- ter | Command | Address | Data 1 | Data 2 | Data 3 | Data 4 | Data 5 | | | | Data 6 | | | | Data 7 | | | | | |
|---------------|-------------------------------|---------|---------|---------|--------|--------|--------|----|----|----|--------|----|----|----|--------|----|----|----|---|--|
| | | | | | | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | | |
| 8 | MODE specification | 1 0 0 0 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 9 | Function specification | 1 0 0 1 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| A | AUDIO CTRL | 1 0 1 0 | 0 0 * * | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | | |
| | Signal select | | 0 1 0 0 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Bass boost | | 0 1 0 1 | 0 0 1 * | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | |
| | | | | 0 1 * * | | | | 0 | 1 | 0 | 0 | | | | | | | | | |
| | | | | 1 0 * * | | | | 0 | 0 | 0 | 0 | | | | | | | | | |
| | | | | 1 1 * 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | | |
| | Headphone | | 0 1 1 0 | 0 0 1 * | | | | 0 | 0 | 0 | 0 | | | | | | | | | |
| | | | | 0 1 * * | | | | 0 | 1 | 0 | 0 | | | | | | | | | |
| | | | | 1 0 * * | | | | 0 | 0 | 0 | 0 | | | | | | | | | |
| | | | | 1 1 * 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | | |
| | Shock-proof memory setting | | 0 1 1 1 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

—: don't care

Command Preset Table (\$4X to EX) cont.

| Register | Command | Address | Data 1 | Data 2 | Data 3 | Data 4 | Data 5 | | | | Data 6 | | | | Data 7 | | | | | |
|----------|-------------------------------------|---------|---------|---------|---------|--------|--------|----|----|----|--------|----|----|----|--------|----|----|----|---|---|
| | | | | | | | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | | |
| A | DOUT subcode-Q setting | 1 0 1 0 | 1 0 0 1 | * * * * | 0 0 0 0 | | 0 | 0 | 0 | 0 | | | | | | | | | | |
| | DRAM I/F | | | 1 1 1 0 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | 1 1 1 1 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Compression setting | | 1 0 1 0 | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | | | |
| | EFM playability enhancement setting | | 1 0 1 1 | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| | Sync expansion specification | | 1 1 0 0 | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | |
| | Spindle servo setting | | 1 1 1 1 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | |
| B | Traverse monitor counter setting | 1 0 1 1 | | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | | |
| C | Spindle servo coefficient setting | 1 1 0 0 | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | | |
| D | CLV CTRL | 1 1 0 1 | | | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | — | — | — | — | | |

—: don't care

(Coefficient ROM Preset Values Table (1))

| ADDRESS | DATA | CONTENTS |
|---------|------|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | Not used |
| K2F | 00 | Not used |

* Fix indicates that normal preset values should be used.

<Coefficient ROM Preset Values Table (2)>

| ADDRESS | DATA | CONTENTS |
|---------|------|--|
| K30 | 80 | SLED INPUT GAIN (Only when TRK gain up2 is accessed with SFSK = 1.) |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | Not used |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | Not used |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | TRACKING HOLD FILTER INPUT GAIN (Only when TRK gain up2 is accessed with THSK = 1.) |
| K47 | 00 | Not used |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | Not used |
| K4F | 00 | Not used |

§1-4. Description of SENS Signals

SENS output

| Microcomputer serial register (latching not required) | ASEQ = 0 | ASEQ = 1 | Output data length |
|---|--------------------|--|--------------------|
| \$0X | Z | FZC | — |
| \$1X | Z | AS | — |
| \$2X | Z | TZC | — |
| \$30 to \$37 | Z | SSTP | — |
| \$38 | Z | AGOK* | — |
| \$38 | Z | XAVEBSY* | — |
| \$39X | Z | See §5-18. Description of Commands and Data Sets "\$39". | 8 to 16 bits |
| \$3A | Z | FBIAS Count STOP | — |
| \$3B to \$3F | Z | SSTP | — |
| \$4X | Z | XBUSY | — |
| \$5X | Z | FOK | — |
| \$6X | Z | 0 | — |
| \$A0 to \$A8 \$AA to \$AF | GFS | GFS | — |
| \$BX | COMP | COMP | — |
| \$CX | COU \overline{T} | COU \overline{T} | — |
| \$EX | $\overline{OV64}$ | $\overline{OV64}$ | — |
| \$7X, 8X, 9X, DX, FX | Z | 0 | — |

* \$38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

| | |
|--------------------------|---|
| SENS output | |
| Z | The SENS pin is high impedance. |
| XBUSY | Low while the auto sequencer is in operation, high when operation terminates. |
| FOK | Outputs the same signal as the FOK pin. High for "focus OK". |
| GFS | High when the regenerated frame sync is obtained with the correct timing. |
| COMP | Counts the number of tracks set with Reg.B. High when Reg.B is latched, low when COUT is counted for the initial Reg.B number. |
| COUT | Counts the number of tracks set with Reg.B. High when Reg.B is latched, toggles each time COUT is counted for the Reg.B number. While \$44 and \$45 are being executed, toggles with each COUT 8-count instead of the Reg.B number. |
| $\overline{\text{OV64}}$ | Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter. |

§1-5. Description of Commands

The meaning of the data for each address on the XLAT pin side is explained below.

\$4X commands

| Register name | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|---------------|---------|-----|-----|-----|-----------------|-----|-----|-----|-------------|---|---|---|
| 4 | Command | | | | MAX timer value | | | | Timer range | | | |
| | AS3 | AS2 | AS1 | AS0 | MT3 | MT2 | MT1 | MT0 | LSSL | 0 | 0 | 0 |

| Command | AS3 | AS2 | AS1 | AS0 |
|---------------|-----|-----|-----|-----|
| Cancel | 0 | 0 | 0 | 0 |
| Fine Search | 0 | 1 | 0 | RXF |
| Focus-On | 0 | 1 | 1 | 1 |
| 1 Track Jump | 1 | 0 | 0 | RXF |
| 10 Track Jump | 1 | 0 | 1 | RXF |
| 2N Track Jump | 1 | 1 | 0 | RXF |
| M Track Move | 1 | 1 | 1 | RXF |

RXF = 0 Forward
 RXF = 1 Reverse

- When the Focus-on command (\$47) is canceled, \$02 is sent and the auto sequence is interrupted.
- When the Track jump commands (\$44, \$45 and \$48 to \$4D) are canceled, \$25 is sent and the auto sequence is interrupted.

| MAX timer value | | | | Timer range | | | |
|-----------------|--------|-------|-------|-------------|---|---|---|
| MT3 | MT2 | MT1 | MT0 | LSSL | 0 | 0 | 0 |
| 23.2ms | 11.6ms | 5.8ms | 2.9ms | 0 | 0 | 0 | 0 |
| 1.49s | 0.74s | 0.37s | 0.18s | 1 | 0 | 0 | 0 |

- To disable the MAX timer, set the MAX timer value to "0".

\$5X commands

| Timer | TR3 | TR2 | TR1 | TR0 |
|-------------------------------|--------|--------|---------|---------|
| Blind (A, E), Overflow (C, G) | 0.18ms | 0.09ms | 0.045ms | 0.022ms |
| Brake (B) | 0.36ms | 0.18ms | 0.09ms | 0.045ms |

\$6X commands

| Register name | Data 1 | | | | Data 2 | | | |
|---------------|----------|-----|-----|-----|----------|-----|-----|-----|
| 6 | KICK (D) | | | | KICK (F) | | | |
| | SD3 | SD2 | SD1 | SD0 | KF3 | KF2 | KF1 | KF0 |

| Timer | SD3 | SD2 | SD1 | SD0 |
|--------------------------------------|--------|--------|-------|--------|
| When executing KICK (D) \$44 or \$45 | 23.2ms | 11.6ms | 5.8ms | 2.9ms |
| When executing KICK (D) \$4C or \$4D | 11.6ms | 5.8ms | 2.9ms | 1.45ms |

| Timer | KF3 | KF2 | KF1 | KF0 |
|----------|--------|--------|--------|--------|
| KICK (F) | 0.72ms | 0.36ms | 0.18ms | 0.09ms |

\$7X commands

Auto sequence track jump count setting

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Auto sequence track jump count setting | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |

- This command is used to set N when a 2N-track jump is executed, to set M when an M-track move is executed and to set the jump count when fine search is executed for auto sequencer.
- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal is counted for 2N-track jumps and M-track moves; when the count is 16 or over, the MIRR signal is counted. For fine search, the COUT signal is counted.

\$8X commands

| Command | Data 1 | | | | Data 2 | | | |
|--------------------|--------|-----------|-------------|------|----------|------|-------|----------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| MODE specification | CD-ROM | DOUT Mute | DOUT Mute-F | WSEL | VCO SEL2 | ASHS | SOCT0 | VCO SEL1 |

| Command bit | C2PO timing | Processing |
|-------------|-------------|---|
| CDROM = 1 | 1-3 | CDROM mode; average value interpolation and pre-value hold are not performed. |
| CDROM = 0 | 1-3 | Audio mode; average value interpolation and pre-value hold are performed. |

| Command bit | Processing |
|---------------|---|
| DOUT Mute = 1 | When Digital Out is on (\$B MD2 = 1), DOUT output is muted. |
| DOUT Mute = 0 | When Digital Out is on, DOUT output is not muted. |

| Command bit | Processing |
|-----------------|--|
| DOUT Mute F = 1 | When Digital Out is on (\$B MD2 = 1), DA output is muted. |
| DOUT Mute F = 0 | DA output mute is not affected when Digital Out is either on or off. |

| MD2 | Other mute conditions* | DOUT Mute | DOUT Mute F | DOUT output | DA output for 48-bit slot |
|-----|------------------------|-----------|-------------|-------------|---------------------------|
| 0 | 0 | 0 | 0 | OFF | 0dB |
| 0 | 0 | 0 | 1 | | |
| 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 0 | | -∞dB |
| 0 | 1 | 0 | 1 | | |
| 0 | 1 | 1 | 0 | | |
| 0 | 1 | 1 | 1 | | |
| 1 | 0 | 0 | 0 | 0dB | 0dB |
| 1 | 0 | 0 | 1 | | -∞dB |
| 1 | 0 | 1 | 0 | -∞dB | 0dB |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |

* See "Mute conditions" (1) to (5) under \$AX commands for other mute conditions.

* When \$A4 DTSL1 = 1, the Digital Out from the bass boost or shock-proof is selected. See the description of Digital Out.

| Command bit | Sync protection window width | Application |
|-------------|------------------------------|-------------------------------------|
| WSEL = 1 | ±26 channel clock | Anti-rolling is enhanced. |
| WSEL = 0 | ±6 channel clock | Sync window protection is enhanced. |

* In normal-speed playback, channel clock = 4.3218MHz.

| Command bit | Function |
|-------------|---|
| ASHS = 0 | The command transfer rate from the auto sequencer to the DSSP block is set to normal speed. |
| ASHS = 1 | The command transfer rate from the auto sequencer to the DSSP block is set to half speed. |

* See "§4-8. CD-DSP Block Playback Speed" for settings.

| Command bit | | Processing |
|-------------|-------|--|
| SOCT0 | SOCT1 | |
| 0 | 0 | Subcode-Q is output from the SQSO pin. |
| 0 | 1 | The spindle speed measurement result is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-5.) |
| 1 | 0 | Various signals are output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-4.) |
| 1 | 1 | The error rate is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-6.) |

* \$8X command TXOUT = 0 and \$A8X command SDTO OUT = 0 must be set.

| Command | Data 2 | | | | Data 3 | | | |
|--------------------|----------|------|-------|----------|--------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| MODE specification | VCO SEL2 | ASHS | SOCT0 | VCO SEL1 | KSL3 | KSL2 | KSL1 | KSL0 |

See above.

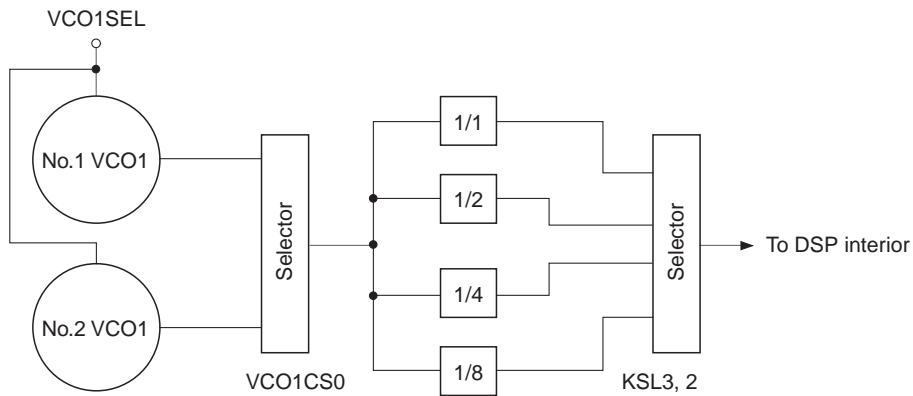
| Command bit | Processing |
|-------------|---|
| VCOSEL2 = 0 | Multiplier PLL VCO2 is set to normal speed. |
| VCOSEL2 = 1 | Multiplier PLL VCO2 is set to approximately twice the normal speed. |

| Command bit | | Processing |
|-------------|------|--|
| KSL3 | KSL2 | |
| 0 | 0 | Output of multiplier PLL VCO1 selected by VCO1 CS0 is 1/1 frequency-divided. |
| 0 | 1 | Output of multiplier PLL VCO1 selected by VCO1 CS0 is 1/2 frequency-divided. |
| 1 | 0 | Output of multiplier PLL VCO1 selected by VCO1 CS0 is 1/4 frequency-divided. |
| 1 | 1 | Output of multiplier PLL VCO1 selected by VCO1 CS0 is 1/8 frequency-divided. |

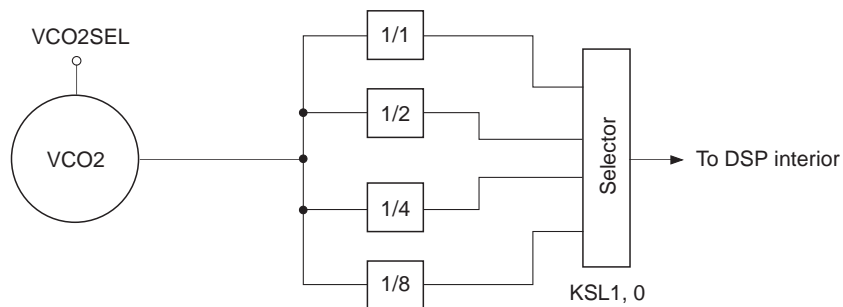
| | |
|-------------|--|
| Command bit | Processing |
| VCOSEL1 = 0 | Wide-band PLL VCO1 is set to normal speed. |
| VCOSEL1 = 1 | Wide-band PLL VCO1 is set to approximately twice the normal speed. |

| | | |
|-------------|------|--|
| Command bit | | Processing |
| KSL1 | KSL0 | |
| 0 | 0 | Output of wide-band PLL VCO2 is 1/1 frequency-divided. |
| 0 | 1 | Output of wide-band PLL VCO2 is 1/2 frequency-divided. |
| 1 | 0 | Output of wide-band PLL VCO2 is 1/4 frequency-divided. |
| 1 | 1 | Output of wide-band PLL VCO2 is 1/8 frequency-divided. |

* Block Diagram of VCO Internal Path



VCO1 internal path



VCO2 internal path

\$8X commands cont.

| Command | Data 4 | | | | Data 5 | | | | Data 6 | | | |
|--------------------|--------|----------|----|----|--------|----------|------|-------|--------|-------|-------|-------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| MODE specification | 0 | VCO1 CS0 | 0 | 0 | ERC4 | SCOR SEL | SCSY | SOCT1 | TXON | TXOUT | OUTL1 | OUTL0 |

See page 48.

| Command bit | Processing |
|-------------|-------------------------|
| VCO1CS0 = 0 | Selects the No. 1 VCO1. |
| VCO1CS0 = 1 | Selects the No. 2 VCO1. |

* The CXD3048R has two multiplier PLL VCO1s, and this command selects one of these VCO1s. The two VCOs are No. 2 and No. 1 in order of the maximum frequency.

* The block diagrams for VCO1 and VCO2 including VCOSEL1, VCOSEL2, KSL0 to KSL3 and VCO1CS0 shown on the previous page.

| Command bit | Processing |
|-------------|--|
| ERC4 = 0 | C2 error double correction is performed when DSPB = 1. |
| ERC4 = 1 | C2 error quadruple correction is performed even when DSPB = 1. |

| Command bit | Processing |
|--------------|------------------------------------|
| SCOR SEL = 0 | WDCK signal is output. |
| SCOR SEL = 1 | GRSCOR (protected SCOR) is output. |

* Used when outputting GRSCOR from the WDCK pin.

| Command bit | Processing |
|-------------|---|
| SCSY = 0 | No processing. |
| SCSY = 1 | GRSCOR (protected SCOR) synchronization is applied again. |

* Used to resynchronize GRSCOR.

The rising edge signal of this command bit is used internally, so when resynchronizing GRSCOR, first return the setting to "0" and then set to "1".

GRSCOR is the crystal accuracy SCOR signal obtained by removing the motor wow component.

This signal is synchronized with PCMDATA.

The resynchronization conditions are when GTOP = high.

| Command bit | Processing |
|-------------|--|
| TXON = 0 | When CD TEXT data is not demodulated, set TXON to "0". |
| TXON = 1 | When CD TEXT data is demodulated, set TXON to "1". |

* See "\$4-16. CD TEXT Data Demodulation".

| | |
|-------------|--|
| Command bit | Processing |
| TXOUT = 0 | Various signals except for CD TEXT are output from the SQSO pin. |
| TXOUT = 1 | CD TEXT data is output from the SQSO pin. |

* See "§4-16. CD TEXT Data Demodulation".

| | |
|-------------|------------------------------------|
| Command bit | Processing |
| OUTL1 = 0 | WDCK and XPCK are output. |
| OUTL1 = 1 | WDCK and XPCK outputs are set low. |

| | |
|-------------|---|
| Command bit | Processing |
| OUTL0 = 0 | PCMD, BCK and LRCK are output. |
| OUTL0 = 1 | PCMD, BCK and LRCK outputs are set low. |

| | | | | |
|--------------------|--------|----|-------|----|
| Command | Data 7 | | | |
| | D3 | D2 | D1 | D0 |
| MODE specification | 0 | 0 | OUTL2 | 0 |

| | |
|-------------|------------------|
| Command bit | Processing |
| OUTL2 = 0 | WFCK is output. |
| OUTL2 = 1 | WFCK is set low. |

* The \$A7X command XOE OUT must be set to "0".

\$9X commands

| Command | Data 1 | | | | Data 2 | | | |
|------------------------|--------|-------------|-------------|----|-------------|------------|------|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Function specification | 1 | DSPB ON-OFF | ASEQ ON-OFF | 1 | BiliGL MAIN | BiliGL SUB | FLFC | 0 |

| Command bit | Processing |
|-------------|---|
| DSPB = 0 | Normal-speed playback, C2 error quadruple correction. |
| DSPB = 1 | Double-speed playback, C2 error double correction. (quadruple correction when ERC4 = 1) |

Normally FLFC = 0.

In CAV-W mode, set FLFC to "1" independently of the playback speed.

| Command bit | BiliGL MAIN = 0 | BiliGL MAIN = 1 |
|----------------|-----------------|-----------------|
| BiliGL SUB = 0 | STEREO | MAIN |
| BiliGL SUB = 1 | SUB | Mute |

Definition of bilingual capable MAIN, SUB and STEREO

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels, respectively, for STEREO.

| Command | Data 3 | | | | Data 4 | | | | Data 5 | | | |
|------------------------|--------|----|----|----|--------|----|----|----|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Function specification | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Data 6 | | | | Data 7 | | | |
|--------|----|----|----|--------|----|----|----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | DIV4 | 0 | 0 | 0 |

This switches the digital PLL master clock.

Either the conventional mode or the 2/3 mode (2/3 of the conventional clock) can be selected.

| Command bit | Processing |
|-------------|---|
| DIV4 = 0 | Digital PLL master clock; conventional mode. (preset) |
| DIV4 = 1 | Digital PLL master clock; 2/3 mode. |

Note) Do not set DIV4 to "1" when DSPB = 0.

\$AX commands

| Command | Data 1 | | | | Data 2 | | | |
|------------|--------|----|------|-----|--------|------|----|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Audio CTRL | 0 | 0 | Mute | ATT | PCT1 | PCT2 | 0 | SOC2 |

| Command bit | Meaning |
|-------------|--|
| Mute = 0 | Mute off if other mute conditions are not set. |
| Mute = 1 | Mute on. Peak register reset. |

| Command bit | Meaning |
|-------------|------------------|
| ATT = 0 | Attenuation off. |
| ATT = 1 | -12dB |

Mute conditions

- (1) When register A mute = 1.
 - (2) When register 8 DOUT Mute F = 1 and Digital Out is on (\$B command MD2 = 1).
 - (3) When GFS stays low for over 35ms (during normal-speed).
 - (4) When register 9 BiliGL MAIN = Sub = 1.
 - (5) When register A PCT1 = 1 and PCT2 = 0.
- (1) to (3) perform zero-cross muting with a 1ms time limit.

| Command bit | | Meaning | PCM Gain | ECC error correction ability |
|-------------|------|------------------|----------|------------------------------|
| PCT1 | PCT2 | | | |
| 0 | 0 | Normal mode | × 0dB | C1: double; C2: quadruple |
| 0 | 1 | Level meter mode | × 0dB | C1: double; C2: quadruple |
| 1 | 0 | Peak meter mode | Mute | C1: double; C2: double |
| 1 | 1 | Normal mode | × 0dB | C1: double; C2: double |

Description of level meter mode (see Timing Chart 1-4.)

- When the LSI is set to this mode, it performs digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
The initial 80 bits are subcode-Q data (see "[2] Subcode Interface"). The last 16 bits are LSB first, which are 15-bit PCM data (absolute values) and an L/R flag.
The final bit (L/R flag) is high when the 15-bit PCM data is from the left channel and low when the data is from the right channel.
- The PCM data is reset and the L/R flag is inverted after one readout.
Then the measurement for the maximum value continues until the next readout.

Description of peak meter mode (see Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the value is set in the LSI internal register again.
In other words, the PCM maximum value register is not reset by the readout.
- To reset the PCM maximum value register to "0", set PCT1 = PCT2 = 0 or set the \$AX command Mute.
- The subcode-Q absolute time is automatically controlled in this mode.
In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally "0".
- The pre-value hold and average value interpolation data are fixed to level ($-\infty$) for this mode.

| Command bit | Processing |
|-------------|---|
| SOC2 = 0 | The SENS signal is output from the SENS pin as usual. |
| SOC2 = 1 | The SQSO pin signal is output from the SENS pin. |

SENS output switching

- This command is used to output the SQSO pin signal from the SENS pin.
When SOC2 = 0, SENS output is performed as usual.
When SOC2 = 1, the SQSO pin signal is output from the SENS pin.
At this time, the readout clock is input to the SCLK pin.

Note) Perform the SOC2 switching when SQCK = SCLK = high.

| Command | Data 3 | | | | Data 4 | | | | Data 5 | | | | Data 6 | | | |
|------------|--------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Audio CTRL | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

\$A4 commands (preset: \$A4C800)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-----------------------|--------|----|----|----|--------|------|----|----|--------|------|------|------|--------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A4 (Signal select) | 0 | 1 | 0 | 0 | RSL1 | RSL0 | 0 | 0 | DTSL | DTSL | MCSL | MCSL | 0 | SDSL | SDSL | SDSL |
| | | | | | | | | | 1 | 0 | 1 | 0 | | 2 | 1 | 0 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|--------|-------|-------|------|--------|-------|-------|-------|--------|-------|-------|-------|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| EN | CKOUT | CKOUT | SLD | max | max | max | max | max | max | max | max |
| XSOE | SL2 | SL1 | BBIN | C2P07 | C2P06 | C2P05 | C2P04 | C2P03 | C2P02 | C2P01 | C2P00 |

RSL1, RSL0: These bits set the external buffer RAM.

| RSL1 | RSL0 | Processing |
|------|------|---|
| 0 | 0 | The external buffer RAM is set to 4M bits. |
| 1 | 0 | No selected. |
| 1 | 1 | The external buffer RAM is set to 16M bits. |

*: preset

DTSL1, DTSL0: See the second half of the description of \$A4 commands.

MCSL1: This bit sets the DAC block master clock.

When "0", the DAC block master clock is set to 16.9344MHz (384fs). (default)

When "1", the DAC block master clock is set to 33.8688MHz (768fs).

MCSL0: This bit sets the shock-proof memory controller block master clock.

When "0", the shock-proof memory controller block master clock is set to 16.9344MHz (384fs). (default)

When "1", the shock-proof memory controller block master clock is set to 33.8688MHz (768fs).

ENXSOE: This bit switches the command input method.

When "0", the command transfer clock and the SENS serial data readout clock are input from the respective pins. (default)

When "1", the command transfer clock and the SENS serial data readout clock are input from the CLOK pin.

The clock input is switched with the XSOE pin. At this time, connect the SCLK pin to high.

| ENXSOE | XSOE pin | CLOK pin | SCLK pin |
|--------|----------|--------------------------------------|--------------------------------------|
| 0 | L | Command transfer clock input | SENS serial data readout clock input |
| 0 | H | Command transfer clock input | SENS serial data readout clock input |
| 1 | L | SENS serial data readout clock input | Connect to high. |
| 1 | H | Command transfer clock input | Connect to high. |

In addition, when ENXSOE is set to "1" and the SQSO pin signal output is read from the SENS pin, the command input method is as follows.

At this time, connect the SCLK and SQCK pins to high.

See the command descriptions for \$A command SOC2 and \$8 commands TXOUT, SOCT0 and SOCT1.

| ENXS OE | XSOE pin | \$A SOC2 | \$A8 SDTO OUT | \$8 TX OUT | \$8 SOC T0 | \$8 SOC T1 | CLOCK pin | SENS pin |
|------------|-------------|-------------|---------------------|------------------|------------------|------------------|--|--|
| 1 | H | * | * | * | * | * | Command transfer clock input | High or low output |
| 1 | L | 0 | * | * | * | * | SENS serial data readout clock input | SENS output*1 |
| 1 | L | 1 | 0 | 0 | 0 | 0 | Subcode-Q readout clock input | Subcode-Q output |
| 1 | L | 1 | 0 | 0 | 0 | 1 | Readout clock input of the spindle speed measurement result | Spindle speed measurement result output*2 |
| 1 | L | 1 | 0 | 0 | 1 | 0 | Various signal readout clock input | Various signal output*3 |
| 1 | L | 1 | 0 | 0 | 1 | 1 | Error rate readout clock input | Error rate output*4 |
| 1 | L | 1 | 0 | 1 | * | * | CD TEXT data readout clock input | CD TEXT data output |
| 1 | L | 1 | 1 | * | * | * | Readout clock input of shock-proof memory controller serial data | Shock-proof memory controller serial data output |

*: don't care

*1 See "§1-4. Description of SENS Signals" for the SENS output.

*2 See Timing Chart 2-5 for the spindle speed measurement result.

*3 The output signals are PER7 to PER0, FOK, GFS, LOCK, EMPH, ALOCK and VF9 to VF0. For details, see Timing Chart 2-4.

*4 For the error rate timing, see Timing Chart 2-6.

CKOUTSL2, CKOUTSL1:

These bits select the clock output from the R4M pin.

When the crystal is 16.9344MHz and XTSL = high, the output frequency is halved.

| CKOUTSL2 | CKOUTSL1 | Processing |
|----------|----------|--|
| 0 | 0 | 4.2336MHz output |
| 0 | 1 | 8.4672MHz (R8M) output |
| 1 | 0 | 4.2336MHz (C4M) output |
| 1 | 1 | Changes in CAV-W mode and variable pitch mode. |

*: preset

DTSL1, DTSL0: These bits select the data output from the DOUT pin.

In external mode, the data input through the LRCKI, BCKI and PCMDI pins is used.

DOUT output in the following tables is valid when \$34A commands DOUT EN1 and DOUT EN2 are both 1. In this case, see "\$34A commands".

When \$34A commands DOUT EN1 and DOUT EN2 are both 0, see "§4-5-2. Digital Out from DA Interface Input".

At this time, the data from the CD DSP is output from the DOUT pin with a subcode is added.

SDSL2, SDSL1: These bits select the data input to the DAC block and the data output from the PCMD pin.

SLDBBIN: This bit selects the data input to the DAC block and the data output from the PCMD and DOUT pins.

max C2PO7 to max C2PO0:

These bits set the C2PO conditions.

| | |
|------------------------|---|
| max C2PO7 to max C2PO0 | Ptrocessing |
| 00000000 to 11111111 | The C2PO upper limit value reflected to mon C2PO and added to the write prohibited condition. |

When SLDBBIN = 0, the internally connected data is selected. (default)

| DTSL1 | DTSL0 | SDSL2 | SDSL1 | SDSL0 | Input to DAC block | DOUT output | PCMD output | |
|-------|-------|-------|-------|-------|------------------------------------|--|--|--|
| 0 | 0 | 0 | 0 | 0 | DSP mode | DSP & DAC mode | DSP mode | |
| 0 | 0 | 0 | 1 | *1 | | | DSP & DAC mode | |
| 0 | 0 | 1 | 0 | 0 | Shock-proof memory controller mode | Shock-proof memory controller & DAC mode | Shock-proof memory controller mode | |
| 0 | 0 | 1 | 1 | *1 | | | Shock-proof memory controller & DAC mode | |
| 0 | 1 | 0 | 0 | 0 | DSP mode | DSP mode | DSP mode | |
| 0 | 1 | 0 | 1 | *1 | | | DSP & DAC mode | |
| 0 | 1 | 1 | 0 | 0 | Shock-proof memory controller mode | Shock-proof memory controller mode | Shock-proof memory controller mode | |
| 0 | 1 | 1 | 1 | *1 | | | Shock-proof memory controller & DAC mode | |
| * | 1 | 0 | 0 | 0 | DSP mode | DSP mode | DSP mode | |
| | 1 | 0 | 0 | *1 | | | DSP & DAC mode | |
| | 1 | 0 | 1 | 0 | Shock-proof memory controller mode | | Shock-proof memory controller mode | |
| | 1 | 0 | 1 | *1 | | | Shock-proof memory controller & DAC mode | |
| | 1 | 1 | 0 | 0 | DSP mode | | External mode | DSP mode |
| | 1 | 1 | 0 | *1 | | | | DSP & DAC mode |
| | 1 | 1 | 1 | 0 | Shock-proof memory controller mode | | | Shock-proof memory controller mode |
| | 1 | 1 | 1 | *1 | | | | Shock-proof memory controller & DAC mode |

*: preset

*1: The relationship between LRCK, BCK and PCMD changes according to the setting value.

When SDSL0 = 0, the LRCK, BCK and PCMD phase difference is constant but the LRCK frequency changes when SDSL0 is switched.

When SDSL0 = 1, the LRCK frequency is constant but the phase difference between LRCK, BCK and PCMD changes before and after SDSL1 is switched. When not switching the output data selection, set SDSL1 and SDSL0 to the same value.

When SLDBBIN = 1, the data input from the LRCKI, BCKI and PCMDI pins is selected.

| DTSL1 | DTSL0 | SDSL2 | SDSL1 | SDSL0 | Input to DAC block | DOUT output | PCMD output |
|-------|-------|-------|-------|-------|--------------------|------------------------------------|------------------------------------|
| 0 | 0 | 0 | 0 | 0 | External mode | External & DAC mode | DSP mode |
| 0 | 0 | 0 | 1 | *1 | | | External & DAC mode |
| 0 | 0 | 1 | 0 | 0 | | | Shock-proof memory controller mode |
| 0 | 0 | 1 | 1 | *1 | | | External & DAC mode |
| 0 | 1 | 0 | 0 | 0 | | DSP mode | DSP mode |
| 0 | 1 | 0 | 1 | *1 | | External & DAC mode | |
| 0 | 1 | 1 | 0 | 0 | | Shock-proof memory controller mode | Shock-proof memory controller mode |
| 0 | 1 | 1 | 1 | *1 | | External & DAC mode | |
| 1 | 0 | 0 | 0 | 0 | | DSP mode | DSP mode |
| 1 | 0 | 0 | 1 | *1 | | | External & DAC mode |
| 1 | 0 | 1 | 0 | 0 | | | Shock-proof memory controller mode |
| 1 | 0 | 1 | 1 | *1 | | | External & DAC mode |
| 1 | 1 | 0 | 0 | 0 | | External mode | DSP mode |
| 1 | 1 | 0 | 1 | *1 | | | External & DAC mode |
| 1 | 1 | 1 | 0 | 0 | | | Shock-proof memory controller mode |
| 1 | 1 | 1 | 1 | *1 | | | External & DAC mode |

*1: The relationship between LRCK, BCK and PCMD changes according to the setting value.

When SDSL0 = 0, the LRCK, BCK and PCMD phase difference is constant but the LRCK frequency changes when SDSL0 is switched.

When SDSL0 = 1, the LRCK frequency is constant but the phase difference between LRCK, BCK and PCMD changes before and after SDSL1 is switched. When not switching the output data selection, set SDSL1 and SDSL0 to the same value.

\$A5 commands (when Data 2 D3 = 0, D2 = 0) (preset: \$A504000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------|--------|----|----|----|--------|----|----|-----------|--------|------|-----|-----|--------|-----|-----|-----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A5 (Bass boost) | 0 | 1 | 0 | 1 | 0 | 0 | 1 | ZMUT A | SMUT | AD10 | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 |

| Data 5 | | | | Data 6 | | | |
|--------|-----|-----|-----|--------|----|----|----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AD3 | AD2 | AD1 | AD0 | setup | 0 | 0 | 0 |

- ZMUTA:** This bit sets the zero detection analog mute on/off.
 When "0", zero detection analog mute is on. (default)
 When "1", zero detection analog mute is off.
 When zero data is detected for both the left and right channels, the LPF block output is set to center output.
- SMUT:** This bit sets the soft mute on/off.
 When "0", soft mute is off. (default)
 When "1", soft mute is on.
- AD10 to AD0:** These bits set the attenuation data. The attenuation data consists of 11 bits, and is set as follows.

| Attenuation data | Audio output |
|------------------|--------------|
| 7FF (h) | +6.02dB |
| 7FE (h) | +6.016dB |
| ⋮ | ⋮ |
| 402 (h) | +0.017dB |
| 401 (h) | +0.0085dB |
| * 400 (h) | 0dB |
| 3FF (h) | -0.0085dB |
| 3FE (h) | -0.017dB |
| ⋮ | ⋮ |
| 001 (h) | -60.206dB |
| 000 (h) | -∞ |

*: preset

The audio output from 001 (h) to 7FF (h) is obtained using the following equation:

$$\text{Audio data output} = 20 \log \frac{\text{Attenuation data}}{1024} \text{ [dB]}$$

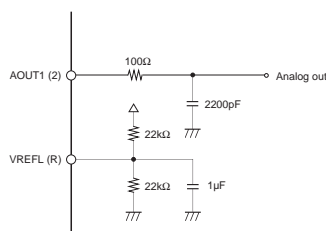
- setup:** This bit can shorten the rise time of the VREFL and VREFR pins.
 When "0", the rise time is not shortened. (default) (Recommendation setting when the external capacitance is 1μF or less.)
 When "1", the rise time is shortened. (Recommendation setting when the external capacitance exceeds 1μF.)
 Return setup to 0 after the VREFL and VREFR pins rise. (setup = 0 for normal use)

\$A5 commands (when Data 2 D3 = 0, D2 = 1) (preset: \$A540A4)

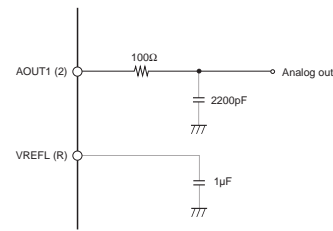
| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------|--------|----|----|----|--------|----|------|------|--------|-------------|-----------------|-----------|--------|------------|-----------|-----------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A5 (Bass boost) | 0 | 1 | 0 | 1 | 0 | 1 | PWDN | ZDPL | WOC | DAC EMPH | HiCut FILTER | BST CL | 1 | PDM SEL | OBIT 1 | OBIT 0 |

| Data 5 | | | |
|--------|----|----|----|
| D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 |

- PWDN:** This bit sets the DAC block operation mode.
When "0", the DAC block clock is stopped. This makes it possible to reduce power consumption. (default)
The zero detection flag for the headphone volume circuit side is output from the LRMU pin.
When "1", the DAC block operates normally.
- ZDPL:** This bit sets the zero detection flag polarity.
When "0", the LRMU pin is set low during mute. (default)
When "1", the LRMU pin is set high during mute.
- WOC:** When WOC = 1, the DAC sync window opens. This is used to synchronize the DAC.
- DAC EMPH:** This bit sets the digital de-emphasis on/off.
When "0", digital de-emphasis is off. (default)
When "1", digital de-emphasis is on.
- HiCutFILTER:** This bit sets the high-cut filter on/off.
When "0", the high-cut filter is off. (default)
When "1", the high-cut filter is on.
- BSTCL:** This bit sets the bass boost level clear on/off.
1: On; the set bass boost level is cleared to 0dB.
0: Off; normal operation (default)
- PDMSEL:** This bit switches the PDM signal output from the DAC block.
When "0", connect the external resistors and capacitors to the VREFL and VREFR pins. (default)
When "1", connect the external capacitors to the VREFL and VREFR pins.



LPF external circuit example (PDMSEL = 0)



LPF external circuit example (PDMSEL = 1)

- OBIT1, OBIT0:** These bits set the word length of the serial data output from the PCMD pin.
The serial data word length can be selected only when the data output from the PCMD pin is set to DAC output.

| OBIT1 | OBIT0 | Serial data word length |
|-------|-------|-------------------------|
| 0 | 0 | 20 bits |
| 0 | 1 | 18 bits |
| 1 | 0 | 16 bits |

*

*: preset

\$A5 commands (when Data 2 D3 = 1, D2 = 0) (preset: \$A58000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------|--------|----|----|----|--------|----|-------|-------|--------|-------|-------|-------|--------|-------|------------|------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A5 (Bass boost) | 0 | 1 | 0 | 1 | 1 | 0 | BBON1 | BBON0 | HBON1 | HBON0 | BBSL1 | BBSL0 | HBSL1 | HBSL0 | BBST Vdwn1 | BBST Vdwn0 |

| Data 5 | | | |
|-----------|-----------|----------|----------|
| D3 | D2 | D1 | D0 |
| BBST Vup1 | BBST Vup0 | BBST Uth | BBST Lth |

BBON1, BBON0: These bits set the bass boost on/off and the turnover frequency.

| | BBON1 | BBON0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | Bass boost is off. |
| | 0 | 1 | Bass boost is on and the turnover frequency is set to 125Hz. |
| | 1 | 0 | Bass boost is on and the turnover frequency is set to 160Hz. |
| | 1 | 1 | Bass boost is on and the turnover frequency is set to 200Hz. |

*: preset

HBON1, HBON0: These bits set the high boost on/off and the turnover frequency.

| | HBON1 | HBON0 | Processing |
|---|-------|-------|---|
| * | 0 | 0 | High boost is off. |
| | 1 | 0 | High boost is on and the turnover frequency is set to 5kHz. |
| | 1 | 1 | High boost is on and the turnover frequency is set to 7kHz. |

*: preset

BBSL1, BBSL0: These bits set the boost level for bass boost.

| | BBSL1 | BBSL0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | The boost level for bass boost is set to 10dB. |
| | 0 | 1 | The boost level for bass boost is set to 14dB. |
| | 1 | 0 | The boost level for bass boost is set to 18dB. |
| | 1 | 1 | The boost level for bass boost is set to 22dB. |

*: preset

HBSL1, HBSL0: These bits set the boost level for high boost.

| | HBSL1 | HBSL0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | The boost level for high boost is set to 4dB. |
| | 0 | 1 | The boost level for high boost is set to 6dB. |
| | 1 | 0 | The boost level for high boost is set to 8dB. |
| | 1 | 1 | The boost level for high boost is set to 10dB. |

*: preset

BBST Vdwn1, BBST Vdwn0: These bits set the boost attack time (Vol Down) for bass and high boost.

| | BBST Vdwn1 | BBST Vdwn0 | Processing |
|---|------------|------------|---|
| * | 0 | 0 | The boost attack time for bass and high boost is set to standard. |
| | 0 | 1 | The boost attack time for bass and high boost is set to fast. |
| | 1 | 1 | The boost attack time for bass and high boost is set to slow. |

*: preset

BBST Vup1, BBST Vup0: These bits set the boost release time (Vol Up) for bass and high boost.

| | BBST Vup1 | BBST Vup0 | Processing |
|---|-----------|-----------|--|
| * | 0 | 0 | The boost release time for bass and high boost is set to standard. |
| | 0 | 1 | The boost release time for bass and high boost is set to fast. |
| | 1 | 1 | The boost release time for bass and high boost is set to slow. |

*: preset

BBST Uth: This bit sets the bass and high boost Uth.
When "0", Uth is set to -1.9dB. (default)
When "1", Uth is set to -0.9dB.

BBST Lth: This bit sets the bass and high boost Lth.
When "0", Lth is set to -12dB. (default)
When "1", Lth is set to -4.4dB.

* When the volume rises above Uth, the boost level is reduced. The speed at which the boost level is reduced is the attack time.

When the volume falls below Lth, the boost level is increased up to the setting value. The speed at which the boost level is increased is the release time.

\$A5 commands (when Data 2 D3 = 1, D2 = 1) (preset: \$A5C000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------|--------|----|----|----|--------|----|------------|----|--------|----|----|----|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A5 (Bass boost) | 0 | 1 | 0 | 1 | 1 | 1 | COMP ON | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Data 5 | | | |
|--------|----|----|------------|
| D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | PDM INV |

COMP ON: This bit sets the compressor on/off.
When "0", the compressor is off. (default)
When "1", the compressor is on.

PDM INV: This bit sets the DAC block PDM signal polarity.
When "0", the polarity is set to non-inverted. (default)
When "1", the polarity is set to inverted.

\$A6 commands (when Data 2 D3 = 0, D2 = 0) (preset: \$A604000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------|--------|----|----|----|--------|----|----|----|--------|------|-----|-----|--------|-----|-----|-----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A6 (Headphone) | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | SMUT | AD10 | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 |

| Data 5 | | | |
|--------|-----|-----|-----|
| D3 | D2 | D1 | D0 |
| AD3 | AD2 | AD1 | AD0 |

SMUT: This bit sets the soft mute on/off.
 When "0", soft mute is off. (default)
 When "1", soft mute is on.

AD10 to AD0: These bits set the attenuation data. The attenuation data consists of 11 bits, and is set as follows.

| Attenuation data | Audio output |
|------------------|--------------|
| 7FF (h) | +6.02dB |
| 7FE (h) | +6.016dB |
| ⋮ | ⋮ |
| 402 (h) | +0.017dB |
| 401 (h) | +0.0085dB |
| * 400 (h) | 0dB |
| 3FF (h) | -0.0085dB |
| 3FE (h) | -0.017dB |
| ⋮ | ⋮ |
| 001 (h) | -60.206dB |
| 000 (h) | -∞ |

*: preset

The audio output from 001 (h) to 7FF (h) is obtained using the following equation:

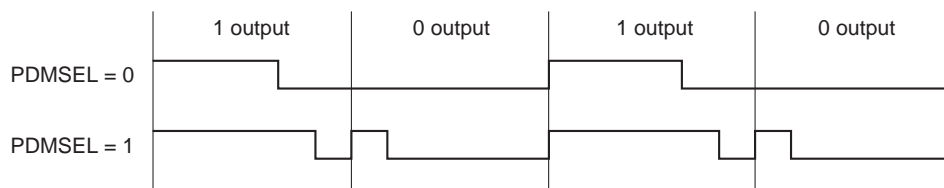
$$\text{Audio data output} = 20 \log \frac{\text{Attenuation data}}{1024} \text{ [dB]}$$

\$A6 commands (when Data 2 D3 = 0, D2 = 1) (preset: \$A640A4)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------|--------|----|----|----|--------|----|------|------|--------|-------------|-----------------|-----------|--------|------------|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A6 (Headphone) | 0 | 1 | 1 | 0 | 0 | 1 | PWDN | ZDPL | WOC | DAC EMPH | HiCut FILTER | BST CL | 1 | PDM SEL | 0 | 0 |

| Data 5 | | | |
|--------|----|----|----|
| D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 |

- PWDN: This bit sets the headphone block operation mode.
When "0", the headphone block clock is stopped. This makes it possible to reduce power consumption. (default)
When "1", the headphone block operates normally.
- ZDPL: This bit sets the zero detection flag polarity. The zero detection flag for the headphone volume circuit is output from the LRMU pin when \$A6 PWDN = 0.
When "0", the LRMU pin is set low during mute. (default)
When "1", the LRMU pin is set high during mute.
- WOC: When WOC = 1, the headphone sync window opens. This is used to synchronize the DAC.
- DAC EMPH: This bit sets the digital de-emphasis on/off.
When "0", digital de-emphasis is off. (default)
When "1", digital de-emphasis is on.
- HiCutFILTER: This bit sets the high-cut filter on/off.
When "0", the high-cut filter is off. (default)
When "1", the high-cut filter is on.
- BSTCL: This bit sets the bass boost level clear on/off.
1: On; the set bass boost level is cleared to 0dB.
0: Off; normal operation (default)
- PDMSEL This bit switches the PDM signal output from the headphone block.



Left channel side waveform (Right channel side waveform is inverted.)

\$A6 commands (when Data 2 D3 = 1, D2 = 0) (preset: \$A68000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------|--------|----|----|----|--------|----|-------|-------|--------|-------|-------|-------|--------|-------|------------|------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A6 (Headphone) | 0 | 1 | 1 | 0 | 1 | 0 | BBON1 | BBON0 | HBON1 | HBON0 | BBSL1 | BBSL0 | HBSL1 | HBSL0 | BBST Vdwn1 | BBST Vdwn0 |

| Data 5 | | | |
|-----------|-----------|----------|----------|
| D3 | D2 | D1 | D0 |
| BBST Vup1 | BBST Vup0 | BBST Uth | BBST Lth |

BBON1, BBON0: These bits set the bass boost on/off and the turnover frequency.

| | BBON1 | BBON0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | Bass boost is off. |
| | 0 | 1 | Bass boost is on and the turnover frequency is set to 125Hz. |
| | 1 | 0 | Bass boost is on and the turnover frequency is set to 160Hz. |
| | 1 | 1 | Bass boost is on and the turnover frequency is set to 200Hz. |

*: preset

HBON1, HBON0: These bits set the high boost on/off and the turnover frequency.

| | HBON1 | HBON0 | Processing |
|---|-------|-------|---|
| * | 0 | 0 | High boost is off. |
| | 1 | 0 | High boost is on and the turnover frequency is set to 5kHz. |
| | 1 | 1 | High boost is on and the turnover frequency is set to 7kHz. |

*: preset

BBSL1, BBSL0: These bits set the boost level for bass boost.

| | BBSL1 | BBSL0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | The boost level for bass boost is set to 10dB. |
| | 0 | 1 | The boost level for bass boost is set to 14dB. |
| | 1 | 0 | The boost level for bass boost is set to 18dB. |
| | 1 | 1 | The boost level for bass boost is set to 22dB. |

*: preset

HBSL1, HBSL0: These bits set the boost level for high boost.

| | HBSL1 | HBSL0 | Processing |
|---|-------|-------|--|
| * | 0 | 0 | The boost level for high boost is set to 4dB. |
| | 0 | 1 | The boost level for high boost is set to 6dB. |
| | 1 | 0 | The boost level for high boost is set to 8dB. |
| | 1 | 1 | The boost level for high boost is set to 10dB. |

*: preset

BBST Vdwn1, BBST Vdwn0:

These bits set the boost attack time (Vol Down) for bass and high boost.

| BBST Vdwn1 | BBST Vdwn0 | Processing |
|------------|------------|---|
| * 0 | 0 | The boost attack time for bass and high boost is set to standard. |
| 0 | 1 | The boost attack time for bass and high boost is set to fast. |
| 1 | 1 | The boost attack time for bass and high boost is set to slow. |

*: preset

BBST Vup1, BBST Vup0:

These bits set the boost release time (Vol Up) for bass and high boost.

| BBST Vup1 | BBST Vup0 | Processing |
|-----------|-----------|--|
| * 0 | 0 | The boost release time for bass and high boost is set to standard. |
| 0 | 1 | The boost release time for bass and high boost is set to fast. |
| 1 | 1 | The boost release time for bass and high boost is set to slow. |

*: preset

BBST Uth: This bit sets the bass and high boost Uth.
 When "0", Uth is set to -1.9dB. (default)
 When "1", Uth is set to -0.9dB.

BBST Lth: This bit sets the bass and high boost Lth.
 When "0", Lth is set to -12dB. (default)
 When "1", Lth is set to -4.4dB.

* When the volume rises above Uth, the boost level is reduced. The speed at which the boost level is reduced is the attack time.

When the volume falls below Lth, the boost level is increased up to the setting value. The speed at which the boost level is increased is the release time.

\$A6 commands (when Data 2 D3 = 1, D2 = 1) (preset: \$A6C000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|----------------|--------|----|----|----|--------|----|---------|----|--------|----|----|----|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A6 (Headphone) | 0 | 1 | 1 | 0 | 1 | 1 | COMP ON | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Data 5 | | | |
|--------|----|----|---------|
| D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | PDM INV |

COMP ON: This bit sets the compressor on/off.
 When "0", the compressor is off. (default)
 When "1", the compressor is on.

PDM INV: This bit sets the headphone block PDM signal polarity.
 When "0", the polarity is set to non-inverted. (default)
 When "1", the polarity is set to inverted.

\$A7 commands (preset: \$A7200000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|---------------------------------------|--------|----|----|----|------------|------------|---------------|---------------|-------------|-----------|------------|-----------|------------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A7 (Shock-proof memory setting) | 0 | 1 | 1 | 1 | SL XQOK | SL XWRE | GTOP CHECK | NOLIM WDCK | SPSL COM | READ 2 | REF SEL | REF ON | XOE OUT | MSL2 | MSL1 | MSL0 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|---------------|-----------|----|------------|-----------|-----------|-------------|------------|------------|------------|------------|------------|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| ADDRST SEL | ADR MO | 0 | STA SEL | XWI H2 | XWI H1 | SPSL COM | WQR MON | A11 SEL | READ S2 | READ S1 | MON SEL |

- SL XQOK: This bit sets the XQOK control mode.
When "0", XQOK should be controlled for the period from when SCOR goes high until GRSCOR goes high. (default)
When "1", XQOK should be controlled for the period while GRSCOR is high.
- SL XWRE: This bit sets the XWRE control mode.
When "0", XWRE should be controlled for the period from when SCOR goes high until GRSCOR goes high. (default)
When "1", XWRE should be controlled for the period while GRSCOR is high.
- GTOP CHECK: This bit controls GRSCOR generation when GTOP is high.
When "0", the GRSCOR generation circuit is not resynchronized even when GTOP is high.
When "1", the GRSCOR generation circuit is resynchronized when GTOP goes high. (default)
- NOLIM WDCK: Always set to "1".
- SPSL COM: This bit sets whether to control XQOK, XWRE and XRDE with pins or serial data.
When "0", XQOK, XWRE and XRDE should be controlled with pins. (default)
When "1", XQOK, XWRE and XRDE should be controlled with serial data (\$A8).
Note) The Data 3 D3 and Data 6 D1 bits should be switched simultaneously.
- READ2,
READS2, READS1: This bit sets the audio data readout speed from the shock-proof memory controller block.

| | READ2 | READS2 | READS1 | Readout speed setting |
|---|-------|--------|--------|-----------------------|
| * | 0 | 0 | 0 | 1× speed readout |
| | 0 | 0 | 1 | 0.5× speed readout |
| | 0 | 1 | 0 | 0.25× speed readout |
| | 0 | 1 | 1 | — |
| | 1 | * | * | 2× speed readout |

*: preset

The shock-proof memory controller interior should be resynchronized after the readout speed is switched. Execute the \$AAX ADPWO command for resynchronization.

REF SEL: This bit sets the DRAM refresh rate. (Use this bit in conjunction with the \$AC command REFSEL2.)

| REFSEL2 | REFSEL | Refresh rate |
|---------|--------|--------------------|
| 0 | 0 | 11.51ms/2048 times |
| 0 | 1 | 5.81ms/2048 times |
| 1 | 0 | 46.44ms/2048 times |
| 1 | 1 | 23.22ms/2048 times |

*: preset

REF ON: This bit sets the DRAM refresh function on/off.
 When "0", the refresh function is off. (default)
 When "1", the refresh function is on.

XOE OUT: This bit switches the WFCK pin output mode.
 When "0", WFCK is output from the WFCK pin. (default)
 When "1", XOE is output from the WFCK pin.

MSL2 to MSL0: These bits set the DRAM area that can be accessed from the microcomputer.

| MSL2 | MSL1 | MSL0 | DRAM area that can be accessed from the microcomputer |
|------|------|------|---|
| 0 | 0 | 0 | The entire DRAM area can be used as audio data. |
| 0 | 0 | 1 | 32K bits |
| 0 | 1 | 0 | 64K bits |
| 0 | 1 | 1 | 128K bits |
| 1 | 0 | 0 | 256K bits |
| 1 | 0 | 1 | 512K bits |
| 1 | 1 | 0 | 1M bits |
| 1 | 1 | 1 | 2M bits |

*: preset

ADDRST SEL: This bit selects the address reset mode.
 When "0", the conventional address reset is used. (default)
 When "1", the address is reset by the ADDRST command.

ADRM0: This bit selects the remaining valid addresses.
 When "0", the conventional remaining valid addresses are displayed. (default)
 When "1", the remaining addresses from 0000000 to 11111111 are displayed.

XWIH2: The XWIH condition addition is selected.
 When "0", the condition is added. (default)
 When "1", the write speed condition is added to the write prohibited condition.

XWIH1: The XWIH condition addition is selected.
 When "0", the condition is not added. (default)
 When "1", the condition of failure access to DRAM is added to the write prohibited condition.

WQR MON: This bit selects the XWRE, XQOK and XRDE outputs.
 When "0", XWRE, XQOK and XRDE output is prohibited. (default)
 When "1", XWRE, XQOK and XRDE output is allowed.

A11 SEL: This bit selects the A11 pin function.
 When "0", the A11 pin is used as the A11 pin. (default)
 When "1", the A11 pin is used as a low-active write prohibit factor.

STA SEL: This bit selects the shock-proof memory controller status output.
 When "1", the conventional ESP status is output. (See §4-13-3.)
 When "0", the new shock-proof memory controller status is output. (default)
 The status readout when STA SEL = 0 is as follows.

| | Signal | Description |
|-----|-----------|--|
| D0 | XWPHD | 0: Write prohibited |
| D1 | QRCVD | 1: Address updated |
| D2 | XEMP | 0: No valid data |
| D3 | monGRSCOR | 1: GRSCOR present |
| D4 | monC2PO | 1: C2PO of the setting value or higher present |
| D5 | GTOP | 1: GTOP present in the preceding GRSCOR |
| D6 | — | Don't care. |
| D7 | AM13 | Address monitor |
| D8 | AM14 | Address monitor |
| D9 | AM15 | Address monitor |
| D10 | AM16 | Address monitor |
| D11 | AM17 | Address monitor |
| D12 | AM18 | Address monitor |
| D13 | AM19 | Address monitor |
| D14 | AM20 | Address monitor |
| D15 | AM21 | Address monitor |
| D16 | — | Don't care. |
| D17 | — | Don't care. |
| D18 | monADPCM | 1: ADPCM compression error |
| D19 | XFUL | 0: No write area |
| D20 | ROF | 1: The DSP SRAM has overflowed. |
| D21 | SPOVER | 1: The speed limit is exceeded for more than the set number during one GRSCOR. |
| D22 | NOWR | 1: Access is failed in the shock-proof memory controller. |
| D23 | — | Don't care. |

MONSEL: This bit selects the COUT, XUGF, MIRR and XPCK pin functions.
 When "0", these pins output the signals corresponding to the SRO1, MTSL1 and MTSL0 commands. (See the table on page 8.)
 When "1", these pins output SCOR, QRCVD and GTOP, respectively.

\$A8 commands (preset: \$A8F8)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|---------------------------------------|--------|----|----|----|--------|------|------|-------|------------|------------|----|-------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A8 (Shock-proof memory control) | 1 | 0 | 0 | 0 | XQOK | XWRE | XRDE | XSOEO | XSOEO 2 | ADDR ST | 0 | SDTO OUT |

XQOK, XWRE, XRDE:

When \$A7 command SPSL COM = 1, XQOK, XWRE and XRDE are controlled with serial data. (default: 1)

XSOEO: This bit controls the serial data from the shock-proof block.

Shock-proof block data is loaded to the serial readout register by detecting the falling edge of XSOEO.

XSOEO2: This bit is used when the microcomputer reads data from the DRAM. (default: 1)

The shock-proof memory controller block loads the data from the DRAM to the serial readout register by detecting the fall of XSOEO2.

ADDRST: This command is valid when \$A7 command ADDRST SEL = 1.

When "0", no operations are performed. (default)

When "1", the VWA, WA and RA are all reset.

SDTO OUT: This bit is used to output serial data from the shock-proof block to the SQSO pin.

When "0", various signals are output from the SQSO pin. For details on these signals, see \$8X commands SOCT1, SOCT0 and TXOUT. (default)

When "1", the shock-proof block serial data is output from the SQSO pin.

\$A9 commands (preset: \$A90000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------------------|--------|----|----|----|---------|---------|---------|---------|--------|----|----|----|---------|---------|---------|---------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A9 (DOUT subcode-Q setting) | 1 | 0 | 0 | 1 | SubQ A3 | SubQ A2 | SubQ A1 | SubQ A0 | 0 | 0 | 0 | 0 | SubQ D7 | SubQ D6 | SubQ D5 | SubQ D4 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|---------|---------|---------|---------|--------|----|----|----|--------|----|----|----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| SubQ D3 | SubQ D2 | SubQ D1 | SubQ D0 | | | | | | | | |

SubQA3 to SubQA0, SubQD7 to SubQD0:

These bits set the Ubit inside the DOUT generation circuit in the DAC block. Note that these bits have no effect on the DOUT generation circuit in the CD DSP block.

| SubQA3 | SubQA2 | SubQA1 | SubAD0 | SubQD7 | SubQD6 | SubQD5 | SubQD4 | SubQD3 | SubQD2 | SubQD1 | SubQD0 | Setting contents |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| 0 | 0 | 0 | 0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 | Control, address |
| 0 | 0 | 0 | 1 | Q9 | Q10 | Q11 | Q12 | Q13 | Q14 | Q15 | Q16 | Movement number |
| 0 | 0 | 1 | 0 | Q17 | Q18 | Q19 | Q20 | Q21 | Q22 | Q23 | Q24 | INDEX number |
| 0 | 0 | 1 | 1 | Q25 | Q26 | Q27 | Q28 | Q29 | Q30 | Q31 | Q32 | Elapsed time within a movement (minutes) |
| 0 | 1 | 0 | 0 | Q33 | Q34 | Q35 | Q36 | Q37 | Q38 | Q39 | Q40 | Elapsed time within a movement (seconds) |
| 0 | 1 | 0 | 1 | Q41 | Q42 | Q43 | Q44 | Q45 | Q46 | Q47 | Q48 | Elapsed time within a movement (frames) |
| 0 | 1 | 1 | 0 | Q49 | Q50 | Q51 | Q52 | Q53 | Q54 | Q55 | Q56 | (Set to "0".) |
| 0 | 1 | 1 | 1 | Q57 | Q58 | Q59 | Q60 | Q61 | Q62 | Q63 | Q64 | Absolute time (minutes) |
| 1 | 0 | 0 | 0 | Q65 | Q66 | Q67 | Q68 | Q69 | Q70 | Q71 | Q72 | Absolute time (seconds) |
| 1 | 0 | 0 | 1 | Q73 | Q74 | Q75 | Q76 | Q77 | Q78 | Q79 | Q80 | Absolute time (frames) |
| 1 | 0 | 1 | 0 | DON | DCL | DUP1 | DUP0 | DLD | 0 | 0 | 0 | (Control command) |

DON: This bit sets the Ubit output on/off inside the DOUT generation circuit in the DAC block.

When "0", Ubit is not output. (default)

When "1", Ubit is output.

DCL: This bit clears the elapsed time within a movement to "0".

The elapsed time is cleared to "0" at the falling edge of DCL (DCL = 1 → 0). (default: DCL = 1)

DUP1: This bit sets the absolute time counter operate/stop.

When "0", the absolute time counter is stopped. (default)

When "1", the absolute time counter operates.

DUP0: This bit sets the elapsed time within a movement counter operate/stop.

When "0", the elapsed time within a movement counter is stopped. (default)

When "1", the elapsed time within a movement counter operates.

DLD: This bit is used when setting the INDEX number, elapsed time within a movement, and absolute time.

When "0", the settings cannot be changed. (default)

When "1", the settings can be changed. Note that "0" is output for the INDEX number, elapsed time within a movement, and absolute time while DLD = 1.

The control, address and movement number settings can be changed regardless of the DLD setting.

\$A9E commands (preset: \$A9E00000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------|--------|----|----|----|--------|----|----|----|--------|------|-------|----|--------|-------|-------|-------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A9E (DRAM I/F) | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | DRWR | DRADR | 0 | DRD15 | DRD14 | DRD13 | DRD12 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|--------|-------|------|------|--------|------|------|------|--------|------|------|------|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| DRD11 | DRD10 | DRD9 | DRD8 | DRD7 | DRD6 | DRD5 | DRD4 | DRD3 | DRD2 | DRD1 | DRD0 |

DRWR: This bit sets write/read for access from the microcomputer to the DRAM.

When "0", the read from DRAM mode is set. (default)

When "1", the write to DRAM mode is set.

DRADR: This bit sets the address control method for access from the microcomputer to the DRAM.

When "0", relative address control is set. (default)

When "1", absolute address control is set.

DRD15 to DRD0: These bits set the data to be written to the DRAM for access from the microcomputer to the DRAM.

\$A9F commands (preset: \$A9F00000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------|--------|----|----|----|--------|----|----|----|------------|------------|------------|------------|------------|------------|------------|------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| A9F (DRAM I/F) | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | DADR 19 | DADR 18 | DADR 17 | DADR 16 | DADR 15 | DADR 14 | DADR 13 | DADR 12 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| DADR 11 | DADR 10 | DADR 9 | DADR 8 | DADR 7 | DADR 6 | DADR 5 | DADR 4 | DADR 3 | DADR 2 | DADR 1 | DADR 0 |

DADR19 to DADR0:

These bits set the DRAM address for access from the microcomputer to the DRAM.

\$AA commands (preset: \$AA00004)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-----------------------------|--------|----|----|----|--------|---------|---------|----|--------|----|----|----|--------|--------|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AA (Compression setting) | 1 | 0 | 1 | 0 | ADP ON | BIT SL1 | BIT SL0 | 0 | ADP WO | 0 | 0 | 0 | 0 | GR SEL | 0 | 0 |

| Data 5 | | | | Data 6 | | | |
|-----------|------------|----|----|--------|------|----|----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| ADPCM SEL | ADPCM MUTE | 0 | 0 | 0 | ORMU | 0 | 0 |

ADPON: This bit sets audio data compressed/uncompressed.
 When "0", the audio data uses uncompressed mode. (default)
 When "1", the audio mode is compressed mode.

BITSL1, BITSL0: These bits set the audio data compression mode.

| BITSL1 | BITSL0 | Compression mode |
|--------|--------|------------------|
| 0 | 0 | 4 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 8 bits |

*

∗: preset

ADPWO: The CD-DSP block LRCK and shock-proof memory controller block LRCK are resynchronized. This command should be used when the read speed is changed by \$A7 commands READ2, READS2 and READS1.
 When "0", not resynchronized. (default)
 When "1", resynchronized.
Note) • Set the \$AD command CDDSP SLEEP to 0 for resynchronization.
 • ADPWO should be returned to "0" after ADPWO is set to "1" and one or more LRCK cycle of CD-DSP block is waited.

GRSEL: This bit selects the GRSCOR signal output. Note that GRSCOR is output from the WDCK pin when \$8 command SCOR SEL = 1.
 When "0", the GRSCOR signal is output at the timing used inside the shock-proof memory controller block. (default)
 When "1", the GRSCOR signal generated by the CD DSP block is output.

ADPCM SEL: This bit selects ADPCM compensation.
 When "0", ADPCM is not compensated.
 When "1", ADPCM is compensated.

ADPCM MUTE: This bit sets mute at ADPCM compensation.
 When "0", it does not mute at ADPCM compensation.
 When "1", it mutes at ADPCM compensation.

ORMU: This bit controls the output signal from the LRMU pin.
 When "0", the "0" detection flag for Lch and Rch (AND output) is output.
 When "1", the OR output is made with the "0" detection flag for Lch and Rch (AND output) and SYSM.

\$AB commands (preset: \$AB000000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|---|--------|----|----|----|------------|----|----|----|--------|----|----|----|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AB (EFM playability enhancement setting) | 1 | 0 | 1 | 1 | ARD TEN | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Data 5 | | | | Data 6 | | | | Data 7 | | | |
|--------|----|----|----|--------|----|----|----|--------|----|----|----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

ARDTEN:

This is the EFM playability enhancement setting.

When "0", the EFM playability enhancement function is off.

When "1", the EFM playability enhancement function is on.

* Set this command in the condition when a disc is not being played back.

\$AC commands (preset: \$AC0C001)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------------------------|--------|----|----|----|--------|----|------|------|--------|------|------|------|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AC (Sync expansion specification) | 1 | 1 | 0 | 0 | AVW | 0 | SFP5 | SFP4 | SFP3 | SFP2 | SFP1 | SFP0 | 0 | 0 | 0 | 0 |

| Data 5 | | | | Data 6 | | | |
|---------|-------|-------|-----|--------|-----|-----|-----|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| REFSEL2 | SLIM1 | SLIM0 | OV4 | OV3 | OV2 | OV1 | OV0 |
| | 1 | 0 | | | | | |

AVW: This bit sets the sync protection window width automatic expansion function. When "0", the sync protection window width automatic expansion function is off. When "1", the sync protection window width automatic expansion function is on. This setting is not affected by the sync forward protection times setting SFP5 to SFP0.
 * The sync protection window width (± 6 channel clocks when WSEL = 0, ± 26 channel clocks when WSEL = 1) is widened 32 channel clocks at a time each time a sync mark is inserted during the interval from the 16th forward protection until GFS goes high. When the maximum window width is reached (when the window width exceeds 588 channel clocks), GTOP goes high.

SFP5 to SFP0: These bits set the frame sync forward protection times. The setting range is from 1 to 3F (h). For details on frame sync protection, see "\$4-2. Frame Sync Protection".
 * Part of this command bit register is also used by \$C SFP3 to SFP0. Of \$AC SFP3 to SFP0 or \$C SFP3 to SFP0, the command bit setting made last is valid. When using an existing status, set the value with \$C SFP5 to SFP0. When using the \$AC commands, set \$AC SFP3 to SFP0 to the value set by \$C SFP3 to SFP0.

REFSEL2: This bit sets the refresh rate to DRAM.
 See the description of \$A7 command REFSEL.

SLIM1, 0: This bit sets the DRAM write speed limit value.

| SLIM1 | SLIM0 | Write speed limit value |
|-------|-------|-------------------------|
| 0 | 0 | Up to 4.0× speed write |
| 0 | 1 | Up to 4.5× speed write |
| 1 | 0 | Up to 5.0× speed write |
| 1 | 1 | Up to 5.5× speed write |

*

*: preset

Note) This command is valid when \$A7X XWIH2 = 1.

OV4 to OV0: This bit sets the limit value of the speed violation number for one GRSCOR which is reflected to XWIH.

| OV4 to OV0 | Limit value of speed violation number |
|----------------|---------------------------------------|
| 00000 to 11111 | Can be set from 1 to 31 times. |

*: Preset value: 00001

Note) • The violation speed is set with the \$AC commands SLIM 1 and 0.

• This command is valid when \$A7X XWIH2 = 1.

\$AD commands (preset: \$AD040)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-----------------------|--------|----|----|----|--------|--------------|---------------|---------------|--------------|--------------|---------------|---------------|--------|---------------|----------------|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AD (Sleep setting) | 1 | 1 | 0 | 1 | ADCPS | DSP SLEEP | DSSP SLEEP | ASYM SLEEP | ESP SLEEP | LPF SLEEP | DSUB SLEEP | ASEQ SLEEP | PCOL | HCAV SLEEP | ERCNT SLEEP | 0 |

- ADCPS:** This bit sets the operating mode of the DSSP block A/D converter.
When "0", the operating mode of the DSSP block A/D converter is set to normal. (default)
When "1", the operating mode of the DSSP block A/D converter is set to power saving.
- DSP SLEEP:** This bit sets the operating mode of the DSP block.
When "0", the DSP block operates normally. (default)
When "1", the DSP block clock is stopped. This makes it possible to reduce power consumption.
- DSSP SLEEP:** This bit sets the operating mode of the DSSP block.
When "0", the DSSP block operates normally. (default)
When "1", the DSSP block clock is stopped. In addition, the A/D converter and operational amplifier in the DSSP block are set to standby mode. This makes it possible to reduce power consumption.
- ASYM SLEEP:** This bit sets the operating mode of the asymmetry correction circuit and VCO1/VCO2.
When "0", the asymmetry correction circuit and VCO1/VCO2 operate normally. (default)
When "1", the operational amplifier in the asymmetry correction circuit is set to standby mode. In addition, the multiplier PLL VCO1 and wide-band PLL VCO2 oscillation are stopped. This makes it possible to reduce power consumption.
- ESP SLEEP:** This bit sets the operating mode of the shock-proof memory controller block.
When "0", the shock-proof memory controller block operates normally. (default)
When "1", the shock-proof memory controller block clock is stopped. This makes it possible to reduce power consumption.
- LPF SLEEP:** This bit sets the operating mode of the analog low-pass filter block.
When "0", the analog low-pass filter block operates normally.
When "1", the analog low-pass filter block is set to standby mode. (default) This makes it possible to reduce power consumption.
- DSUB SLEEP:** This bit sets the operating mode of the Ubit generation block inside the DOUT generation circuit in the DAC block. This setting has no effect on the DOUT generation circuit in the CD DSP block.
When "0", the Ubit generation block operates normally. (default)
When "1", The clock for the Ubit generation block inside the DOUT generation circuit in the DAC block is stopped. This makes it possible to reduce power consumption. Also, in this case Ubit is set to "0".
- ASEQ SLEEP:** This bit sets the operation mode of the servo auto sequencer block.
When "0", the servo auto sequencer operates normally. (default)
When "1", the servo auto sequencer block clock is stopped. This makes the power consumption to be reduced.
- PCOL:** The PCOL pin in DSP sleep mode is fixed to low.
When "0", the PCO pin gradually becomes low by the external filter time constant. (default)
When "1", the PCO pin digitally becomes low.
Note) Set DSP SLEEP to "1" so that DSP sleep mode is entered.
- HCAV SLEEP:** This bit sets the hard CAV block operation mode.
When "0", the hard CAV block operates normally. (default)
When "1", the hard CAV block clock is stopped. This makes the power consumption to be reduced.
- ERCNT SLEEP:** This bit sets operation mode for the error rate counter block.
When "0", normally operates. (default)
When "1", the clock in the error rate counter block stops. This reduces the power consumption.

* The DAC block clock can be stopped by setting \$A5 command PWDN (when Data 2 D3 = 0, D2 = 1).

\$AE commands (preset: \$AE0)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------------------|--------|----|----|----|---------|----------|----------|------------|-----------|-----------|-----------|-----------|--------|----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AE (Variable pitch setting) | 1 | 1 | 1 | 0 | VARI ON | VARI USE | WTC C2PO | SCSY (sub) | SENS SEL3 | SENS SEL2 | SENS SEL1 | SENS SEL0 | | | | |

| Command bit | Processing |
|-------------|--|
| VARION = 0 | Variable pitch mode is off. (The internal clock uses the crystal reference.) |
| VARION = 1 | Variable pitch mode is on. (The internal clock uses the VCO2 reference.) |



| Command bit | Processing |
|-------------|---|
| VARIUSE = 0 | Set VARIUSE = 0 when not using variable pitch mode. |
| VARIUSE = 1 | Set VARIUSE = 1 when using variable pitch mode. |

* See "\$DX commands" for the variable pitch range and example of use.

WTC C2PO: This bit selects the write prohibit factor to DRAM.
 When "0", write prohibition is not allowed by the C2PO error number or external input.
 When "1", write prohibition is allowed by the C2PO error number or external input.
 Use this command only when \$8 CDROM = 0.
 • Use this command in conjunction with the \$AX command A11 SEL and \$A4 commands max C2PO7 to max C2PO0.

SCSY (sub): This bit sets the GRSCOR resynchronization period.
 See the \$8X command SCSY. (Set the \$8X command to "0" when using this bit.)

SENS SEL3 to SENS SEL0:

| SENS SEL3 | SENS SEL2 | SENS SEL1 | SENS SEL0 | SOC2 | SDTO OUT | TEXT OUT | SOCT 1 | SOCT 0 | XSOE 0 | XSOE 02 | SENS switching |
|-----------|-----------|-----------|-----------|------|----------|----------|--------|--------|---|---|--------------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | SENS serial data |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Subcode Q |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | Various signals |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Error rate |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | CD-TEXT |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  | 1 | Shock-proof memory controller status |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  | Special area read |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Special area status |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | VF0 to VF9 |

\$AF commands (preset: \$AF8000)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|-------------------------------|--------|----|----|----|--------|--------|--------|--------|------------|------------|-------|----|---------|--------|----|----------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AF (Spindle servo setting) | 1 | 1 | 1 | 1 | SYG3EA | SYG2EA | SYG1EA | SYG0EA | MDP OUTSL1 | MDP OUTSLO | LPWR2 | 0 | MDS CTL | MDP UP | 0 | MDP CTL4 |

| Data 5 | | | |
|----------|----------|----------|----------|
| D3 | D2 | D1 | D0 |
| MDP CTL3 | MDP CTL2 | MDP CTL1 | MDP CTL0 |

SYG3EA to SYG0EA:

These bits set the spindle drive output gain. However, this is valid only in CLV-N mode.

| SYG3EA | SYG2EA | SYG1EA | SYG0EA | GAIN |
|--------|--------|--------|--------|-------------------|
| 0 | 0 | 0 | 0 | 0 ($-\infty$ dB) |
| 0 | 0 | 0 | 1 | 0.125 (−18.1dB) |
| 0 | 0 | 1 | 0 | 0.250 (−12.0dB) |
| 0 | 0 | 1 | 1 | 0.375 (−8.5dB) |
| 0 | 1 | 0 | 0 | 0.500 (−6.0dB) |
| 0 | 1 | 0 | 1 | 0.625 (−4.1dB) |
| 0 | 1 | 1 | 0 | 0.750 (−2.5dB) |
| 0 | 1 | 1 | 1 | 0.875 (−1.2dB) |
| * | 1 | 0 | 0 | 1.000 (0.0dB) |
| | 1 | 0 | 1 | 1.125 (+1.0dB) |
| | 1 | 0 | 1 | 1.250 (+1.9dB) |
| | 1 | 0 | 1 | 1.375 (+2.8dB) |
| | 1 | 1 | 0 | 1.500 (+3.5dB) |
| | 1 | 1 | 0 | 1.625 (+4.2dB) |
| | 1 | 1 | 1 | 1.750 (+4.9dB) |
| | 1 | 1 | 1 | 1.875 (+5.5dB) |

*: preset

MDP OUTSL1, MDP OUTSLO:

These bits set the spindle drive output method.

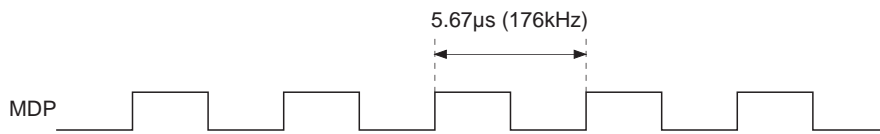
| MDP OUTSL1 | MDP OUTSLO | Spindle drive output | |
|------------|------------|----------------------|--|
| * | 0 | 0 | Ternary output from the MDP pin |
| | 1 | 0 | Binary output from the MDS and MDP pins |
| | 0 | 1 | Command-based MDP and MDS output control |

*: preset

- LPWR2: The low output (brake pulse) of the MDP pin can be masked.
When "0", binary output is high or low output, and ternary output is high, low or high impedance output. (default)
When "1", high or high impedance is output. This makes it possible to mask the brake pulse.
- MDS CTL: This bit sets the PWM output polarity according to the setting from the microcomputer. (valid when MDP OUTSL1 = 0 and MDP OUTSL0 = 1)
When "0", the MDS pin output is set low.
When "1", the MDS pin output is set high.
- MDP UP: This bit switches the MDP pin according to the setting from the microcomputer. (valid when MDP OUTSL1 = 0 and MDP OUTSL0 = 1)
When "0", the MDP pin output is set to PWM output.
When "1", the MDP pin output is set high.
- MDP CTL4 to MDP CTL0: These bits set the PWM output value according to the setting from the microcomputer. (valid when MDP OUTSL1 = 0 and MDP OUTSL0 = 1)
The carrier frequency is 176.4kHz. (88.2kHz when set to quasi-double speed)
At the minimum value (MDP CTL4 to MDP CTL0 = 0), the MDP pin output is set low.
At the maximum value (MDP CTL4 to MDP CTL0 = 1F (h)), the MDP pin output is set high for 31/32 intervals.
Note that when \$AF command MDP UP = 1, the MDP pin output is set high regardless of the MDP CTL4 to MDP CTL0 setting value.

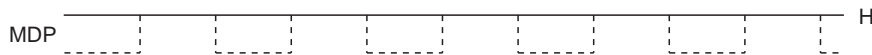
Command-based MDP and MDS output control (MDP OUTSL1 = 0, MDP OUTSL0 = 1)

(1) Timing Chart 1 LPWR2 = 0, MDP UP = 0, MDP CTL4 to MDP CTL0 = 10 (h)



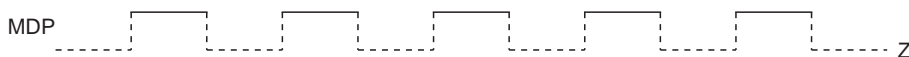
The MDP waveform ratio is set by MDP CTL4 to MDP CTL0.
When MDP CTL4 to MDP CTL0 = 10 (h), 10 (h)/20 (h) intervals are high.

(2) Timing Chart 2 LPWR2 = 0, MDP UP = 1, MDP CTL4 to MDP CTL0 = 10 (h)



When MDP UP = 1, MDP is fixed high regardless of MDP CTL4 to MDP CTL0.

(3) Timing Chart 3 LPWR2 = 1, MDP UP = 0, MDP CTL4 to MDP CTL0 = 10 (h)



When LPWR2 = 1, the low output of MDP binary output becomes high impedance.

\$BX commands

This command sets the traverse monitor count.

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Traverse monitor count setting | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set to monitor the traverse status using the SENS outputs COMP and COUT.

The monitor output is set as follows.

| Command | Data 5 | | | | Data 6 | | | |
|--------------------------------|--------|----|-------|-------|--------|-----|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Traverse monitor count setting | 0 | 0 | MTSL1 | MTSL0 | ASYE | MD2 | 0 | 0 |

| Command bit | | Output data | | | |
|-------------|-------|-------------|------|------|------|
| MTSL1 | MTSL0 | | | | |
| 0 | 0 | XUGF | XPCK | GFS | C2PO |
| 0 | 1 | MINT0 | MNT1 | MNT2 | MNT3 |
| 1 | 0 | RFCK | XPCK | XROF | GTOP |
| 1 | 1 | C4M | FSTO | GFS | C2PO |

*: preset

* However, the \$39 command SRO1 and \$A7 command MON SEL must be set to "0".

| Command bit | Processing |
|-------------|-------------------|
| ASYE = 1 | Asymmetry is on. |
| ASYE = 0 | Asymmetry is off. |

*: preset

| Command bit | Processing |
|-------------|---|
| MD2 = 0 | Digital Out on/off control. Off when "0". |
| MD2 = 1 | Digital Out on/off control. On when "1". |

*: preset

\$CX commands

| Command | Data 1 | | | | Data 2 | | | |
|-----------------------------------|-----------|-----------|-----------|-----------|------------|------------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Spindle servo coefficient setting | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 | Gain DCLV1 | Gain DCLV0 | PCC1 | PCC0 |
| CLV CTRL (\$DX) | | | | Gain CLVS | | | | |

- CLVS mode gain setting: GCLVS

| Gain MDS1 | Gain MDS0 | Gain CLVS | GCLVS |
|-----------|-----------|-----------|-------|
| 0 | 0 | 0 | -12dB |
| 0 | 0 | 1 | -6dB |
| 0 | 1 | 0 | -6dB |
| 0 | 1 | 1 | 0dB |
| 1 | 0 | 0 | 0dB |
| 1 | 0 | 1 | +6dB |

- CLVP mode gain setting: GMDP: GMDS

| Gain MDP1 | Gain MDP0 | GMDP | Gain MDS1 | Gain MDS0 | GMDS |
|-----------|-----------|------|-----------|-----------|------|
| 0 | 0 | -6dB | 0 | 0 | -6dB |
| 0 | 1 | 0dB | 0 | 1 | 0dB |
| 1 | 0 | +6dB | 1 | 0 | +6dB |

- DCLV overall gain setting: GDCLV

| Gain DCLV1 | Gain DCLV0 | GDCLV |
|------------|------------|-------|
| 0 | 0 | 0dB |
| 0 | 1 | +6dB |
| 1 | 0 | +12dB |

| Command bit | | Processing |
|-------------|------|--|
| PCC1 | PCC0 | |
| 0 | 0 | The VPCO signal is output. |
| 0 | 1 | The VPCO pin output is high impedance. |
| 1 | 0 | The VPCO pin output is low. |
| 1 | 1 | The VPCO pin output is high. |

- This command controls the VPCO pin signal.

The VPCO output can be controlled with this setting.

| Command | Data 3 | | | | Data 4 | | | |
|-----------------------------------|--------|------|------|------|--------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Spindle servo coefficient setting | SFP3 | SFP2 | SFP1 | SFP0 | SRP3 | SRP2 | SRP1 | SRP0 |

| Command bit | Processing |
|--------------|---|
| SFP3 to SFP0 | Sets the number of frame sync forward protection times. The setting range is from 1 to F (h). |

| Command bit | Processing |
|--------------|--|
| SRP3 to SRP0 | Sets the number of frame sync backward protection times. The setting range is from 1 to F (h). |

* See "§4-2. Frame Sync Protection" regarding frame sync protection.

- The CXD3048R can serially output the 40 bits (10 BCD codes) of error rate data selected by EDC7 to EDC0 from the SQSO pin and monitor this data using a microcomputer.
In order to output error rate data, set \$C commands for C1 and C2 individually, and set \$8 commands SOCT0 and SOCT1 to "1". Then, the data can be read out from the SQSO pin by sending 40 SQCK pulses.

| Command | Data 5 | | | | Data 6 | | | |
|-----------------------------------|--------|------|------|------|--------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Spindle servo coefficient setting | EDC7 | EDC6 | EDC5 | EDC4 | EDC3 | EDC2 | EDC1 | EDC0 |

Preset value: 00h

Error rate monitor commands

| Command bit | Prpcessing |
|---------------|---|
| EDC7 = 0 EDC6 | The [No C1 errors, pointer reset] count is output When "1". |
| EDC5 | The [One C1 error corrected, pointer reset] count is output When "1". |
| EDC4 | The [No C1 errors, pointer set] count is output When "1". |
| EDC3 | The [One C1 error corrected, pointer set] count is output When "1". |
| EDC2 | The [Two C1 errors corrected, pointer set] count is output When "1". |
| EDC1 | The [C1 correction impossible, pointer set] count is output When "1". |
| EDC0 | 7350-frame count cycle mode*1 When "0". 73500-frame count cycle mode*2 When "1". |
| EDC7 = 1 EDC6 | The [No C2 errors, pointer reset] count is output When "1". |
| EDC5 | The [One C2 error corrected, pointer reset] count is output When "1". |
| EDC4 | The [Two C2 errors corrected, pointer reset] count is output When "1". |
| EDC3 | The [Three C2 errors corrected, pointer reset] count is output When "1". |
| EDC2 | The [Four C2 errors corrected, pointer reset] count is output When "1". |
| EDC1 | The [C2 correction impossible, pointer copy] count is output When "1". |
| EDC0 | The [C2 correction impossible, pointer set] count is output When "1". |

*1 The values selected by C1 (EDC1 to EDC6) and C2 (EDC0 to EDC6) are added to C1 and C2, respectively, and output every 7350 frames.

*2 The values selected by C1 (EDC1 to EDC6) and C2 (EDC0 to EDC6) are added to C1 and C2, respectively, and output every 73500 frames.

\$DX commands

| Command | Data 1 | | | |
|----------|--------|----|----|--------------|
| | D3 | D2 | D1 | D0 |
| CLV CTRL | 0 | TB | TP | Gain CLVS |

See "\$CX commands".

| Command bit | Description |
|-------------|---|
| TB = 0 | Bottom hold at a cycle of RFCK/32 in CLVS mode. |
| TB = 1 | Bottom hold at a cycle of RFCK/16 in CLVS mode. |
| TP = 0 | Peak hold at a cycle of RFCK/4 in CLVS mode. |
| TP = 1 | Peak hold at a cycle of RFCK/2 in CLVS mode. |

| Command | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|----------|--------|-----|-----|-----|--------|-----|-----|-----|------------|------------|----|----|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| CLV CTRL | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | VP CTL1 | VP CTL0 | 0 | 0 |

The settings in CAV-W mode are as follows.

| Command bit | Processing |
|-------------|---------------------------------------|
| VP0 to VP7 | Sets the spindle rotational velocity. |

| Command bit | | Processing |
|-------------|--------|---|
| VPCTL1 | VPCTL0 | |
| 0 | 0 | The setting of VP0 to VP7 is multiplied by 1. |
| 0 | 1 | The setting of VP0 to VP7 is multiplied by 2. |
| 1 | 0 | The setting of VP0 to VP7 is multiplied by 3. |
| 1 | 1 | The setting of VP0 to VP7 is multiplied by 4. |

* The above setting should be "0", "0" except for the CAV-W operating mode.

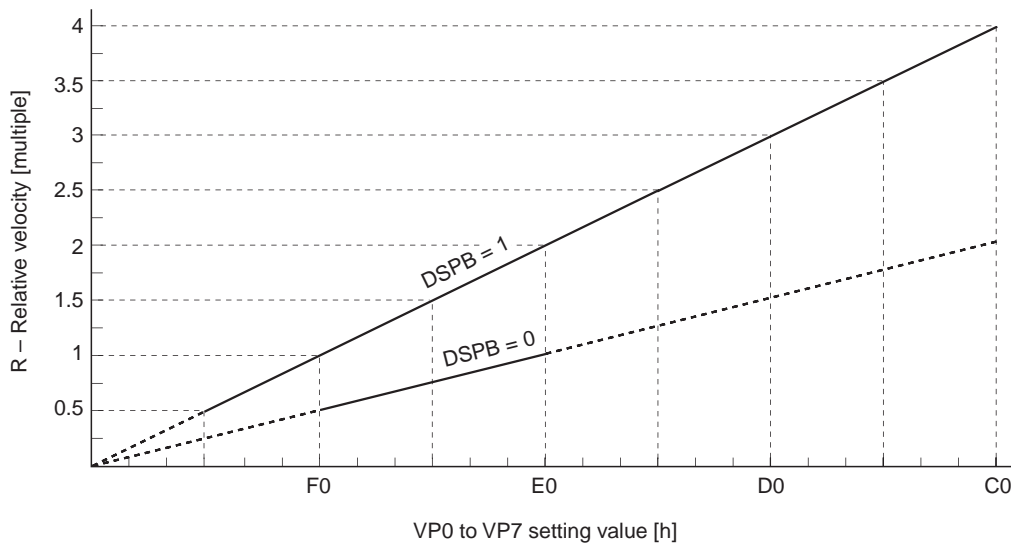
The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32} \times I$$

R: Relative velocity at normal speed = 1
 n: VP0 to VP7 setting value
 I: Multiple set by VPCTL0, VPCTL1

| Command bit | Description |
|---------------------|---|
| VP0 to VP7 = F0 (h) | Playback at half (normal) speed to |
| : | |
| VP0 to VP7 = E0 (h) | Playback at normal (double) speed to |
| : | |
| VP0 to VP7 = C0 (h) | Playback at (quadruple) speed |

- Notes)** 1. Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.
 2. Values in parentheses are for when DSPB is "1".



The settings in variable pitch mode are as follows.

| Command bit | Processing |
|------------------------------|---|
| VPCTL1 to VPCTL0, VP7 to VP0 | Sets the pitch for variable pitch mode. |

The pitch setting can be expressed with the following equation.

$$P = \frac{-n}{10} [\%]$$

P: Pitch setting value
 n: VPCTL1 and VPCTL0, VP7 to VP0 setting value (two's complement, VPCTL1 = sign bit)

| Command bit | | | Pitch setting value [%] | Command setting example |
|-------------|--------|------------|-------------------------|-------------------------|
| VPCTL1 | VPCTL0 | VP7 to VP0 | | |
| 1 | 0 | 00 (H) | +51.2 | \$D60080 |
| | | — | to | : |
| | | FF (H) | +25.7 | \$D6FF80 |
| 1 | 1 | 00 (H) | +25.6 | \$D600C0 |
| | | — | to | : |
| | | FF (H) | +0.1 | \$D6FFC0 |
| 0 | 0 | 00 (H) | 0.0 | \$D60000 |
| | | — | to | : |
| | | FF (H) | -25.5 | \$D6FF00 |
| 0 | 1 | 00 (H) | -25.6 | \$D60040 |
| | | — | to | : |
| | | E7 (H) | -48.7 | \$D6E740 |

The pitch setting range is from -48.7 to +51.2%.

The plus pitch setting should not exceed the playback speed given in the Recommended Operating Conditions.

An example of variable pitch mode commands is shown below.

- \$EX001 (Sets INV VPCO = 1.)
- \$AE4 (Setting to enable variable pitch mode.)
- \$AEC (Turns on variable pitch mode. The internal clock uses the VCO2 reference.)
- \$D60A00 (Sets the pitch to -1.0%.)
- \$D60000 (Sets the pitch to 0.0%.)
- \$AE4 (Turns off variable pitch mode. The internal clock uses the crystal reference.)

\$EX commands

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|----------|--------|-----|-----|-----|--------|------|------|------|--------|------|------|------|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| SPD mode | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON |

| Command bit | | | | Mode | Description |
|-------------|-----|-----|-----|-------|---|
| CM3 | CM2 | CM1 | CM0 | | |
| 0 | 0 | 0 | 0 | STOP | Spindle stop mode.*1 |
| 1 | 0 | 0 | 0 | KICK | Spindle forward rotation mode.*1 |
| 1 | 0 | 1 | 0 | BRAKE | Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.*1 |
| 1 | 1 | 1 | 0 | CLVS | Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range. |
| 1 | 1 | 1 | 1 | CLVP | PLL servo mode. |
| 0 | 1 | 1 | 0 | CLVA | Automatic CLVS/CLVP switching mode. Used for normal playback. |

*1 See Timing Charts 1-6 to 1-29.

In the digital CLV servo, the sampling frequency of the internal digital filter is switched simultaneously with the switching of CLVP/CLVS.

Then, the CLVS mode cut-off frequency f_c is 70Hz when \$D command TB = 0 or 140Hz when \$D command TB = 1.

Spindle control can be set to the ternary output of only MDP or the binary outputs of MDP and MDS by \$AF commands MDPOUTSL1 and MDPOUTSL0.

| Command bit | | | | | | | | | Mode | Description |
|-------------|------|------|------|------|------|------|------|----------|-------|--|
| EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | INV VPCO | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLV-N | Crystal reference CLV servo. |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLV-N | VCO2 reference CLV servo. |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | CLV-W | Used for playback in CLV-W mode.*2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CAV-W | Spindle control with VP0 to VP7. |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CAV-W | Spindle control with the external PWM. |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | VCO-C | VCO control*3 |

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

*3 Fig. 3-3 shows the control flow with the microcomputer software in VCO-C mode.

| Mode | LPWR | LPWR2 | Command | Timing chart – Ternary output | Timing chart – Binary output |
|-------|------|-------|---------|-------------------------------|------------------------------|
| CLV-N | 0 | 0 | KICK | 1-6 (a) | 1-18 (a) |
| | | | BRAKE | 1-6 (b) | 1-18 (b) |
| | | | STOP | 1-6 (c) | 1-18 (c) |
| CLV-W | 0 | 0 | KICK | 1-7 (a) | 1-19 (a) |
| | | | BRAKE | 1-7 (b) | 1-19 (b) |
| | | | STOP | 1-7 (c) | 1-19 (c) |
| | 1 | 0 | KICK | 1-8 (a) | 1-20 (a) |
| | | | BRAKE | 1-8 (b) | 1-20 (b) |
| | | | STOP | 1-8 (c) | 1-20 (c) |
| CAV-W | 0 | 0 | KICK | 1-9 (a) | 1-21 (a) |
| | | | BRAKE | 1-9 (b) | 1-21 (b) |
| | | | STOP | 1-9 (c) | 1-21 (c) |
| | 1 | 0 | KICK | 1-10 (a) | 1-22 (a) |
| | | | BRAKE | 1-10 (b) | 1-22 (b) |
| | | | STOP | 1-10 (c) | 1-22 (c) |

| Mode | LPWR | LPWR2 | Timing chart – Ternary output | Timing chart – Binary output |
|-------|------|-------|-------------------------------|------------------------------|
| CLV-N | 0 | 0 | 1-11 | 1-23 |
| CLV-W | 0 | 0 | 1-12 | 1-24 |
| | 1 | | 1-13 | 1-25 |
| CAV-W | 0 | 0 | 1-14 (EPWM = 0) | 1-26 (EPWM = 0) |
| | 1 | | 1-15 (EPWM = 0) | 1-27 (EPWM = 0) |
| | 0 | | 1-16 (EPWM = 1) | 1-28 (EPWM = 1) |
| | 1 | | 1-17 (EPWM = 1) | 1-29 (EPWM = 1) |

| Mode | LPWR | LPWR2 | Command | Timing chart – Ternary output | Timing chart – Binary output |
|-------|------|-------|---------|-------------------------------|------------------------------|
| CLV-W | 0 | 1 | KICK | 1-8 (a) | 1-30 (a) |
| | | | BRAKE | 1-8 (b) | 1-30 (b) |
| | | | STOP | 1-8 (c) | 1-30 (c) |
| | 1 | 1 | KICK | 1-8 (a) | 1-31 (a) |
| | | | BRAKE | 1-8 (b) | 1-31 (b) |
| | | | STOP | 1-8 (c) | 1-31 (c) |
| CAV-W | 0 | 1 | KICK | 1-10 (a) | 1-32 (a) |
| | | | BRAKE | 1-10 (b) | 1-32 (b) |
| | | | STOP | 1-10 (c) | 1-32 (c) |
| | 1 | 1 | KICK | 1-10 (a) | 1-33 (a) |
| | | | BRAKE | 1-10 (b) | 1-33 (b) |
| | | | STOP | 1-10 (c) | 1-33 (c) |

| Mode | LPWR | LPWR2 | Timing chart – Ternary output | Timing chart – Binary output |
|-------|------|-------|-------------------------------|------------------------------|
| CLV-W | 0 | 1 | 1-13 | 1-34 |
| | 1 | | 1-13 | 1-35 |
| CAV-W | 0 | 1 | 1-15 (EPWM = 0) | 1-36 (EPWM = 0) |
| | 1 | | 1-15 (EPWM = 0) | 1-37 (EPWM = 0) |
| | 0 | | 1-17 (EPWM = 1) | 1-38 (EPWM = 1) |
| | 1 | | 1-17 (EPWM = 1) | 1-39 (EPWM = 1) |

| Command | Data 4 | | | |
|----------|-----------|-----------|----|----------|
| | D3 | D2 | D1 | D0 |
| SPD mode | Gain CAV1 | Gain CAV0 | 0 | INV VPCO |

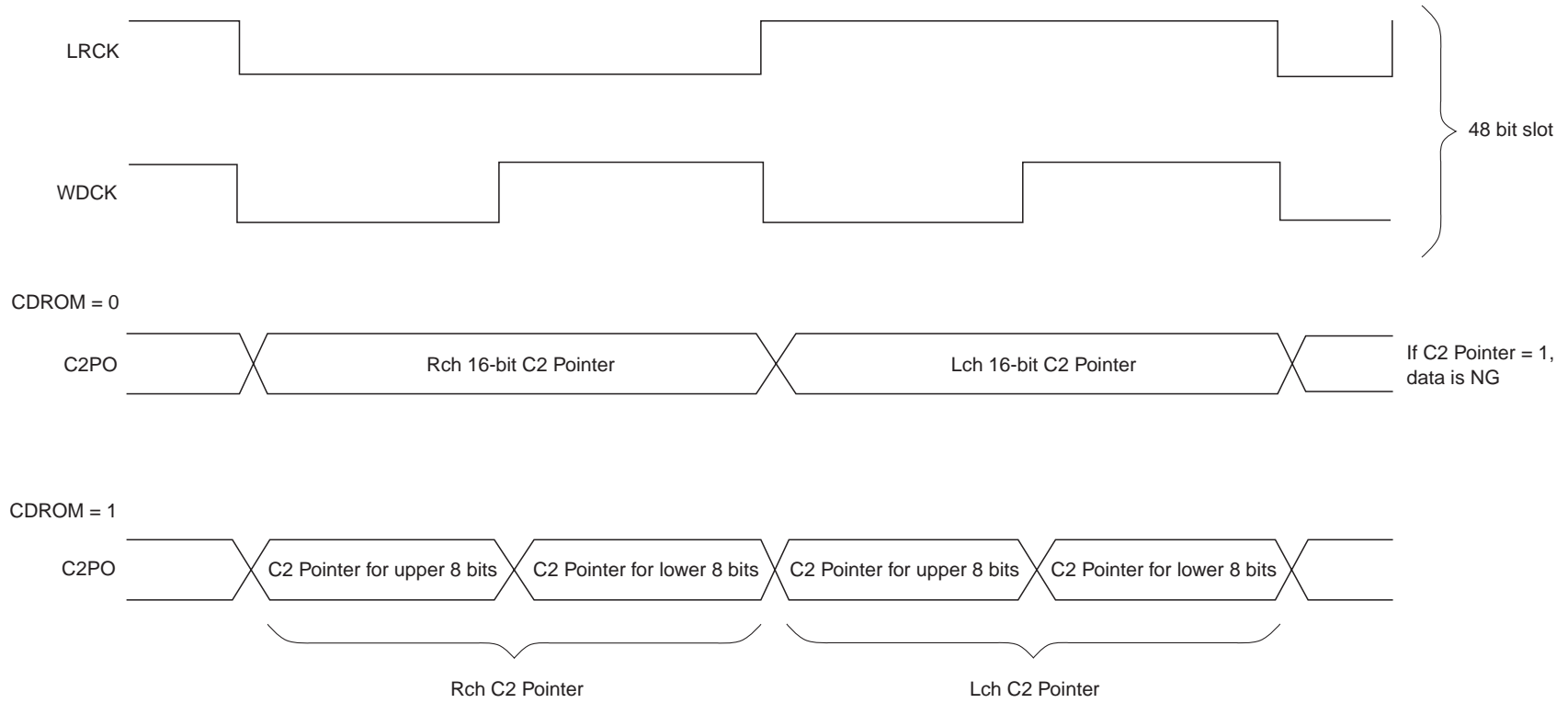
See page 86.

| Gain CAV1 | Gain CAV0 | Gain |
|-----------|-----------|-------|
| 0 | 0 | 0dB |
| 0 | 1 | -6dB |
| 1 | 0 | -12dB |
| 1 | 1 | -18dB |

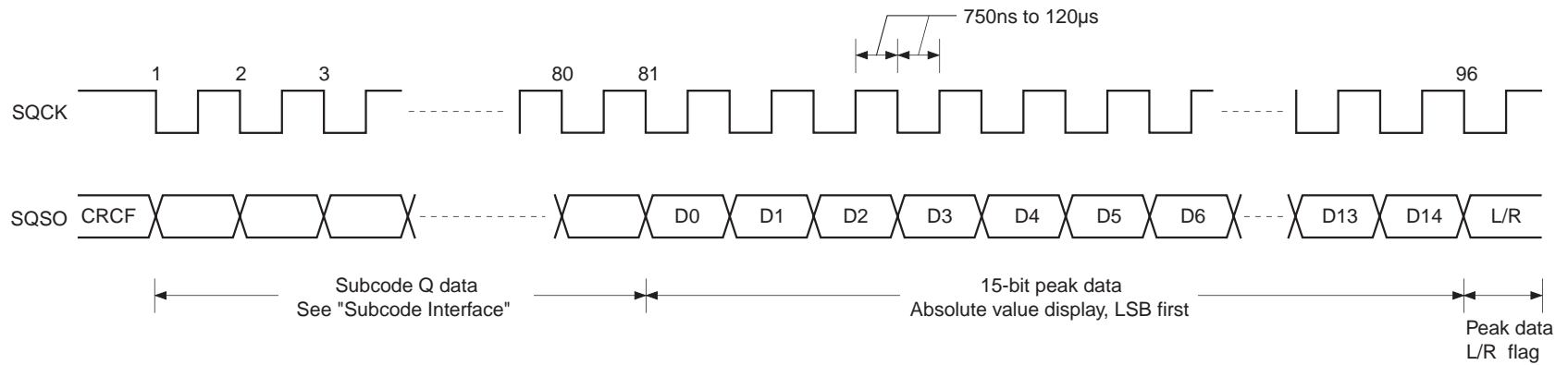
- This sets the gain when controlling the spindle with VP7 to VP0 in CAV-W mode.

Note) The Gain CAV1 and Gain CAV0 commands are invalid for spindle control with the external PWM.

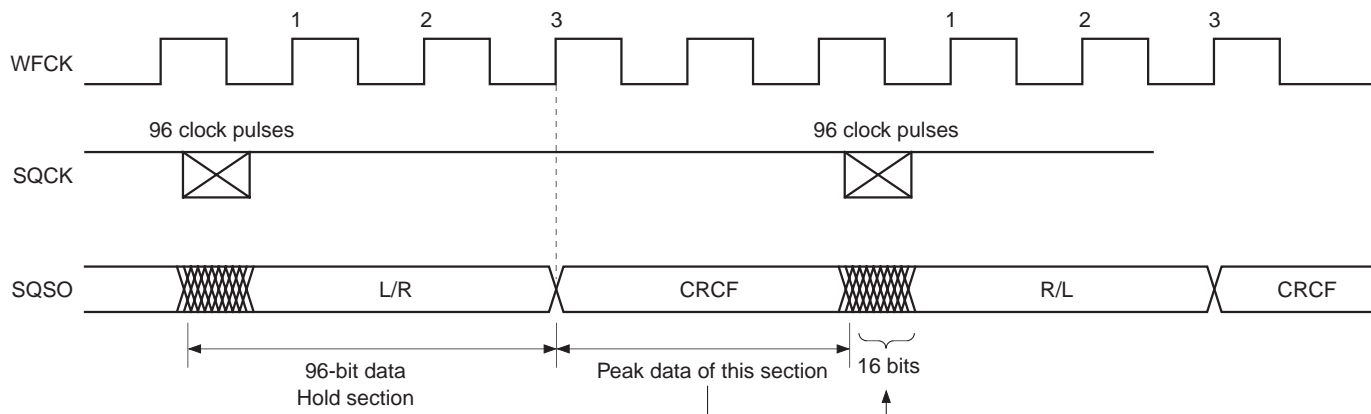
Timing Chart 1-3



Timing Chart 1-4

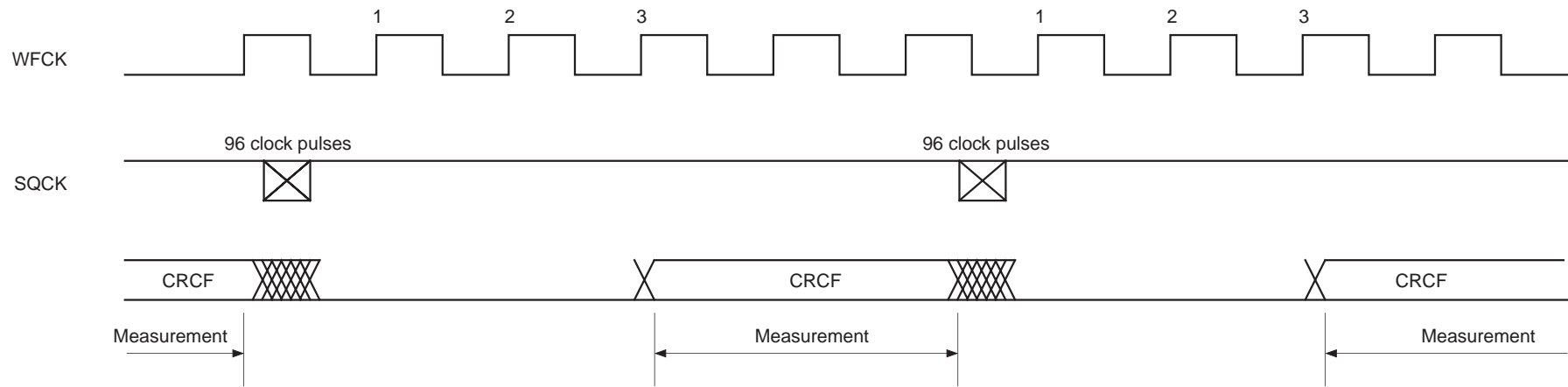


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Level Meter Timing

Timing Chart 1-5



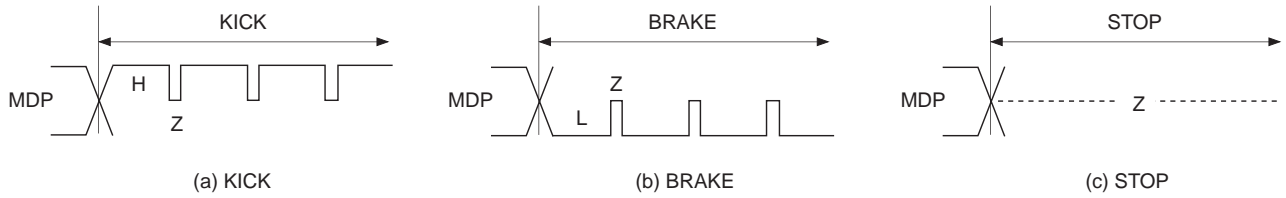
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Peak Meter Timing

Ternary output from MDP pin (\$AF MDPOUTSL1 = 0, MDPOUTSL0 = 0)

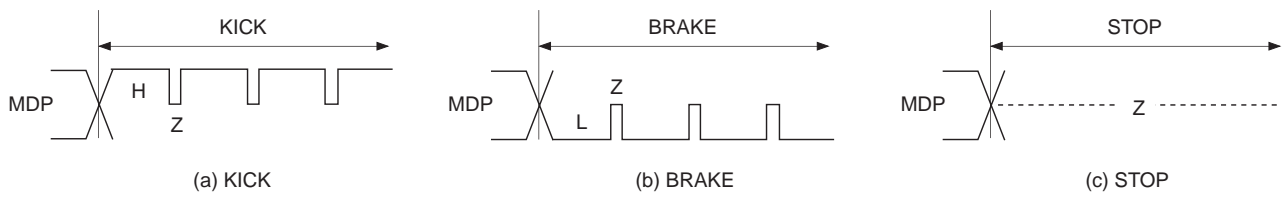
Timing Chart 1-6

CLV-N mode LPWR = 0, LPWR2 = 0



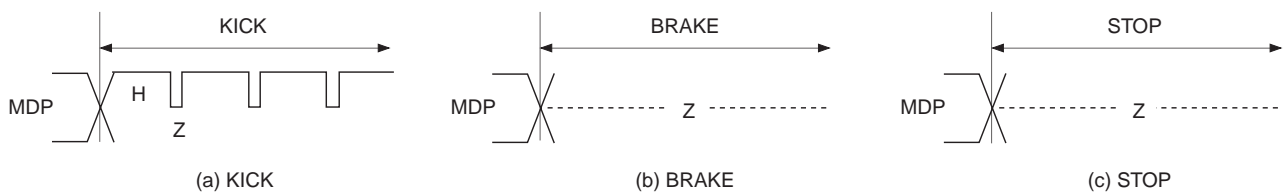
Timing Chart 1-7

CLV-W mode (when following the spindle rotational velocity) LPWR = 0, LPWR2 = 0



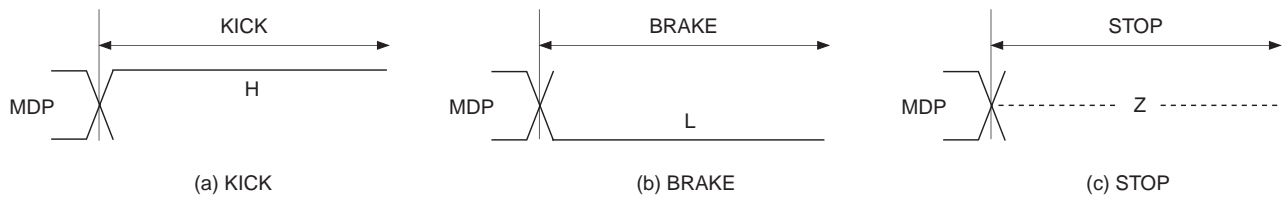
Timing Chart 1-8

CLV-W mode (when following the spindle rotational velocity) LPWR = 1, LPWR2 = 0



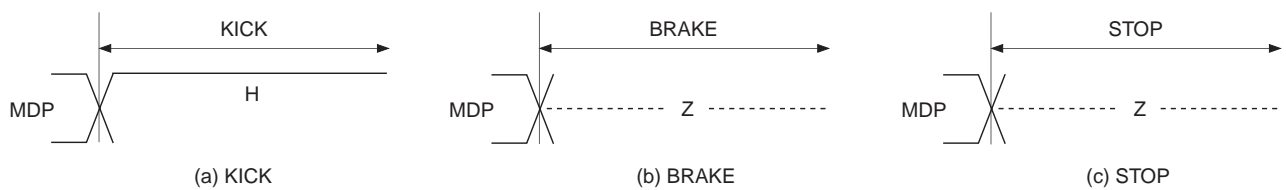
Timing Chart 1-9

CAV-W mode LPWR = 0, LPWR2 = 0



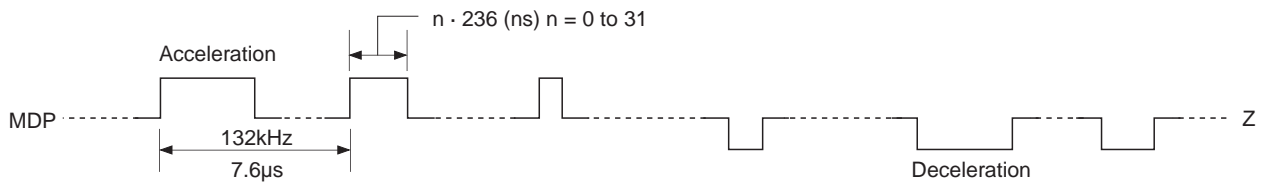
Timing Chart 1-10

CAV-W mode LPWR = 1, LPWR2 = 0



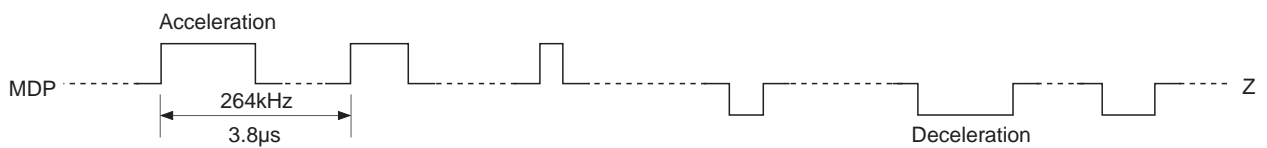
Timing Chart 1-11

CLV-N mode LPWR = 0, LPWR2 = 0



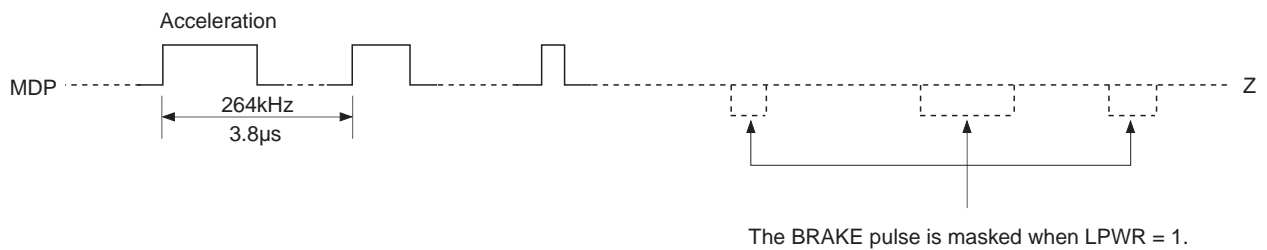
Timing Chart 1-12

CLV-W mode LPWR = 0, LPWR2 = 0



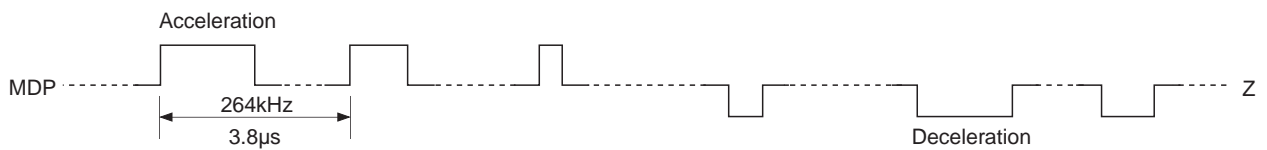
Timing Chart 1-13

CLV-W mode LPWR = 1, LPWR2 = 0



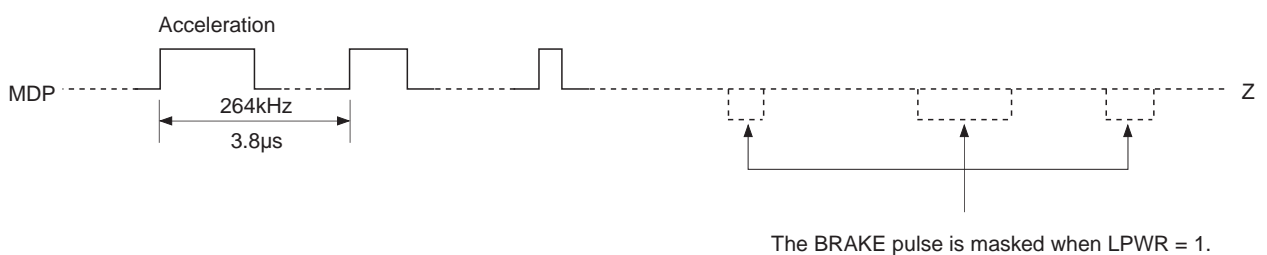
Timing Chart 1-14

CAV-W mode EPWM = LPWR = 0, LPWR2 = 0



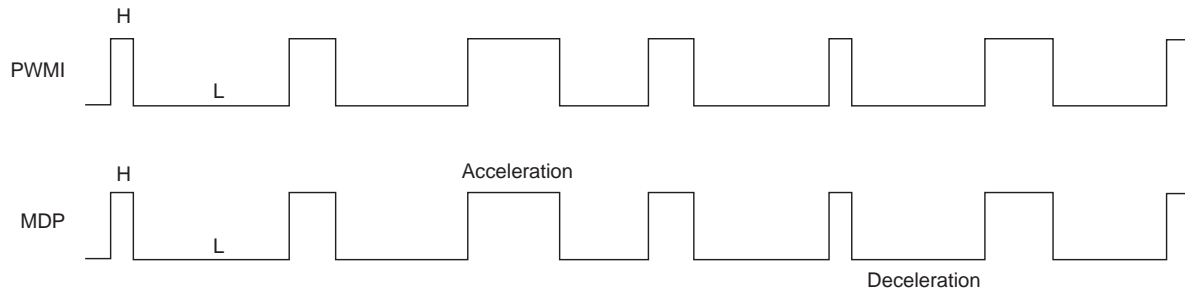
Timing Chart 1-15

CAV-W mode EPWM = 0, LPWR = 1, LPWR2 = 0



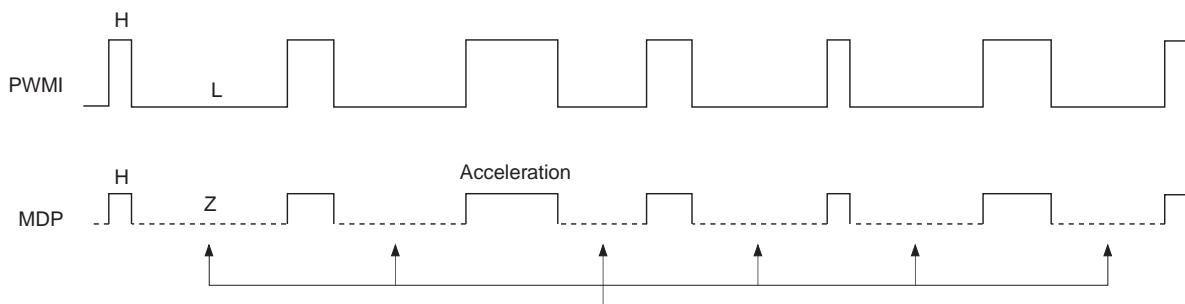
Timing Chart 1-16

CAV-W mode EPWM = 1, LPWR = 0, LPWR2 = 0



Timing Chart 1-17

CAV-W mode EPWM = LPWR = 1, LPWR2 = 0

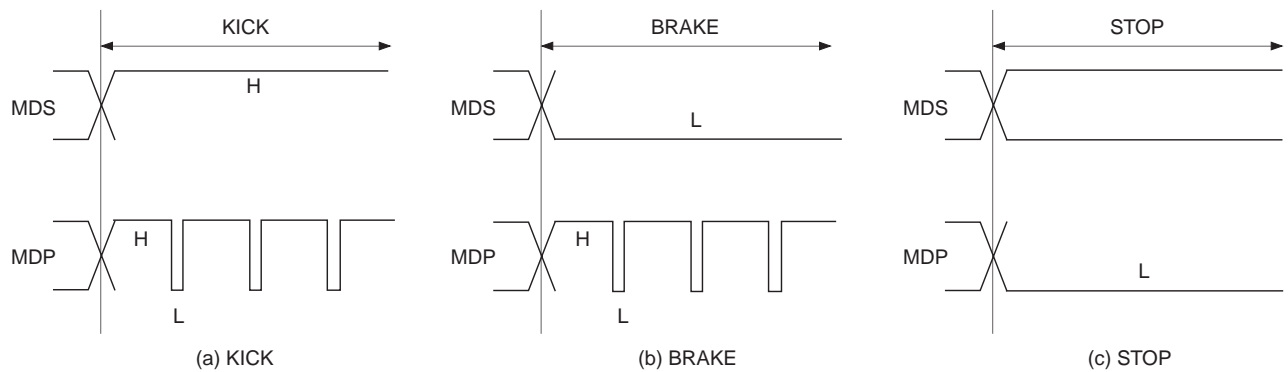


The BRAKE pulse is masked when LPWR = 1.

Binary output from MDP and MDS pins (\$AF MDPOUTSL1 = 1, MDPOUTSL0 = 0)

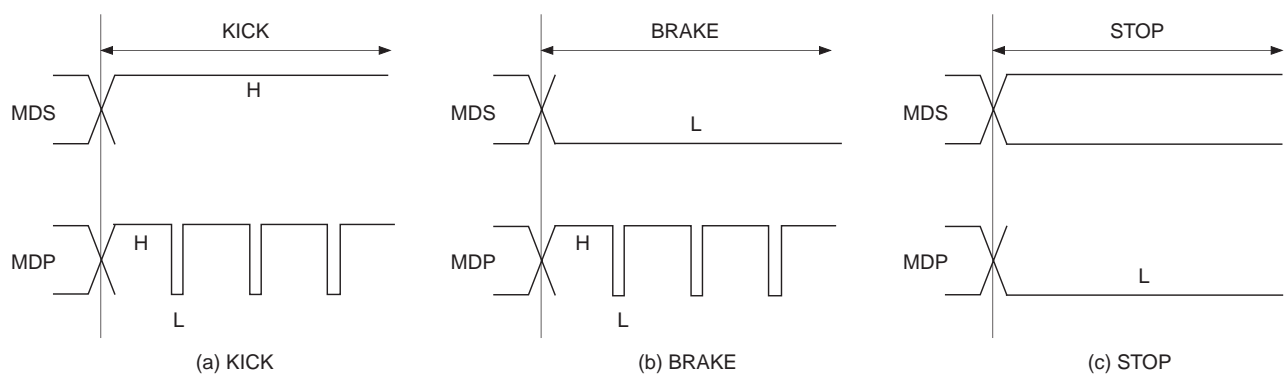
Timing Chart 1-18

CLV-N mode LPWR = 0, LPWR2 = 0



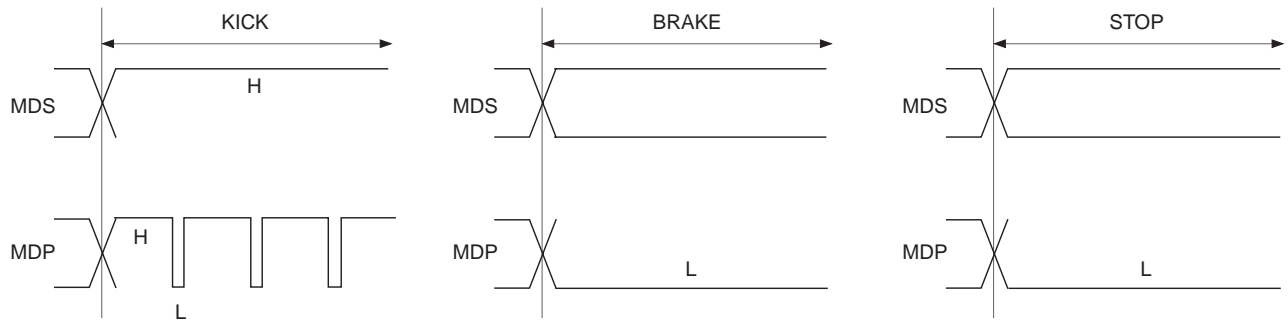
Timing Chart 1-19

CLV-W mode (when following the spindle rotational velocity) LPWR = 0, LPWR2 = 0



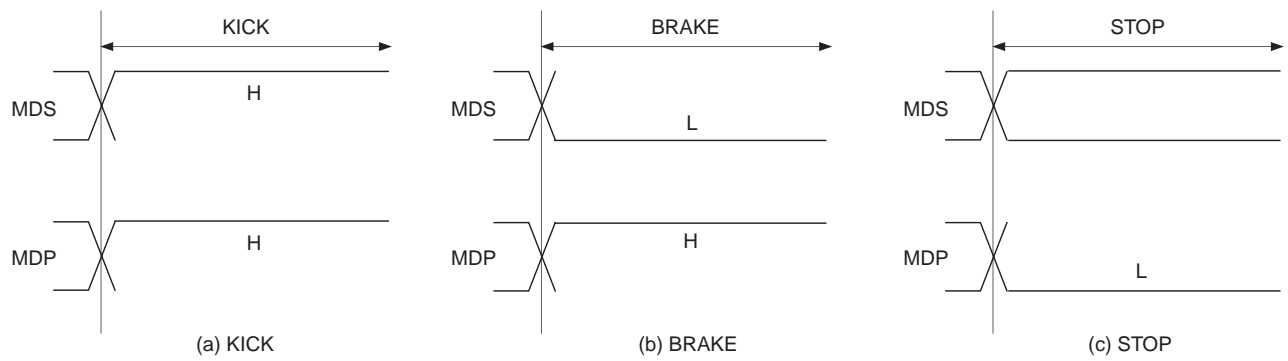
Timing Chart 1-20

CLV-W mode (when following the spindle rotational velocity) LPWR = 1, LPWR2 = 0



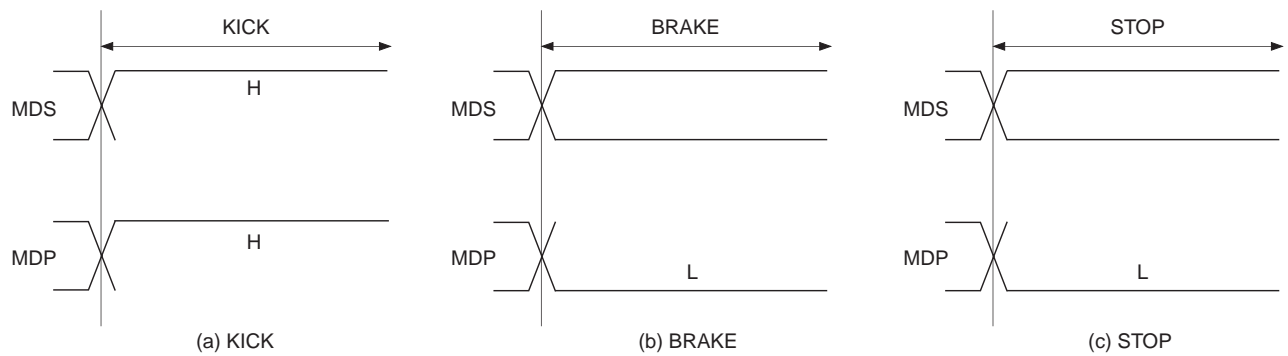
Timing Chart 1-21

CAV-W mode LPWR = 0, LPWR2 = 0



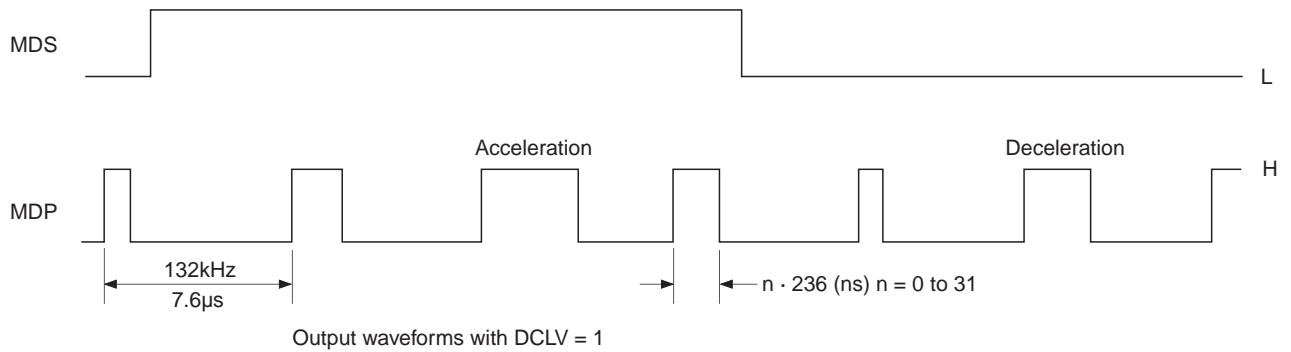
Timing Chart 1-22

CAV-W mode LPWR = 1, LPWR2 = 0



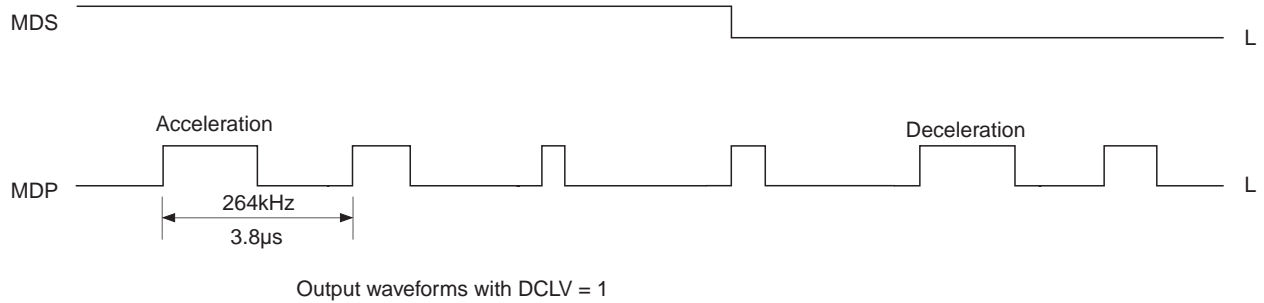
Timing Chart 1-23

CLV-N mode LPWR = 0, LPWR2 = 0



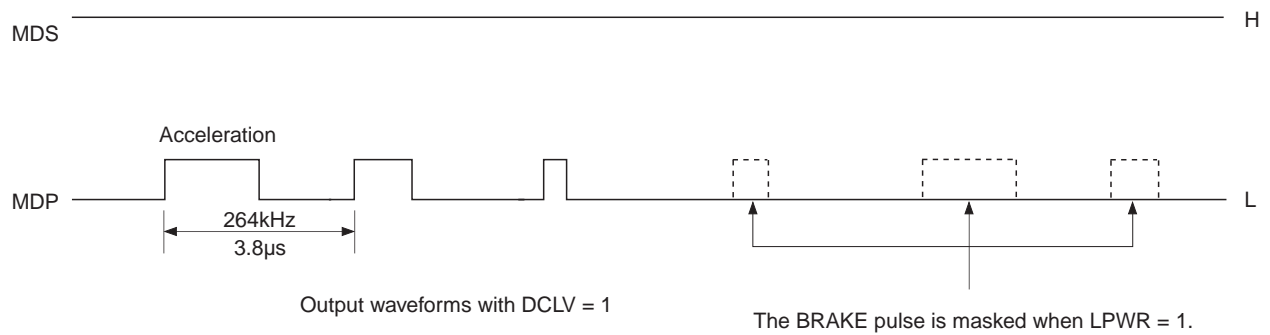
Timing Chart 1-24

CLV-W mode LPWR = 0, LPWR2 = 0



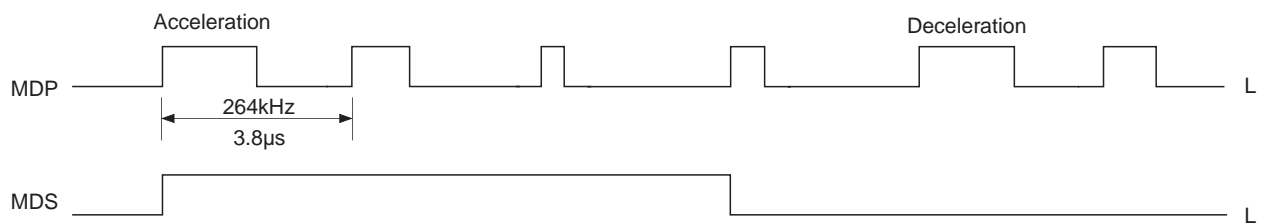
Timing Chart 1-25

CLV-W mode LPWR = 1, LPWR2 = 0



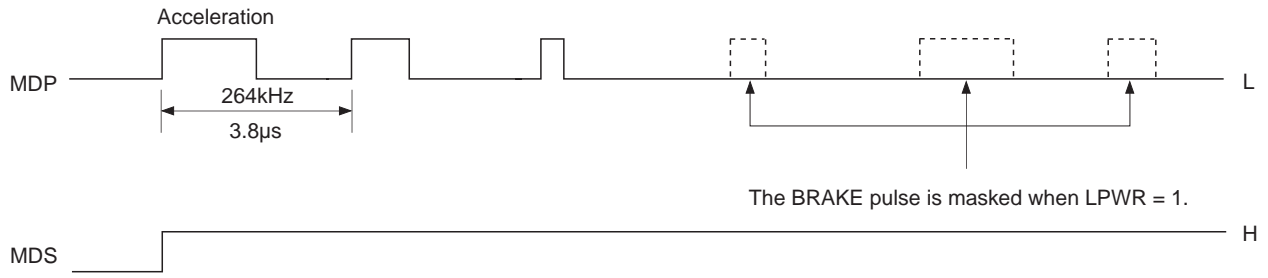
Timing Chart 1-26

CAV-W mode EPWM = 0, LPWR = 0, LPWR2 = 0



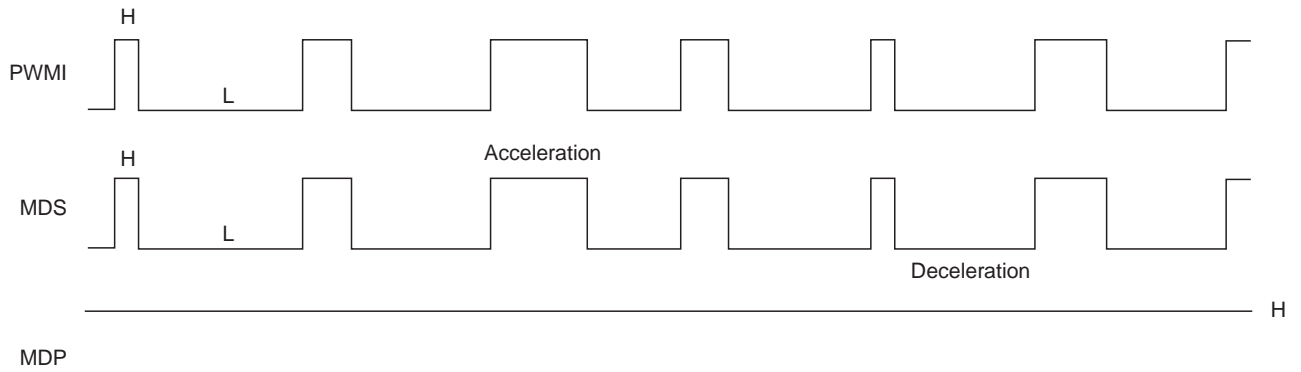
Timing Chart 1-27

CAV-W mode EPWM = 0, LPWR=1, LPWR2 = 0



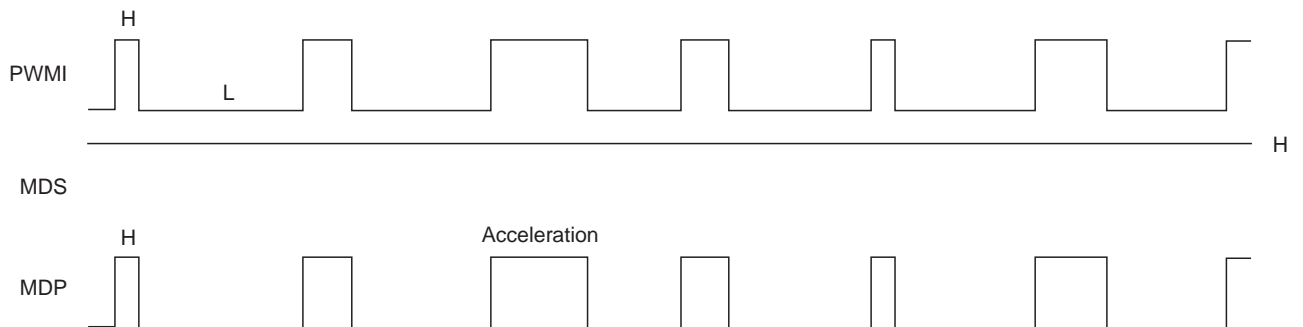
Timing Chart 1-28

CAV-W mode EPWM = 1, LPWR = 0, LPWR2 = 0



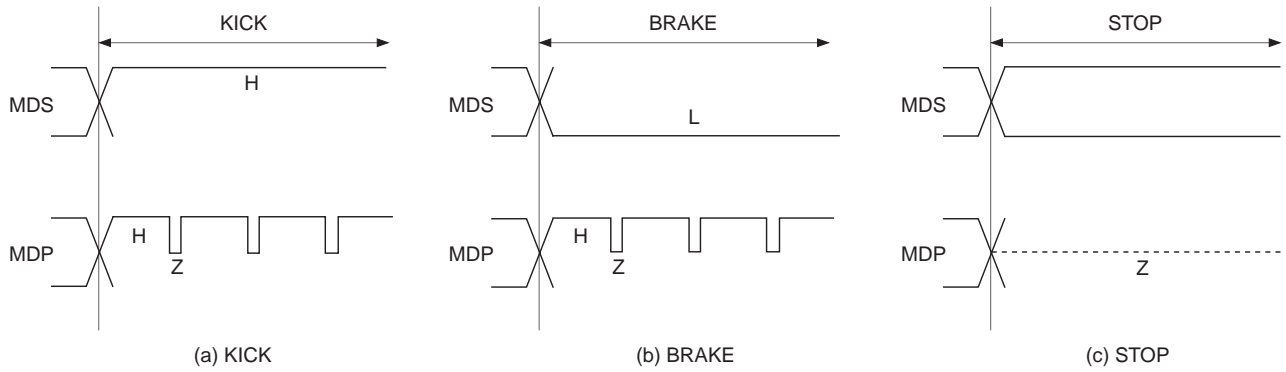
Timing Chart 1-29

CAV-W mode EPWM = 1, LPWR = 1, LPWR2 = 0



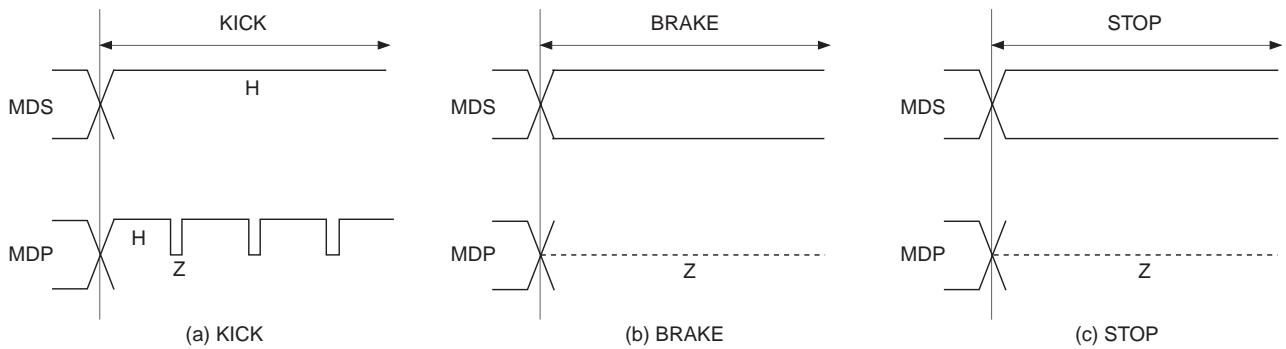
Timing Chart 1-30

CLV-W mode (when following the spindle rotational velocity) LPWR = 0, LPWR2 = 1



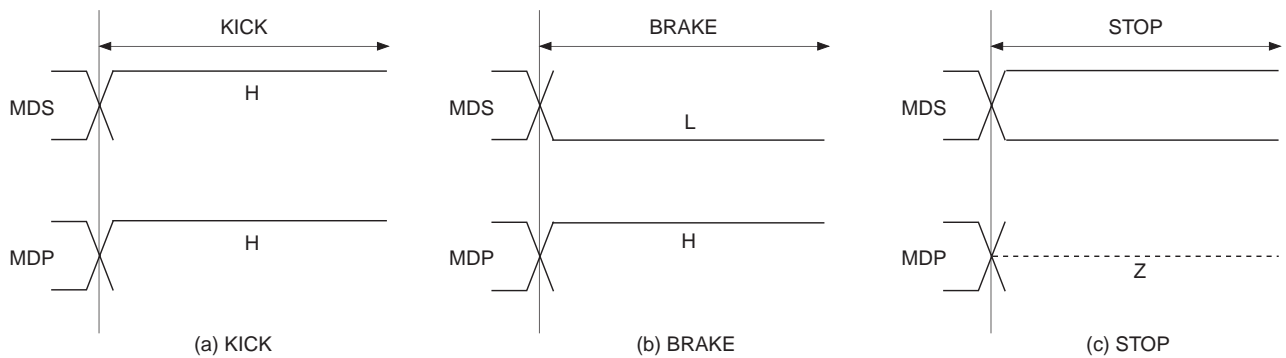
Timing Chart 1-31

CLV-W mode (when following the spindle rotational velocity) LPWR = 1, LPWR2 = 1



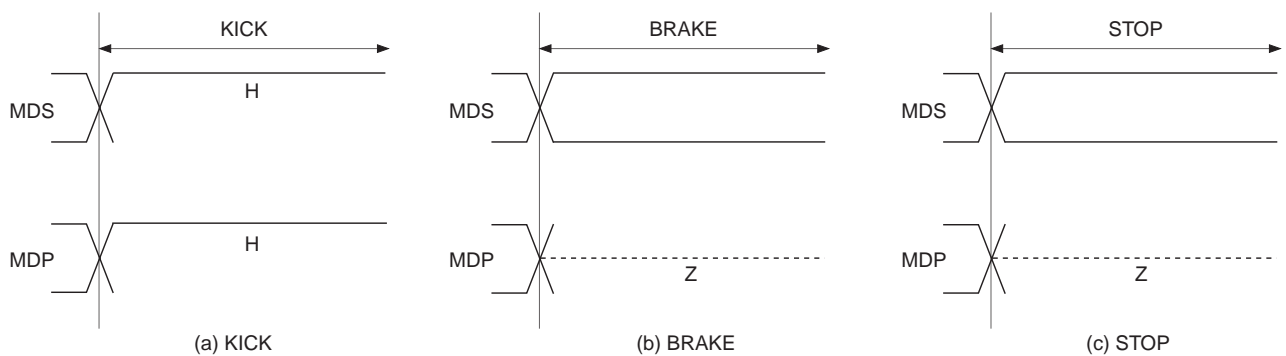
Timing Chart 1-32

CAV-W mode LPWR = 0, LPWR2 = 1



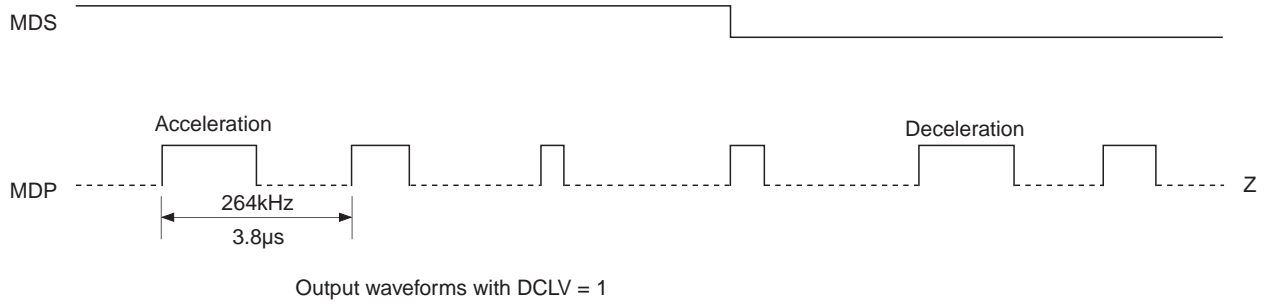
Timing Chart 1-33

CAV-W mode LPWR = 1, LPWR2 = 1



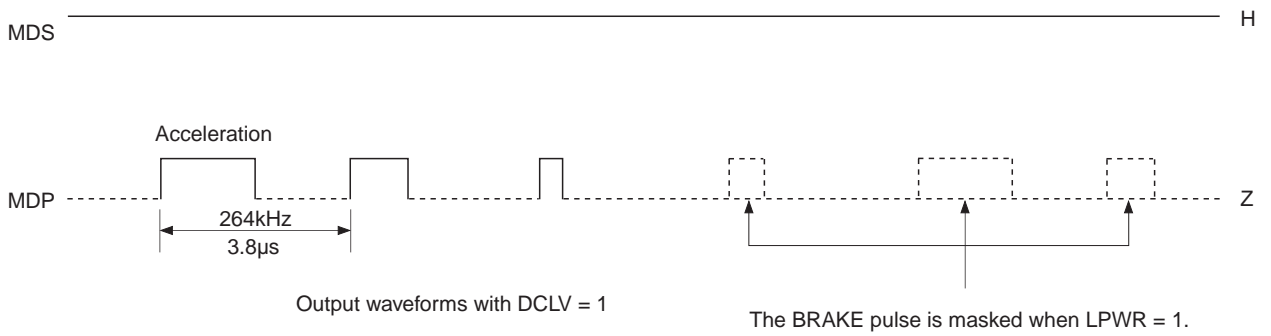
Timing Chart 1-34

CLV-W mode LPWR = 0, LPWR2 = 1



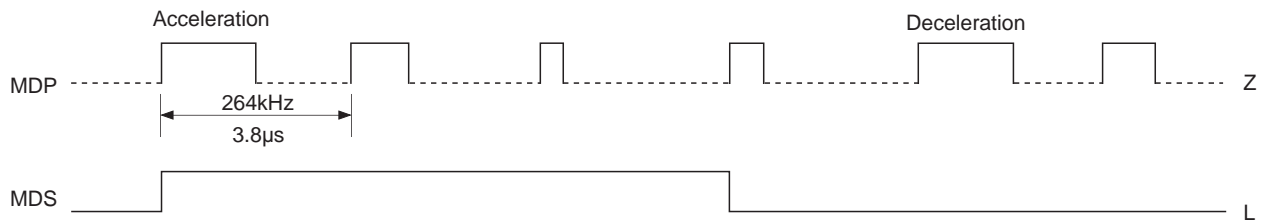
Timing Chart 1-35

CLV-W mode LPWR = 1, LPWR2 = 1



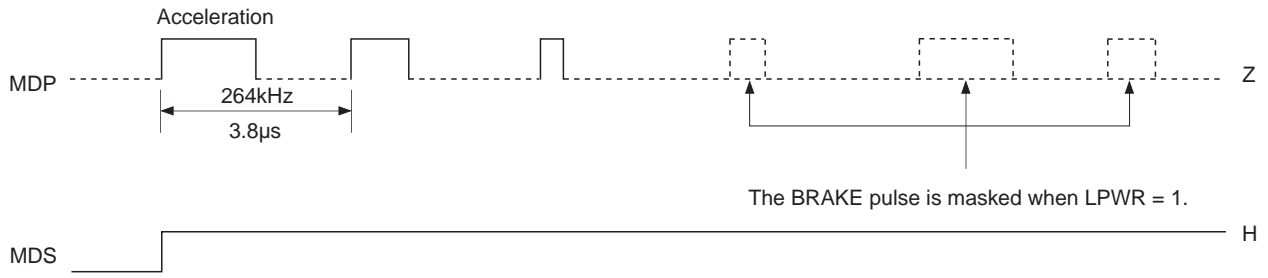
Timing Chart 1-36

CAV-W mode EPWM = 0, LPWR = 0, LPWR2 = 1



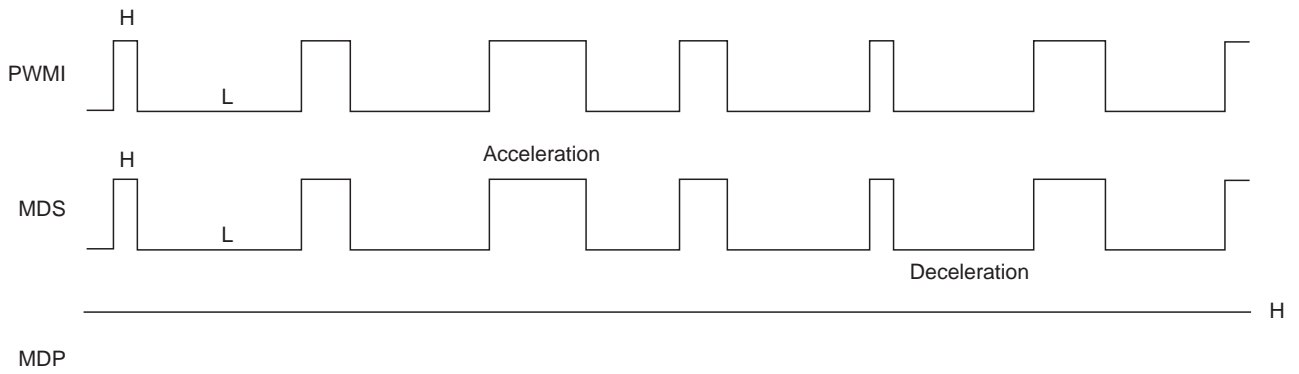
Timing Chart 1-37

CAV-W mode EPWM = 0, LPWR=1, LPWR2 = 1



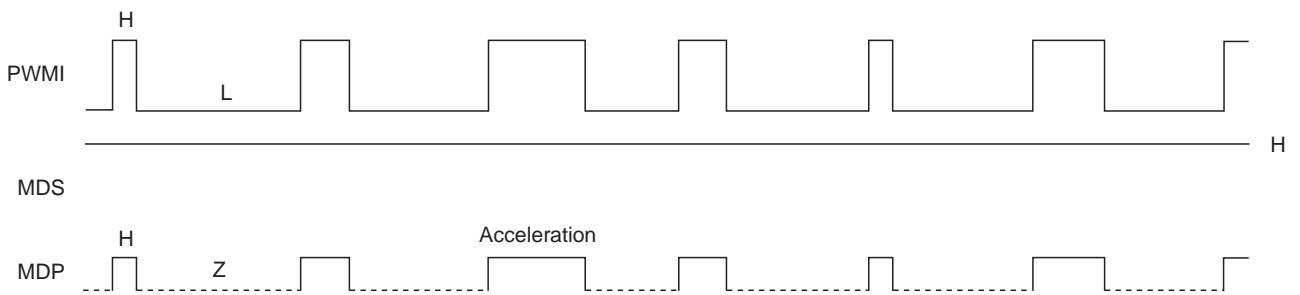
Timing Chart 1-38

CAV-W mode EPWM = 1, LPWR = 0, LPWR2 = 1



Timing Chart 1-39

CAV-W mode EPWM = 1, LPWR = 1, LPWR2 = 1



[2] Subcode Interface

There are two methods for reading out a subcode externally.

The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK.

The subcode-Q can be read out after checking CRC of the 80 bits in the subcode frame.

The subcode-Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

§2-1. P to W Subcode Readout

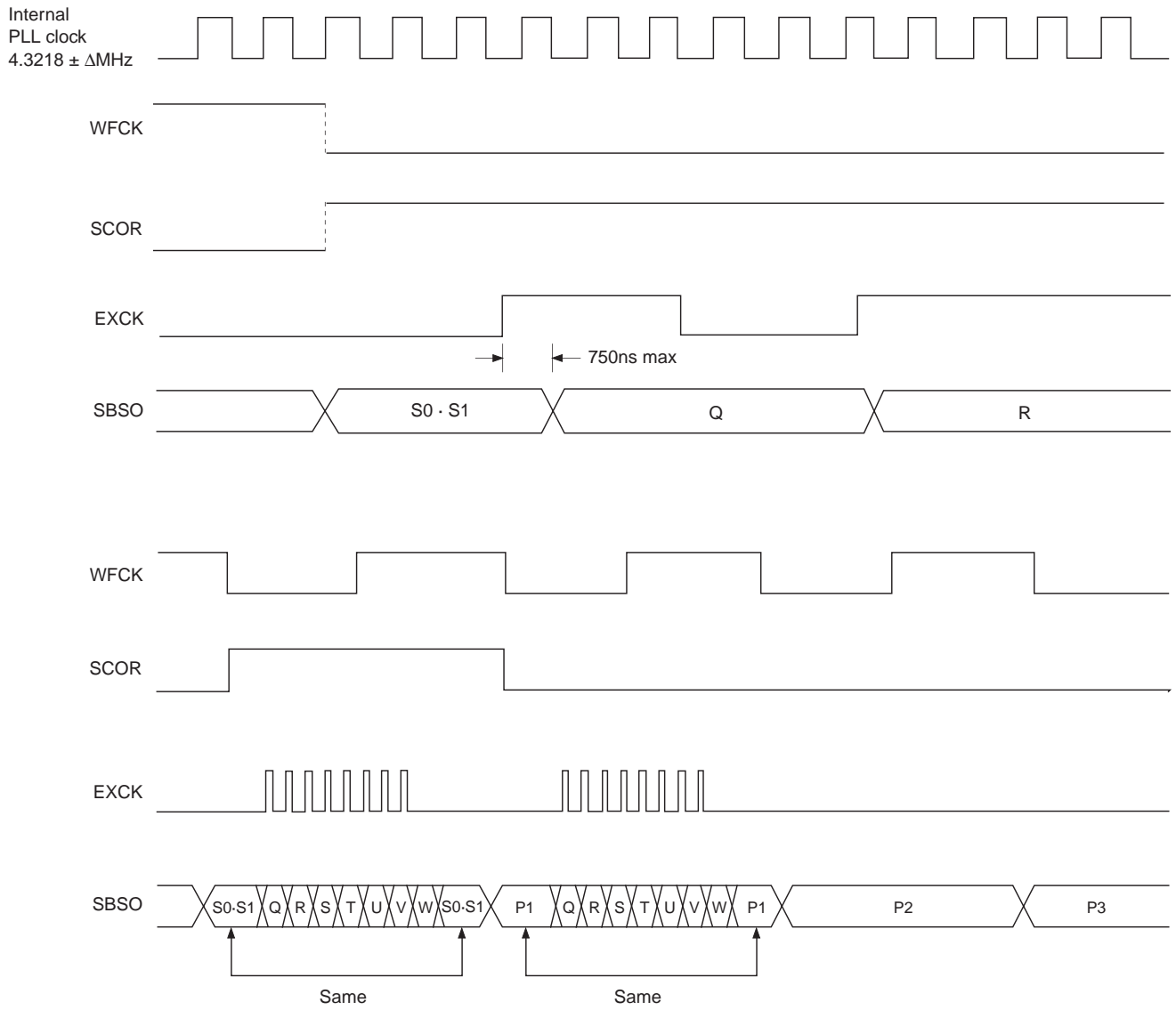
Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-1.)

§2-2. 80-bit Subcode-Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit subcode-Q register.

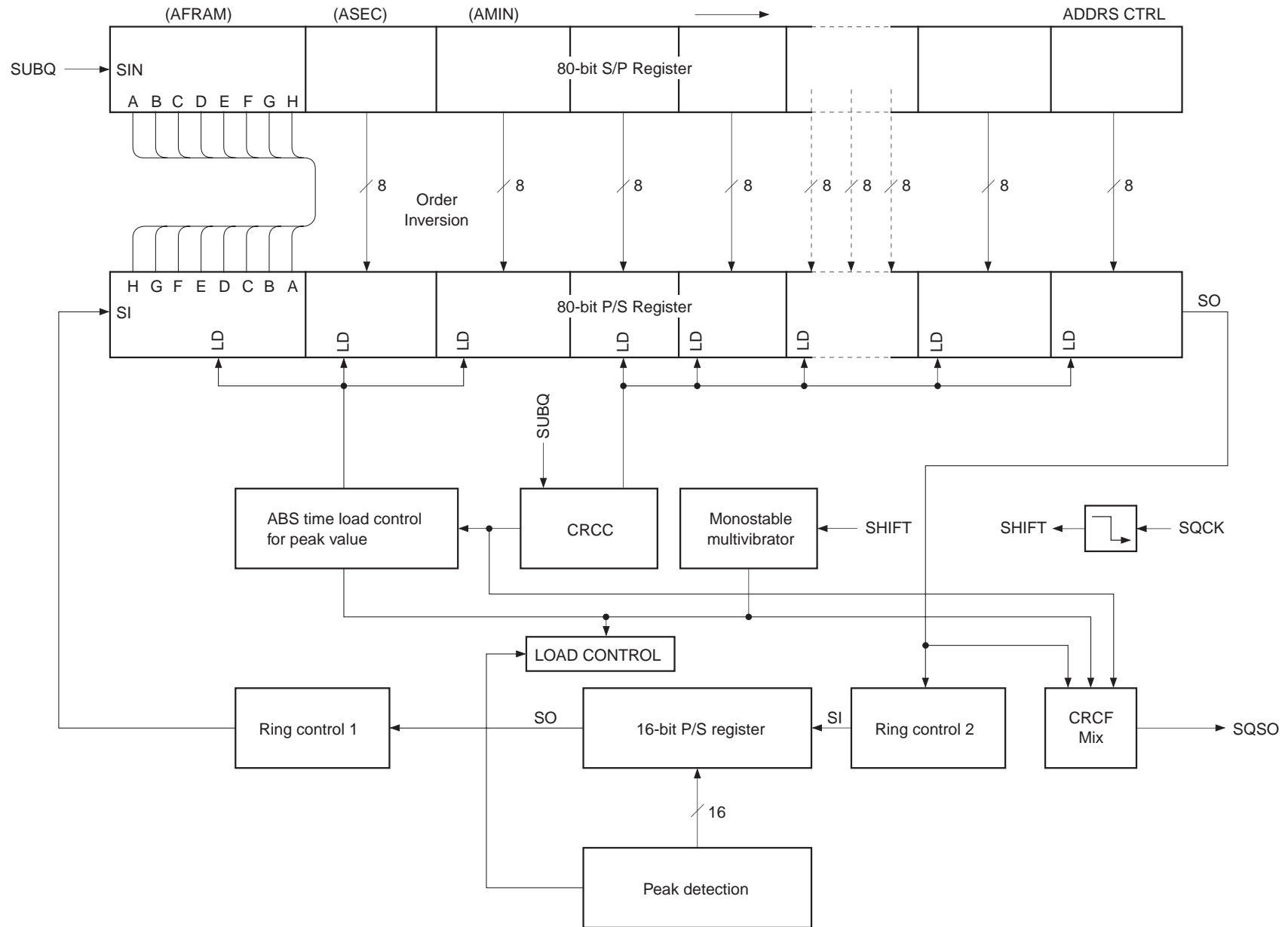
- First, subcode-Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit subcode-Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.
When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.
The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400 μ s. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
In other words, while reading out with a clock cycle shorter than this time constant, these registers will not be rewritten by CRCOK and others.
- The previously mentioned peak detection register can be connected to the shift-in of the 80-bit parallel/serial register.
For ring control 1, input and output are shorted during peak meter and level meter modes.
For ring control 2, input and output are shorted during peak meter mode.
This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
As a result, the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is stored in the memory in peak meter mode as noted in "Description of peak meter mode" on page 95. See Timing Chart 2-3.
- The clock is input from the SQCK pin to perform these operations. The high and low intervals of the clock should be between 750ns and 120 μ s.

Timing Chart 2-1

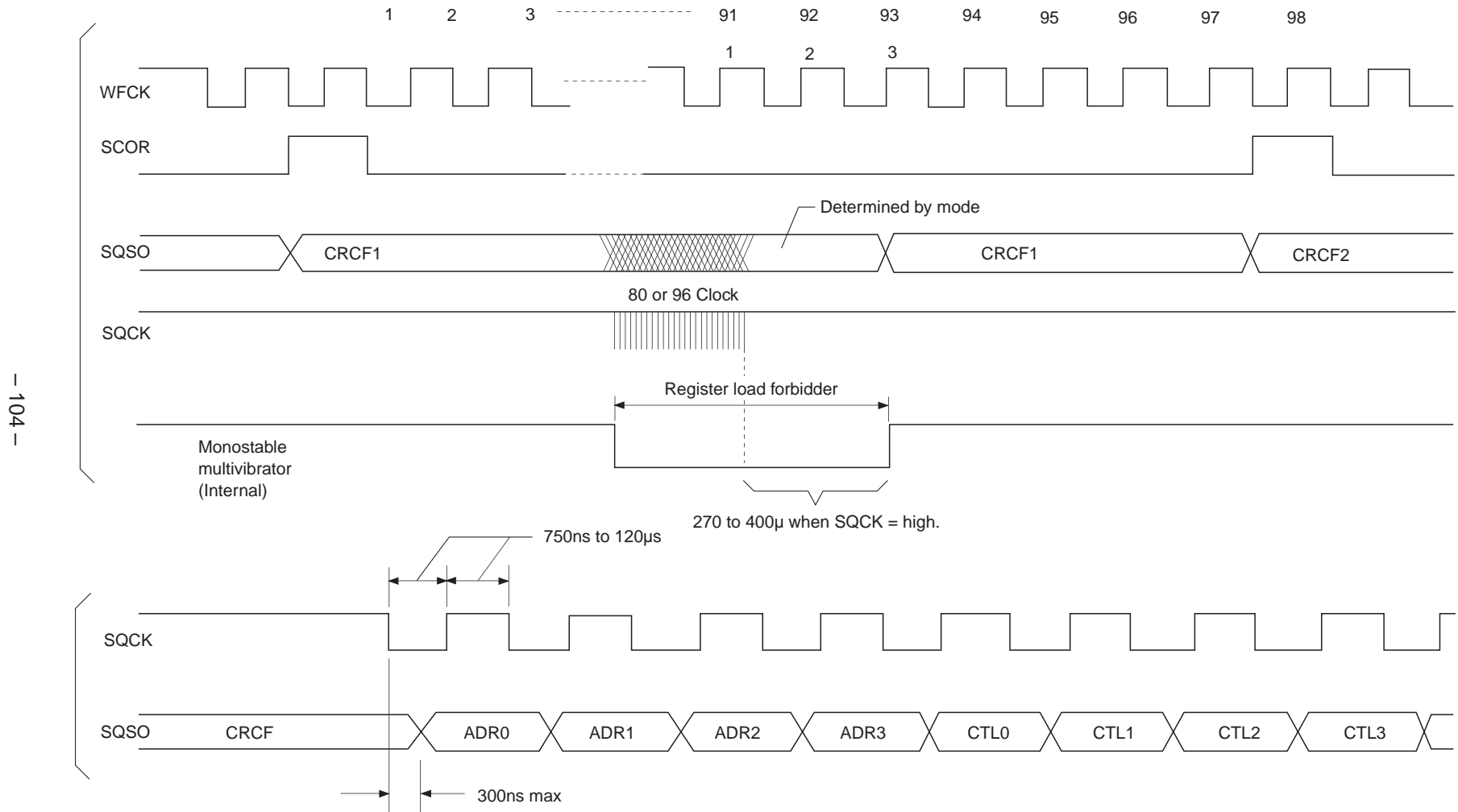


Subcode P.Q.R.S.T.U.V.W Read Timing

Block Diagram 2-2

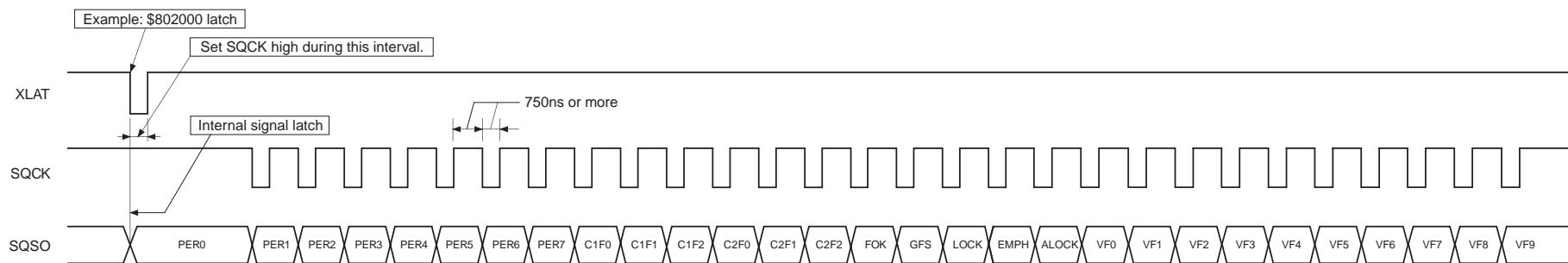


Timing Chart 2-3



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Timing Chart 2-4



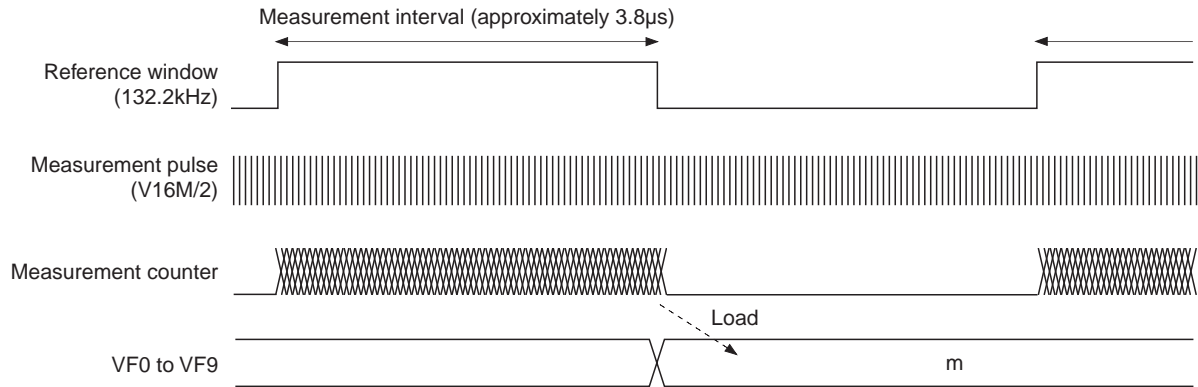
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| Signal | Description |
|--------------|---|
| PER0 to PER7 | RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB. |
| FOK | Focus OK. |
| GFS | High when the frame sync and the insertion protection timing match. |
| LOCK | GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. |
| EMPH | High when the playback disc has emphasis. |
| ALOCK | GFS is sampled at 460Hz; when GFS is high eight consecutive samples, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. |
| VF0 to VF9 | Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See Timing Chart 2-5.) VF0 = LSB, VF9 = MSB. |

| C1F2 | C1F1 | C1F0 | Description |
|------|------|------|--|
| 0 | 0 | 0 | No C1 errors; C1 pointer reset |
| 0 | 0 | 1 | One C1 error corrected; C1 pointer reset |
| 0 | 1 | 0 | — |
| 0 | 1 | 1 | — |
| 1 | 0 | 0 | No C1 errors; C1 pointer set |
| 1 | 0 | 1 | One C1 error corrected; C1 pointer set |
| 1 | 1 | 0 | Two C1 errors corrected; C1 pointer set |
| 1 | 1 | 1 | C1 correction impossible; C1 pointer set |

| C2F2 | C2F1 | C2F0 | Description |
|------|------|------|---|
| 0 | 0 | 0 | No C2 errors; C2 pointer reset |
| 0 | 0 | 1 | One C2 error corrected; C2 pointer reset |
| 0 | 1 | 0 | Two C2 errors corrected; C2 pointer reset |
| 0 | 1 | 1 | Three C2 errors corrected; C2 pointer reset |
| 1 | 0 | 0 | Four C2 errors corrected; C2 pointer reset |
| 1 | 0 | 1 | — |
| 1 | 1 | 0 | C2 correction impossible; C1 pointer copy |
| 1 | 1 | 1 | C2 correction impossible; C2 pointer set |

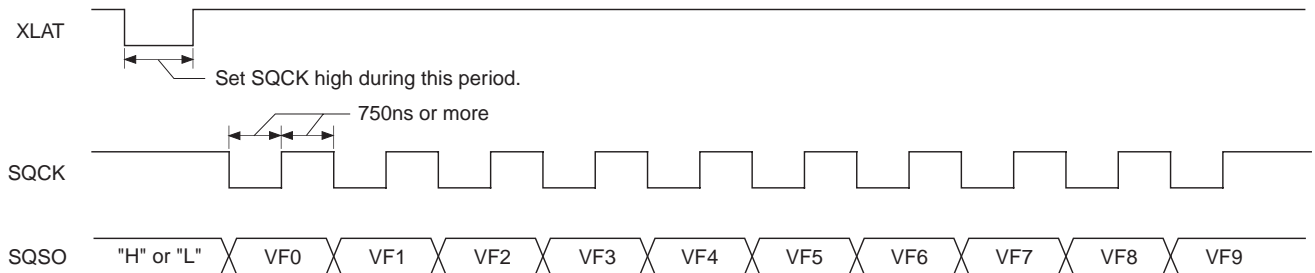
Timing Chart 2-5



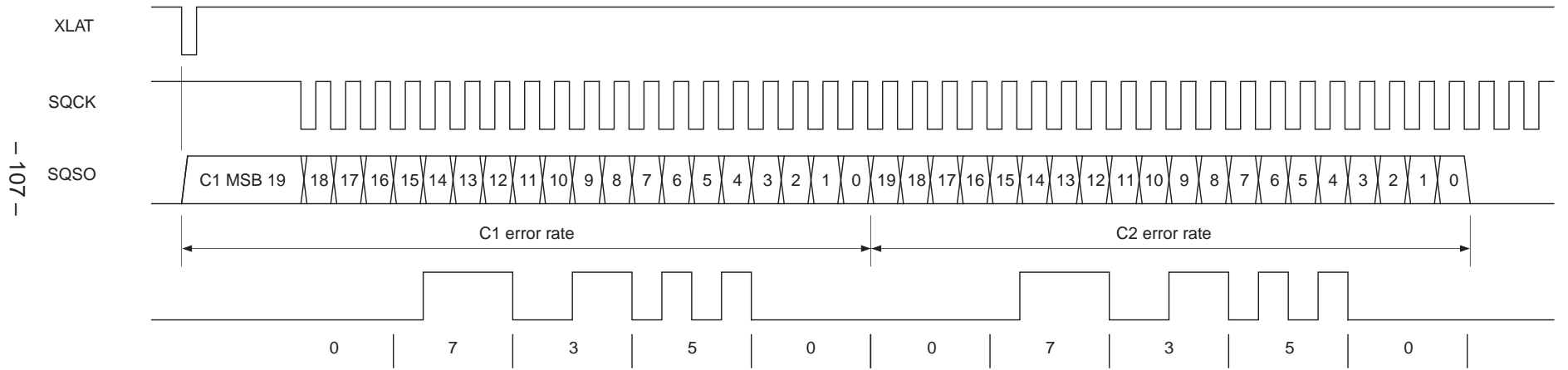
The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{m + 1}{32} \text{ (R: Relative velocity, m: Measurement results)}$$

VF0 to VF9 is the result obtained by counting V16M/2 pulses while the reference signal (132.2kHz) generated from XTAL (XTAI, XTAO) (384Fs) is high. This value is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).



Timing Chart 2-6



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[3] Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§3-1. CLV-N Mode

This mode is compatible with the CXD2510Q, and operation is the same as for conventional control. The PLL capture range is $\pm 150\text{kHz}$.

§3-2. CLV-W Mode

This is the wide capture range mode. This mode allows the conventional PLL to follow the rotational velocity of the disc. This rotational following control uses the built-in VCO2. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below.

When starting to rotate the disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $\$E665X$ to set CAV-W mode and kick the disc, then send $\$E60CX$ to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set high, deceleration pulses are not output, thereby achieving low power consumption mode.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to the desired rotational velocity. The rotational velocity is determined by the VP0 to VP7 setting values or the external PWM. When controlling the spindle with VP0 to VP7, setting CAV-W mode with the $\$E665X$ command and controlling VP0 to VP7 with the $\$DX$ commands allows the rotational velocity to be varied from low speed to quadruple speed. (See "\$DX commands".) When controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using the internal master clock frequency as the parameter. With XTAL (XTAI, XTAO) (384Fs) as the reference frequency, the result after measuring the high interval by the internal master clock is output in 10 bits (VP0 to VP9) from the new CPU interface. These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at quadruple speed. These values match those of the $256 - n$ for control with VP0 to VP7. (See Timing Chart 2-5.)

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc.

Note) The capture range for this mode is theoretically up to the signal processing limit.

Note) Set FLFC to "1" for this mode

§3-4. VCO-C Mode

This is VCO control mode. In this mode, the oscillation frequency of the internal master clock (VCLK) can be controlled by setting \$D commands VP0 to VP7 and VPCTL0, 1. The VCLK oscillation frequency can be expressed by the following equation.

$$VCLK = \frac{1 (256 - n)}{32} \quad \begin{array}{l} n: VP0 \text{ to } VP7 \text{ setting value} \\ 1: VPCTL0, 1 \text{ setting value} \end{array}$$

The VCO1 oscillation frequency is determined by VCLK. The VCO1 frequency can be expressed by the following equation.

- When DSPB = 0

$$VCO1 = VCLK \times \frac{49}{24}$$

- When DSPB = 1

$$VCO1 = VCLK \times \frac{49}{16}$$

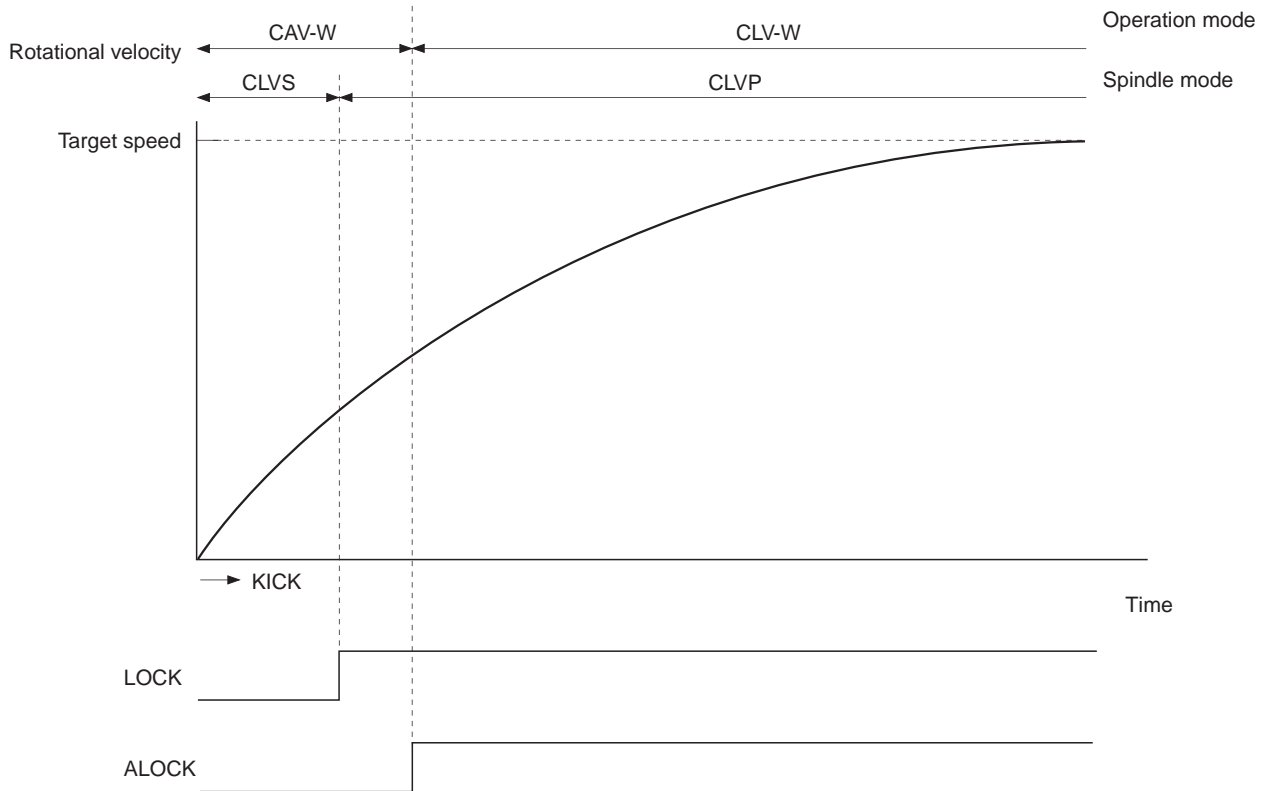


Fig. 3-1. Disc Stop to Regular Playback in CLV-W Mode

CLV-W Mode

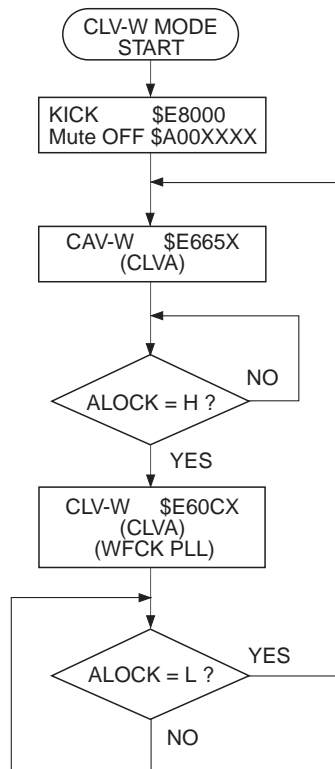


Fig. 3-2. CLV-W Mode Flow Chart

VCO-C Mode

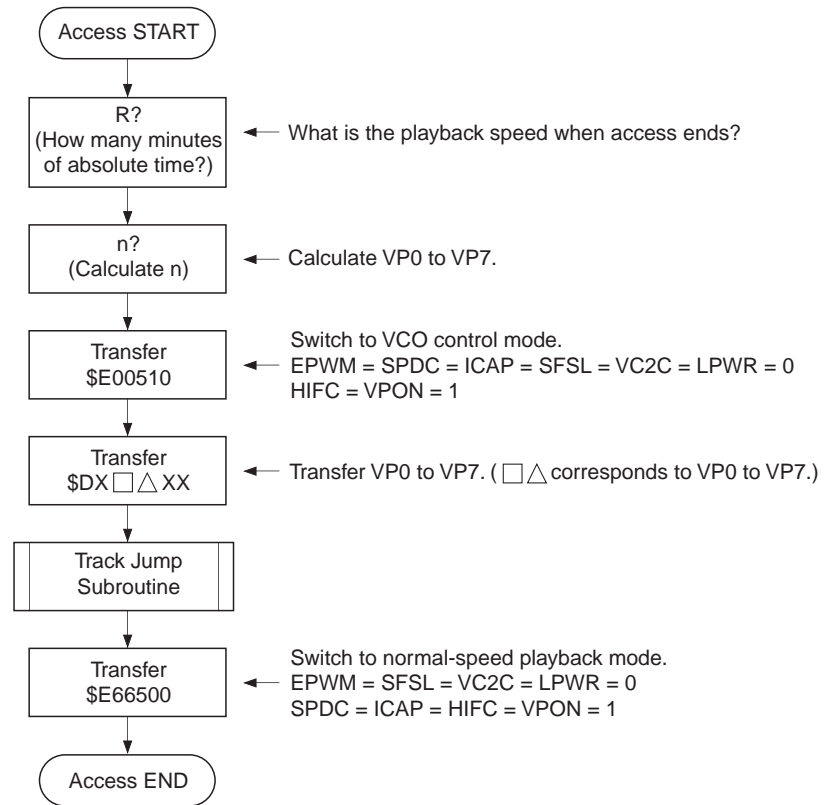


Fig. 3-3. Access Flow Chart Using VCO Control

[4] Description of other functions

§4-1. Channel Clock Recovery by Digital PLL Circuit

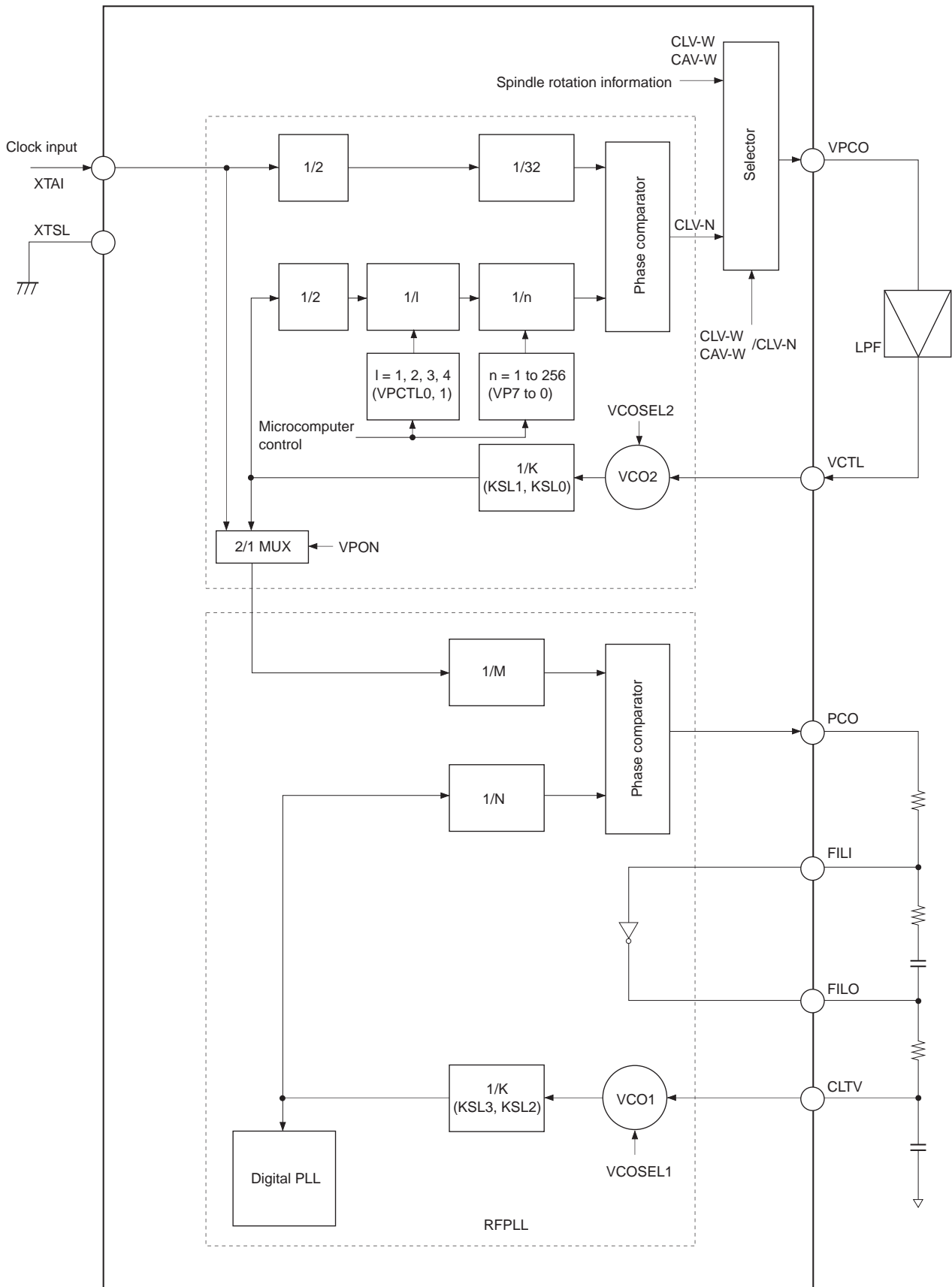
- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system. Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from $3T$ to $11T$.
In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T , that is the channel clock, is necessary.
In an actual player, a PLL is necessary to recover the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.

The CXD3048R has a built-in three-stage PLL.

- The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary. The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that recovers the actual channel clock.
- The digital PLL in CLV-N mode has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When $FLFC = 1$, the secondary loop can be turned off. High frequency components such as $3T$ and $4T$ may contain deviations. In such cases, turning the secondary loop off yields better playability. However, in this case the capture range becomes $\pm 50\text{kHz}$.
- A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

Block Diagram 4-1



§4-2. Frame Sync Protection

- In normal-speed playback, a frame sync is recorded approximately every 136 μ s (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.
- In the CXD3048R, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is set to 12*, and the backward protection counter to 3*. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, etc., a maximum of 12 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.

In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

* Default values. These values can be set as desired by \$C commands SFP3 to SFP0 and SRP3 to SRP0.

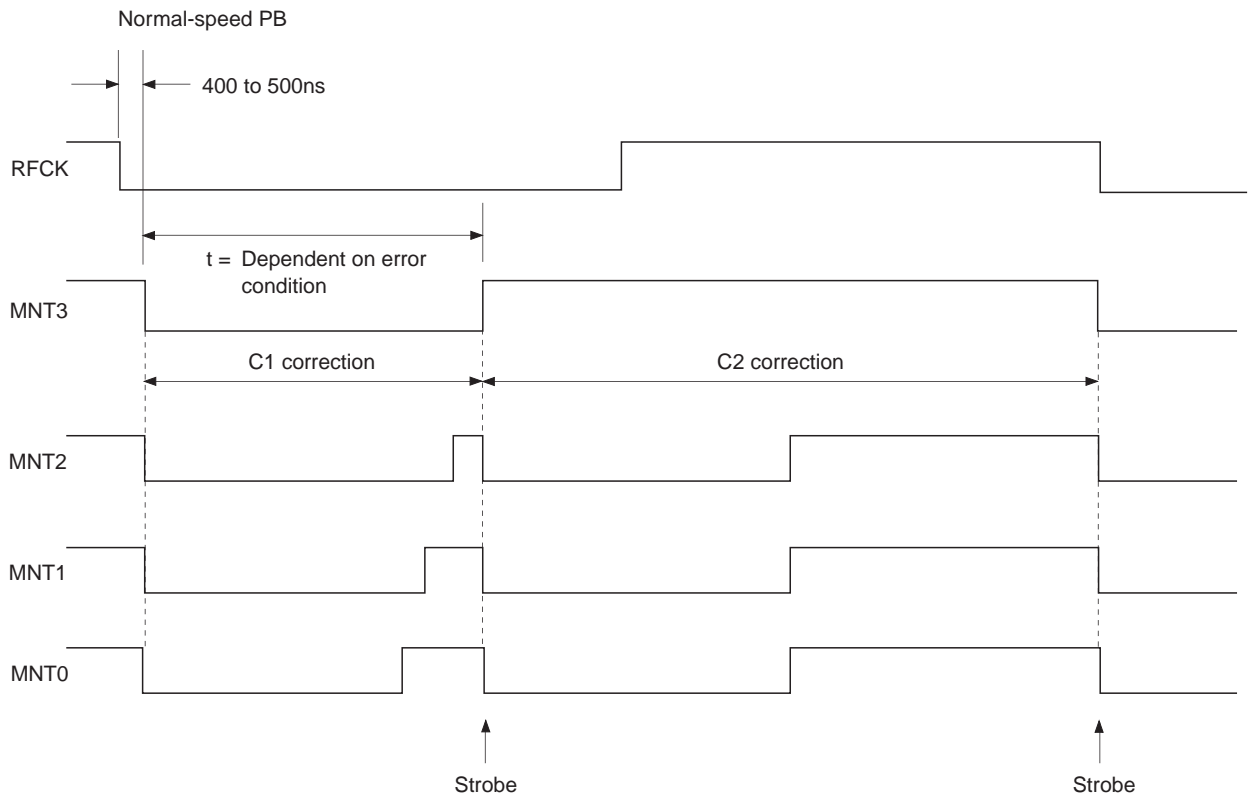
§4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
For C2 correction, the code is created with 24-byte information and 4-byte parity.
Both C1 and C2 are Reed-Solomon codes with a minimum distance of 5.
- The CXD3048R uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal and the operating status of the player.
- The correction status can be monitored externally.
See Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

| MNT3 | MNT2 | MNT1 | MNT0 | Description | |
|------|------|------|------|----------------------------|------------------|
| 0 | 0 | 0 | 0 | No C1 errors; | C1 pointer reset |
| 0 | 0 | 0 | 1 | One C1 error corrected; | C1 pointer reset |
| 0 | 0 | 1 | 0 | | — |
| 0 | 0 | 1 | 1 | | — |
| 0 | 1 | 0 | 0 | No C1 errors; | C1 pointer set |
| 0 | 1 | 0 | 1 | One C1 error corrected; | C1 pointer set |
| 0 | 1 | 1 | 0 | Two C1 errors corrected; | C1 pointer set |
| 0 | 1 | 1 | 1 | C1 correction impossible; | C1 pointer set |
| 1 | 0 | 0 | 0 | No C2 errors; | C2 pointer reset |
| 1 | 0 | 0 | 1 | One C2 error corrected; | C2 pointer reset |
| 1 | 0 | 1 | 0 | Two C2 errors corrected; | C2 pointer reset |
| 1 | 0 | 1 | 1 | Three C2 errors corrected; | C2 pointer reset |
| 1 | 1 | 0 | 0 | Four C2 errors corrected; | C2 pointer reset |
| 1 | 1 | 0 | 1 | | — |
| 1 | 1 | 1 | 0 | C2 correction impossible; | C1 pointer copy |
| 1 | 1 | 1 | 1 | C2 correction impossible; | C2 pointer set |

Table 4-2.

Timing Chart 4-3



§4-4. DA Interface

- The DA interface supports the 48-bit slot interface.

48-bit slot interface

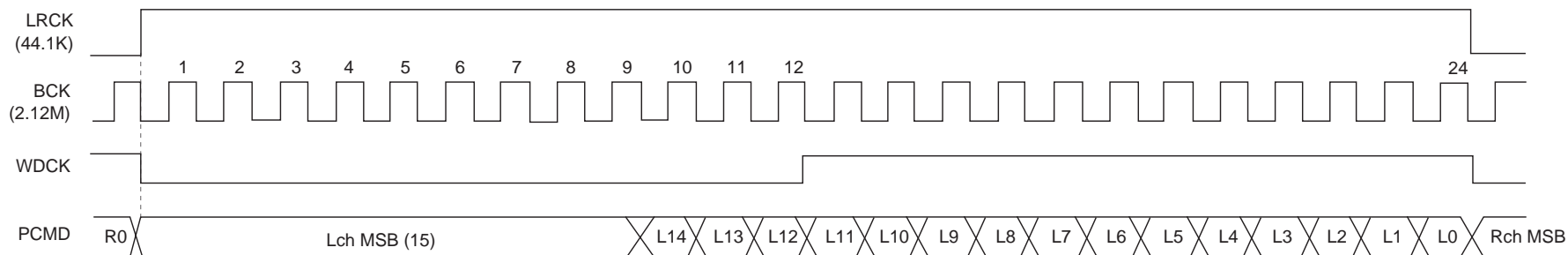
This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.

When LRCK is high, the data is for the left channel.

The output format from the bass boost block supports 18 bits and 20 bits in addition to 16 bits.

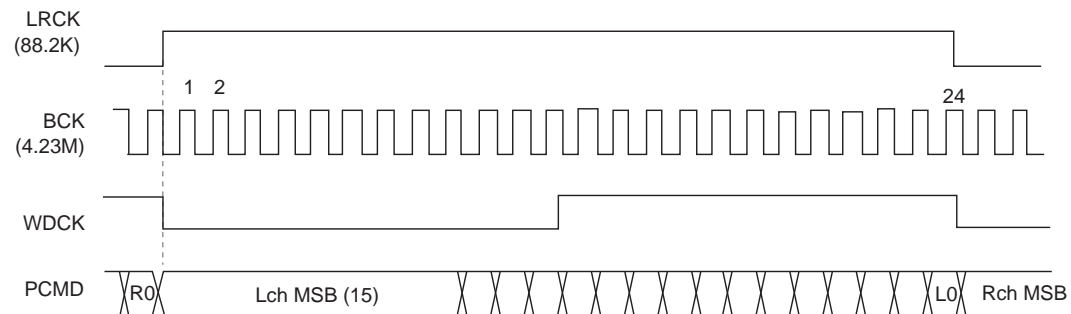
Timing Chart 4-4

48-bit Slot Normal-speed Playback

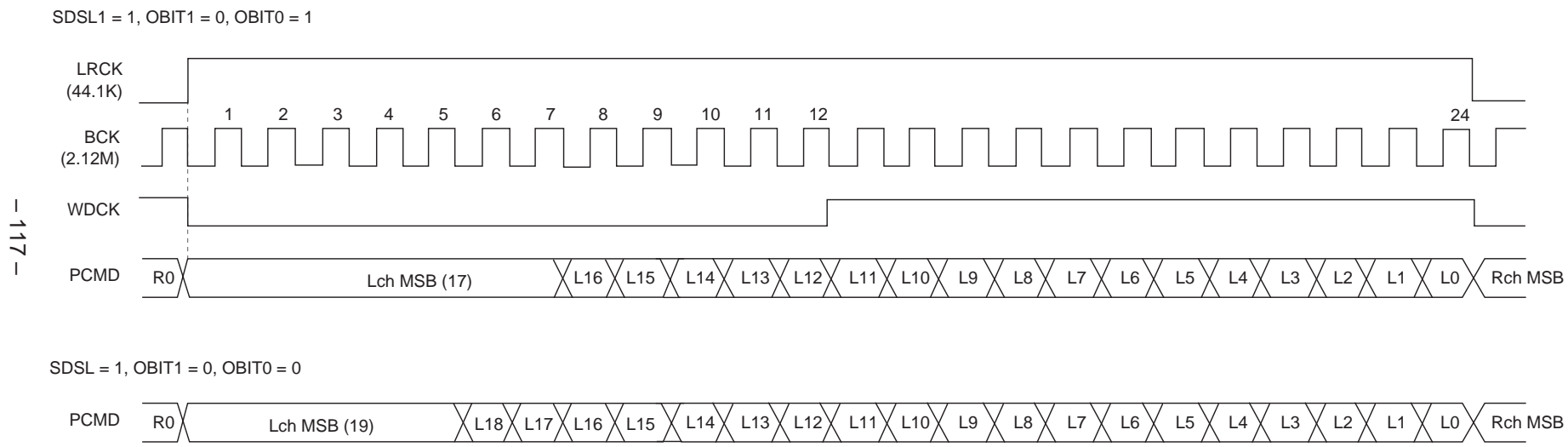


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48-bit Slot Double-speed Playback



Timing Chart 4-5 (DAC output selected)



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§4-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD3048R supports type 2 form 1.

This LSI supports two kinds of Digital Out generation methods; generation from the PCM data read out from the disc, and generation from the DA interface inputs (PCMDI, LRCKI, BCKI).

The timing accuracy of output data depends on the signal accuracy input to XTAI, XTAO pins in CLV-N mode, and the built-in VCO accuracy in VCO-C mode.

§4-5-1. Digital Out from PCM Data

The Digital Out is generated from the PCM data which is read out from the disc.

The clock accuracy of the channel status is automatically set to level II when the crystal clock is used and to level III in CAV-W mode, VCO-C mode or variable pitch mode. In addition, the subcode-Q data matched twice in succession with CRC check are input to the initial 4 bits (bits 0 to 3).

DOUT is output when the crystal is 34MHz and XTSL is high in CLV-N or CLV-W mode with DSPB = 1. Therefore, DOUT is set to off by setting the \$B command MD2 to "0".

Digital Out C bit

| | | | | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|----|----|----|-----|----|----|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | From sub Q ← ID0 ID1 COPY Emph → | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1 | 0 | 0 |
| 32 | 0 | | | | | | | | | | | | | | | |
| 48 | | | | | | | | | | | | | | | | |
| 64 | | | | | | | | | | | | | | | | |
| 176 | | | | | | | | | | | | | | | | |

bit0 to 3 Subcode-Q control bits that matched twice in succession with CRCOK
 bit29 VPON or VARION: 1 Crystal: 0

Table 4-5-1.

§4-5-2. Digital Out from DA Interface Input

The Digital Out is generated from the DA interface input.

Validity Flag and User Data

The Validity Flag is fixed to "0".

The User Data is fixed to "0" or it can be output according to the format by setting 0 data.

For the Q data, first set the Q1 to Q80 data using the \$A90 to \$A99 commands, then the set data can be output according to the digital interface format using the \$A9A command. In addition, CRC operations are performed internally on the Q81 to Q96 data and then this data is output.

The data is output in the order shown in Table 4-5-2.

The setting flow is shown in Figs. 4-5 (a) and 4-5 (b). Fig. 4-5 (a) shows the case when changing all the data, and Fig. 4-5 (b) the case when changing the INDEX, movement time and absolute time.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|------|---|-----|---|---|---|---|---|---|---|---|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | 1 | Q1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36 | 1 | Q2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 48 | 1 | Q3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : | : | : | : | : | : |
| 1164 | 1 | Q96 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 4-5-2.

Channel Status Data

For the Channel Status Data, bits 0, 6 and 7 are fixed to "0". The following items can be set by bits 1, 2, 3 and 8.

- a) Digital data/audio data
- b) Digital copy enabled/prohibited
- c) With/without emphasis
- d) Category code (2 types possible)

Digital Out C bit

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|---|------------|------------|-----------|---|---|---|---|-----------|---|----|----|----|----|----|----|
| 0 | 0 | A/D SEL | COPY En | EMPH D | 0 | 0 | 0 | 0 | CAT b8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32 | 0 | | | | | | | | | | | | | | | |
| 48 | | | | | | | | | | | | | | | | |
| 64 | | | | | | | | | | | | | | | | |
| 176 | | | | | | | | | | | | | | | | |

Table 4-5-3.

Note) In this method, DOUT can be set to off by setting \$B command MD2 to "0" and \$34A command DOUT EN to "0".

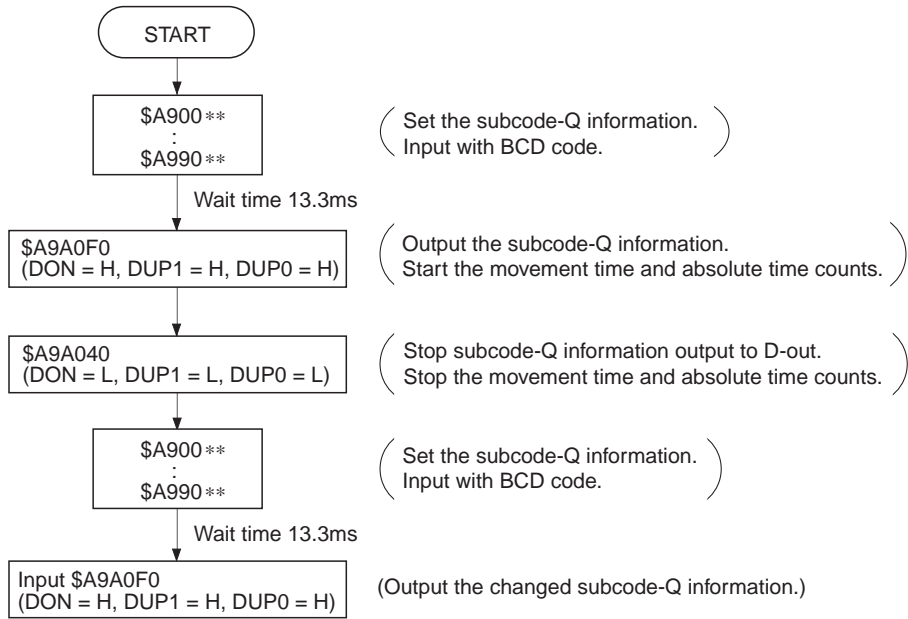


Fig. 4-5(a). Flow Chart for Settings Using Q Data

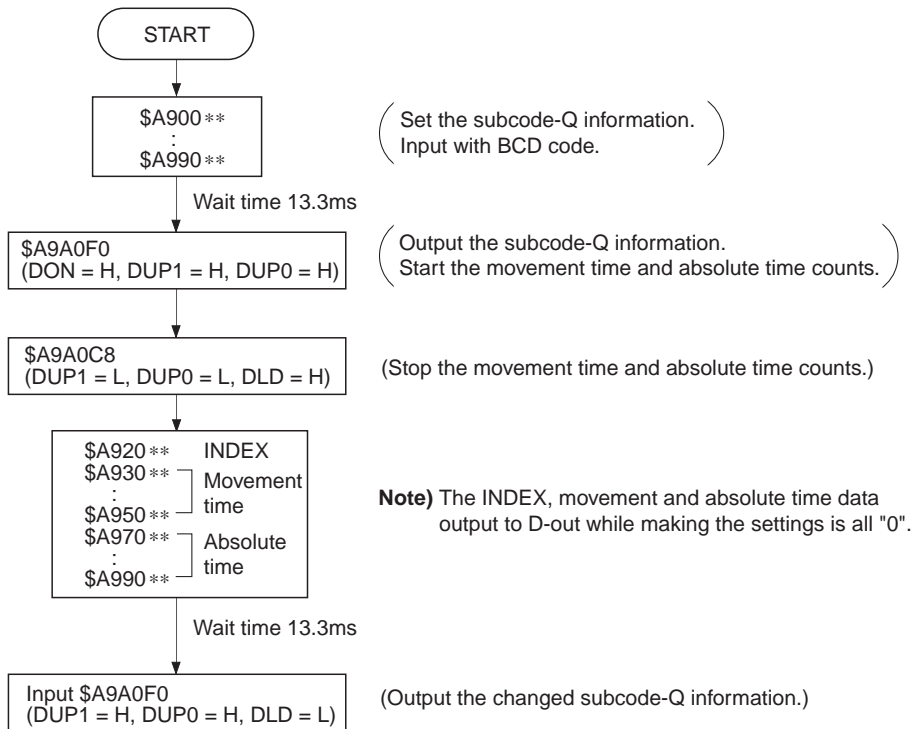


Fig. 4-5(b). Flow Chart for Settings Using Q Data

Digital Audio Data Input

The input signal of the digital audio data is input through the DAC input signal pins PCMDI, LRCKI and BCKI. The input format supports the 48-bit slot, MSB first.

Mute Function

By setting the command bit DOUT_DMUT to "1", all the audio data portions in the Digital Out output can be set to "0" without altering the Channel Status Data.

Input/Output Synchronization Circuit

In normal operation, the DAC automatically synchronizes with the input LRCK. However, synchronization may not be achieved when the input data contains much jitter or during power-on, etc. In such cases, internal operation should be forcibly resynchronized by setting the \$34A command DOUT WOD to "1". Forced synchronization is also required when the operating frequency is changed such as switching between CLV and CAV, etc. Be sure to set DOUT WOD to "0" and then to "1" for forced resynchronization.

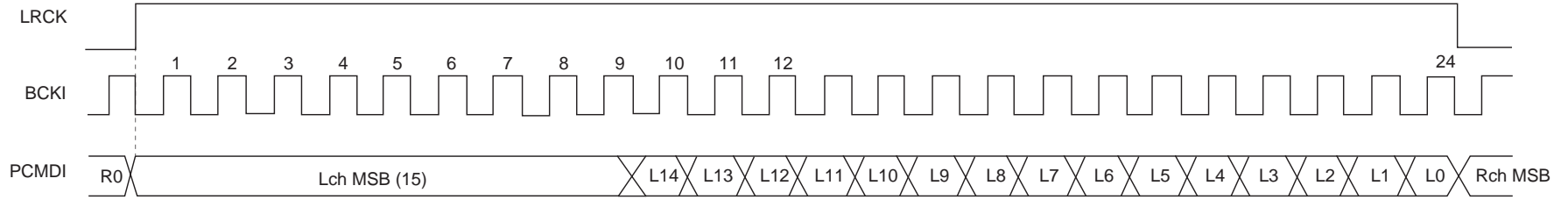
* Resynchronization clears the internal frame counter so that the count starts over from frame 0 after the resynchronization processing. In cases where automatic resynchronization processing is not desirable or the user wants to do it manually, set the \$34A command WINEN to "0" to disable the resynchronization circuit.

DOUT Circuit Clock System

For the DOUT block, the master clock is set using the clock control command MCSL (\$A) employed by the DAC block. Set MCSL to "1" for 768fs, and to "0" for 384fs.

DOUT Block Input Timing Chart

48-bit slot



§4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump, fine search and M-track move are executed automatically.

The servo block operates according to the built-in program during the auto sequence execution (when XBUSY = low), so that commands from the CPU, that is \$0, 1, 2 and 3 commands, are not accepted. (\$4 to E commands are accepted.) When the auto sequencer is used, \$9X command A.SEC ON-OFF is turned on.

In addition, when using the auto sequence, turn the A.SEC ON-OFF of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100 μ s after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built into this LSI as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a \$4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like \$40). See "[1] \$4X commands" concerning the timer value and range. Also, the MAX timer is invalidated by inputting \$4X0.

Although this command is explained in the format of \$4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus (\$47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If \$47 is received from the CPU, the focus servo is turned on according to Fig. 4-6. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on (\$17) should be sent beforehand because they are not involved in this sequence.

• 1-track jump

When \$48 (\$49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-7. Set blind A and brake B with register 5.

• 10-track jump

When \$4A (\$4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-8. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

- 2N-track jump

When \$4C (\$4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-9. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used when N is 16 or more.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

- Fine search

When \$44 (\$45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-10. The differences from a 2N-track jump are that a higher precision is achieved by controlling the traverse speed, and a longer distance jump can be performed by controlling the sled. The track jump count N is set with register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F with register 6 and overflow G with register 5. Also, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls with register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set with register 6.) Then, the tracking and sled servos are turned on.

Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count $N - \alpha$ for the traverse monitor counter which is set with register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be set again.

- M-track move

When \$4E (\$4F for REV) is received from the CPU, a FWD (REV) M-track move is performed in accordance with Fig. 4-11. M can be set to 2^{16} tracks. Like the 2N-track jump, COUT is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or more. The M-track move is executed by moving only the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servos are turned off after M tracks have been counted through COUT or MIRR unlike for the other jumps. Transfer \$25 from the microcomputer after the actuator has stabilized.

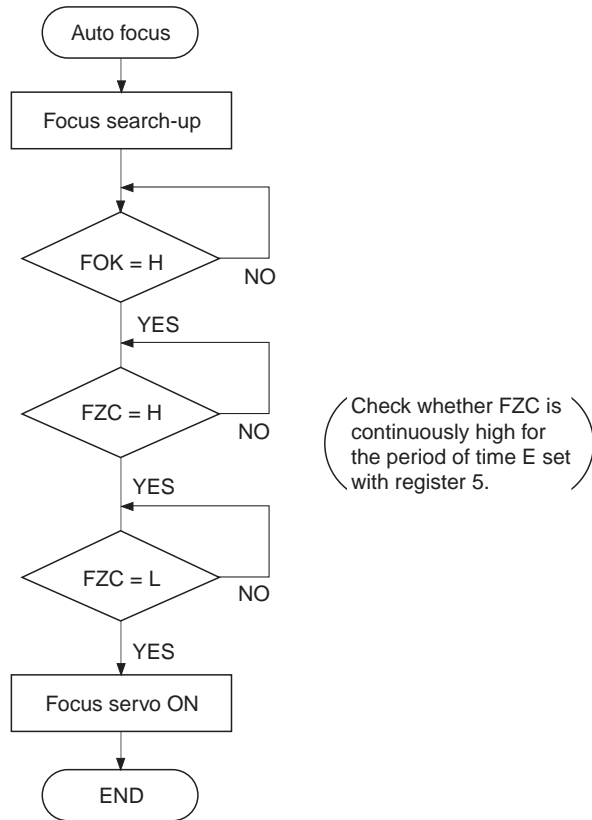


Fig. 4-6-(a). Auto Focus Flow Chart

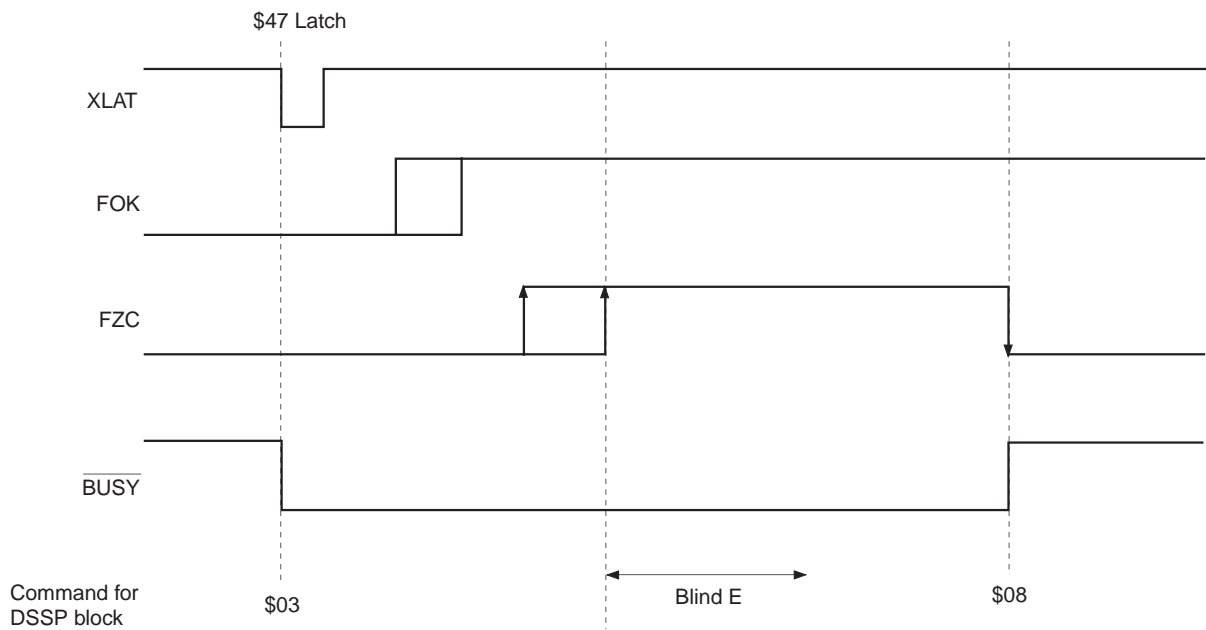


Fig. 4-6-(b). Auto Focus Timing Chart

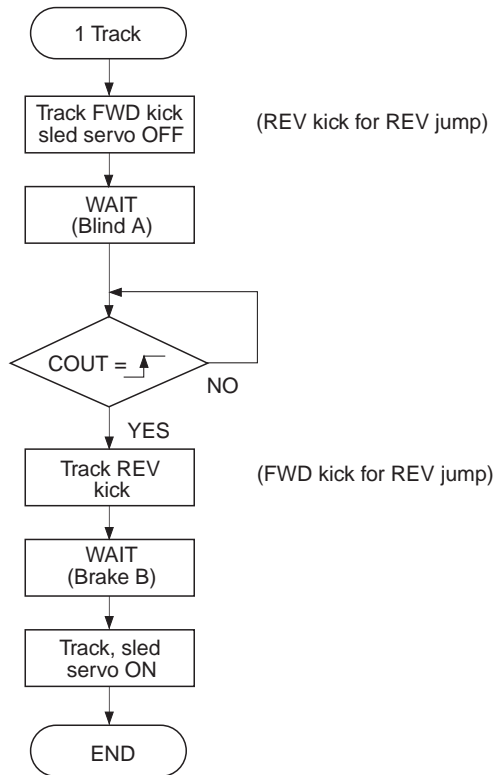


Fig. 4-7-(a). 1-Track Jump Flow Chart

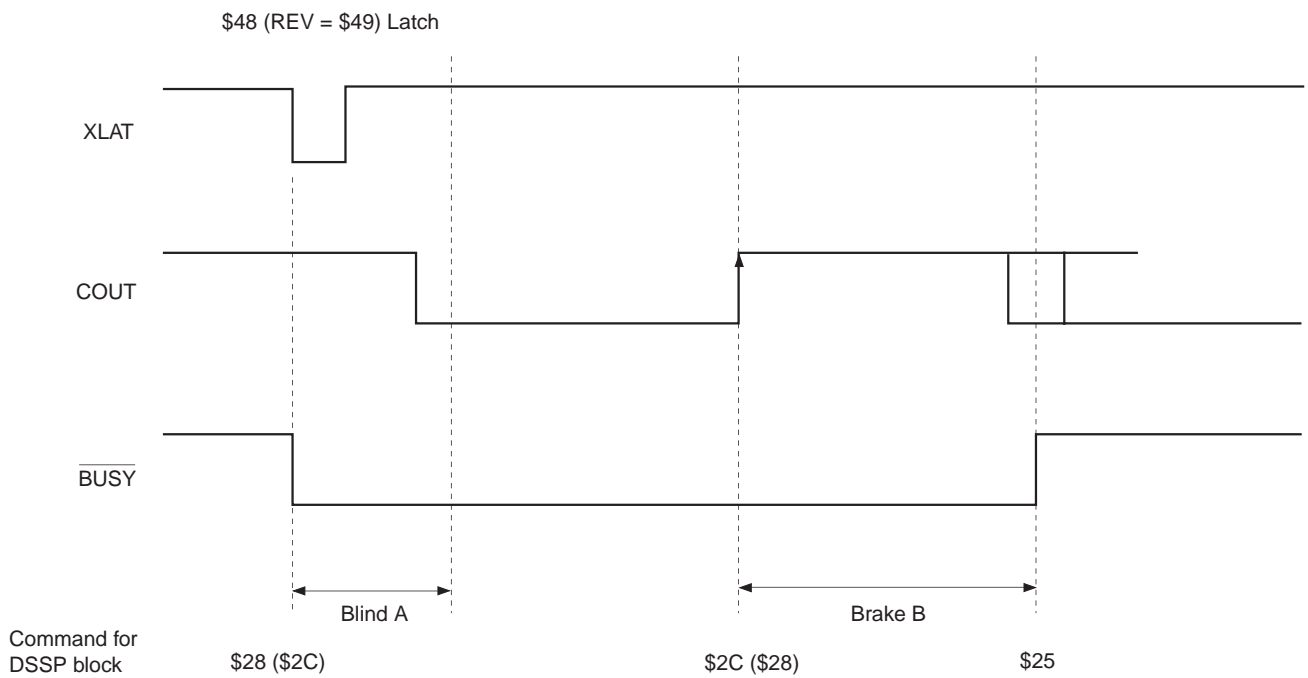


Fig. 4-7-(b). 1-Track Jump Timing Chart

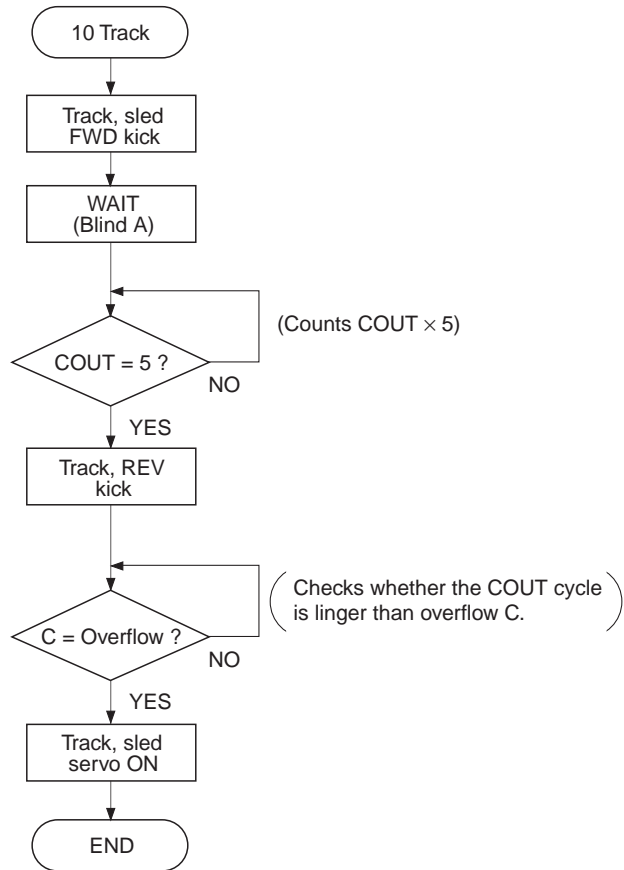


Fig. 4-8-(a). 10-Track Jump Flow Chart

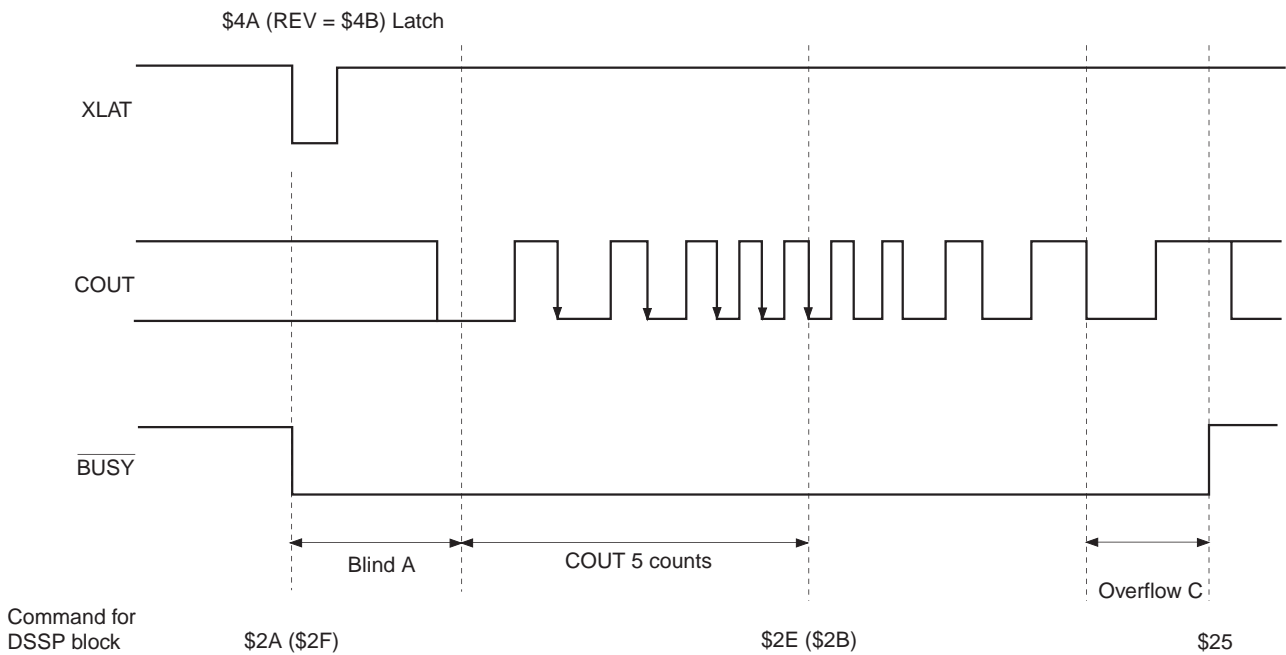


Fig. 4-8-(b). 10-Track Jump Timing Chart

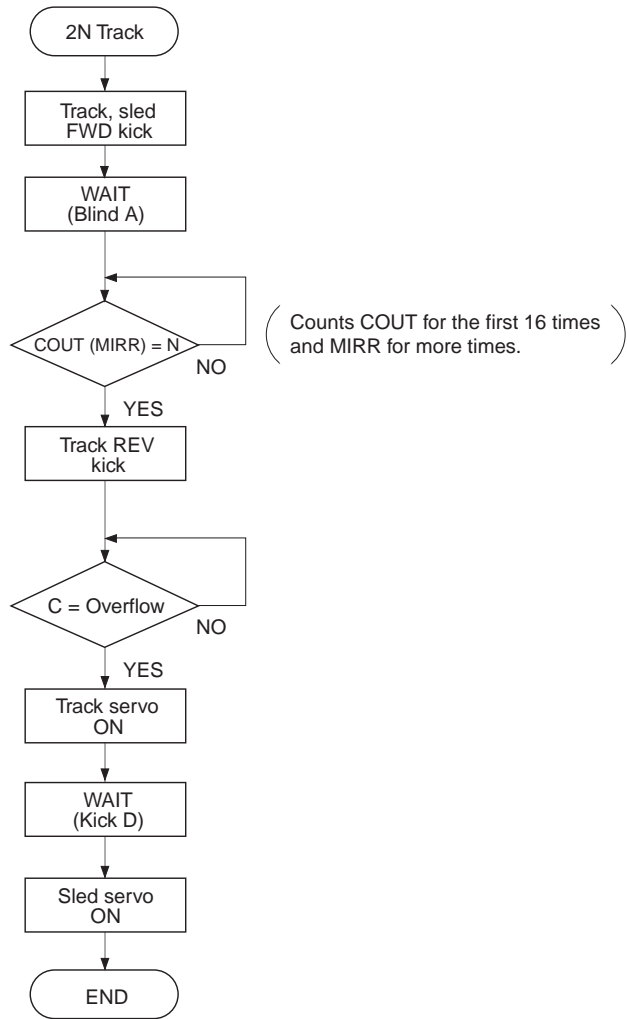


Fig. 4-9-(a). 2N-Track Jump Flow Chart

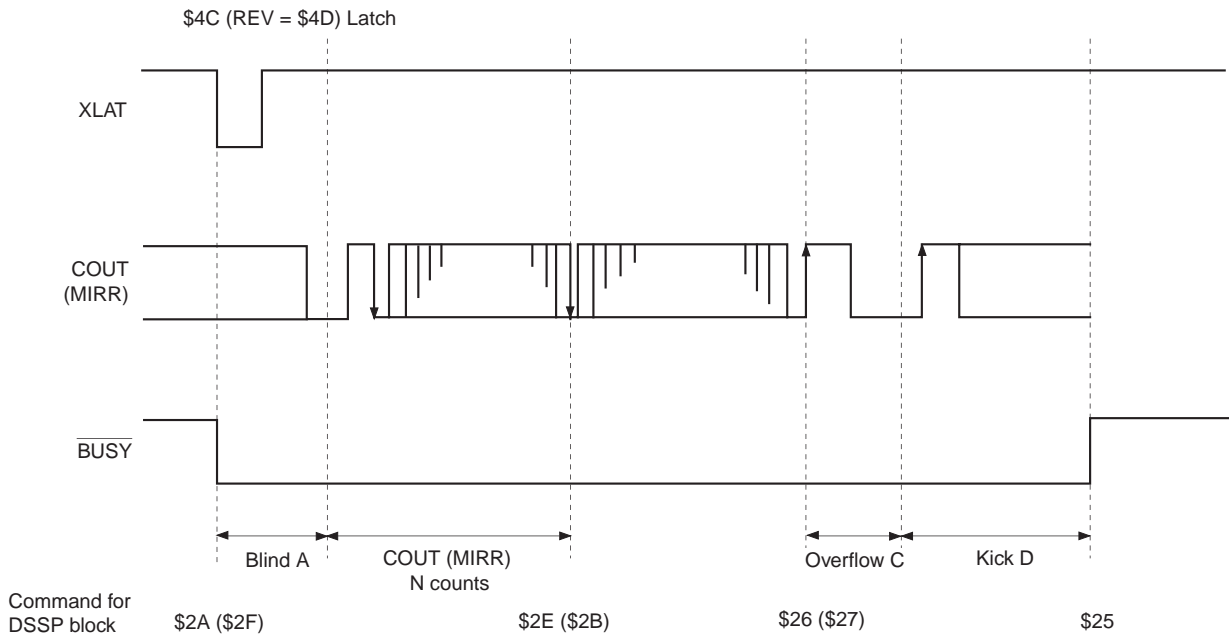


Fig. 4-9-(b). 2N-Track Jump Timing Chart

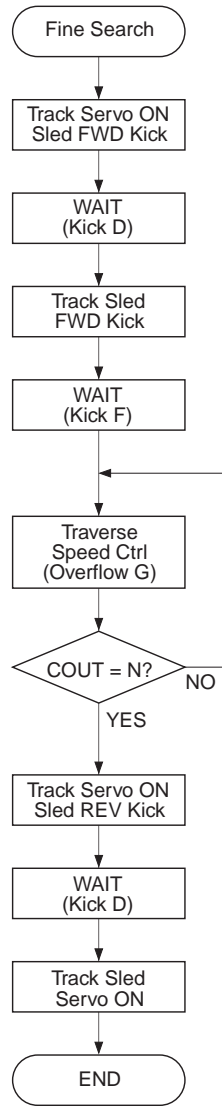


Fig. 4-10-(a). Fine Search Flow Chart

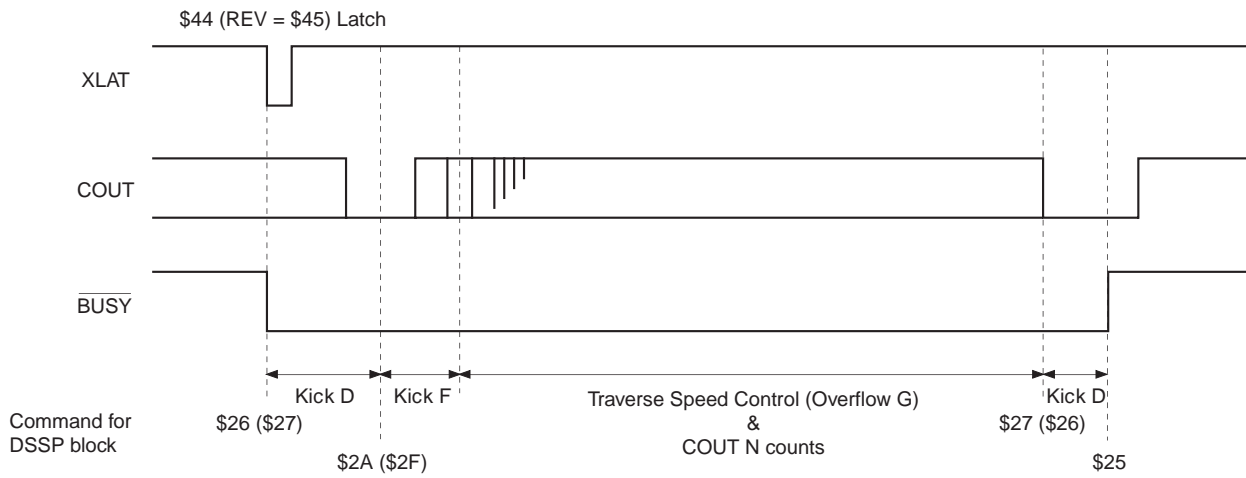


Fig. 4-10-(b). Fine Search Timing Chart

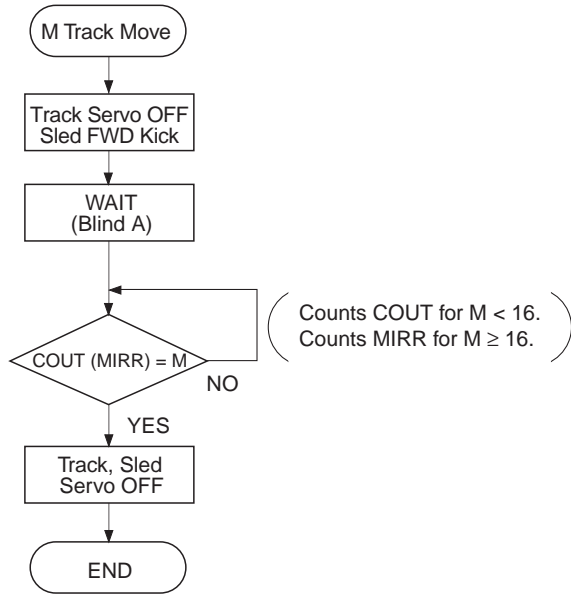


Fig. 4-11-(a). M-Track Move Flow Chart

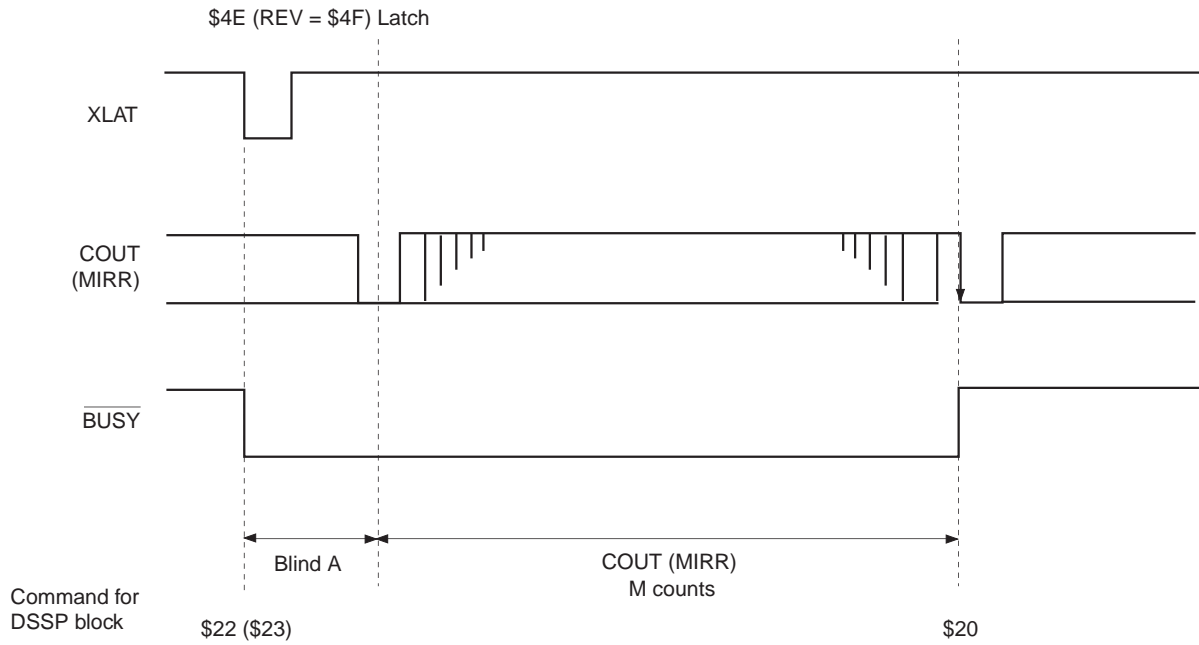
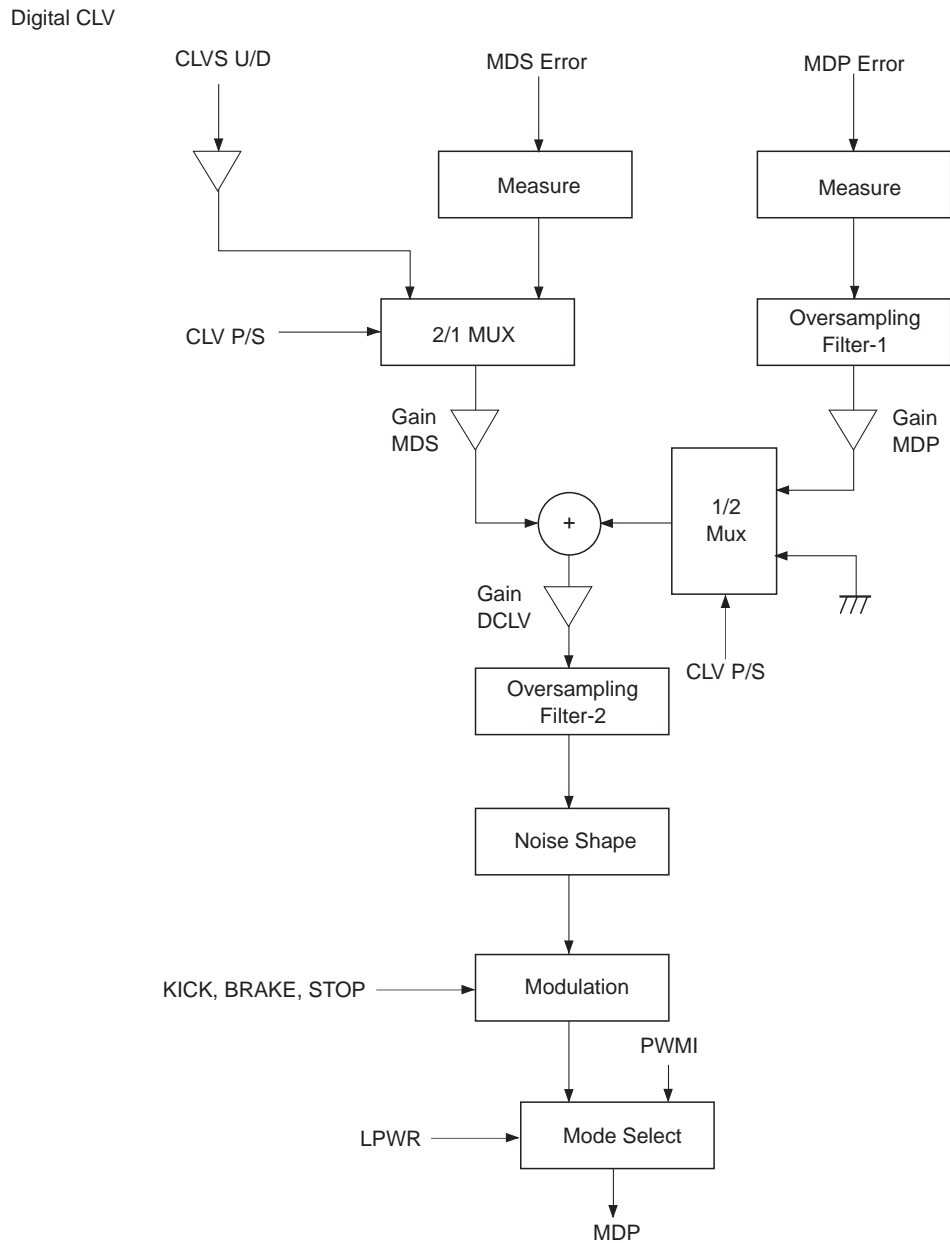


Fig. 4-11-(b). M-Track Move Timing Chart

§4-7. Digital CLV

Fig. 4-12 shows the block diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.



CLVS U/D: Up/down signal from CLVS servo
 MDS error: Frequency error for CLVP servo
 MDP error: Phase error for CLVP servo
 PWMI: Spindle drive signal from the microcomputer for CAV servo

Fig. 4-12. Block Diagram

§4-8. CD-DSP Block Playback Speed

In the CXD3048R, the following playback modes can be selected through different combinations of the XTAI, XTSL pins, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency division commands (KSL3, KSL2) and command transfer rate selector (ASHS) in CLV-N or CLV-W mode.

| Mode | XTAI | XTSL | DSPB | VCOSEL1* ¹ | ASHS | Playback speed | Error correction* ² |
|------|-------|------|------|-----------------------|------|----------------|--------------------------------|
| 1 | 768Fs | 1 | 0 | 0/1 | 0 | 1× | C1: double; C2: quadruple |
| 2 | 768Fs | 1 | 1 | 0/1 | 0 | 2× | C1: double; C2: double |
| 3 | 768Fs | 0 | 0 | 1 | 1 | 2× | C1: double; C2: quadruple |
| 4 | 768Fs | 0 | 1 | 1 | 1 | 4× | C1: double; C2: double |
| 5 | 384Fs | 0 | 0 | 0/1 | 0 | 1× | C1: double; C2: quadruple |
| 6 | 384Fs | 0 | 1 | 0/1 | 0 | 2× | C1: double; C2: double |
| 7 | 384Fs | 1 | 1 | 0/1 | 0 | 1× | C1: double; C2: double |

*¹ Actually, the optimal value should be used together with KSL3 and KSL2.

*² When §8 command ERC4 = 1, C2 is quadruple correction even when DSPB = 1.

The playback speed can be varied by setting VP0 to VP7 in CAV-W mode. See "[3] Description of Modes" for details.

§4-9. Description of DAC Block and Shock-proof Memory Controller Block Circuits

The CXD3048R inputs data from the CD-DSP block to the DAC block via the shock-proof memory controller block.

The data from the shock-proof memory controller block is output externally as bass-boosted data via the DBB circuit.

When not using the DAC block, the data from the shock-proof memory controller block can be output directly to the outside of the LSI.

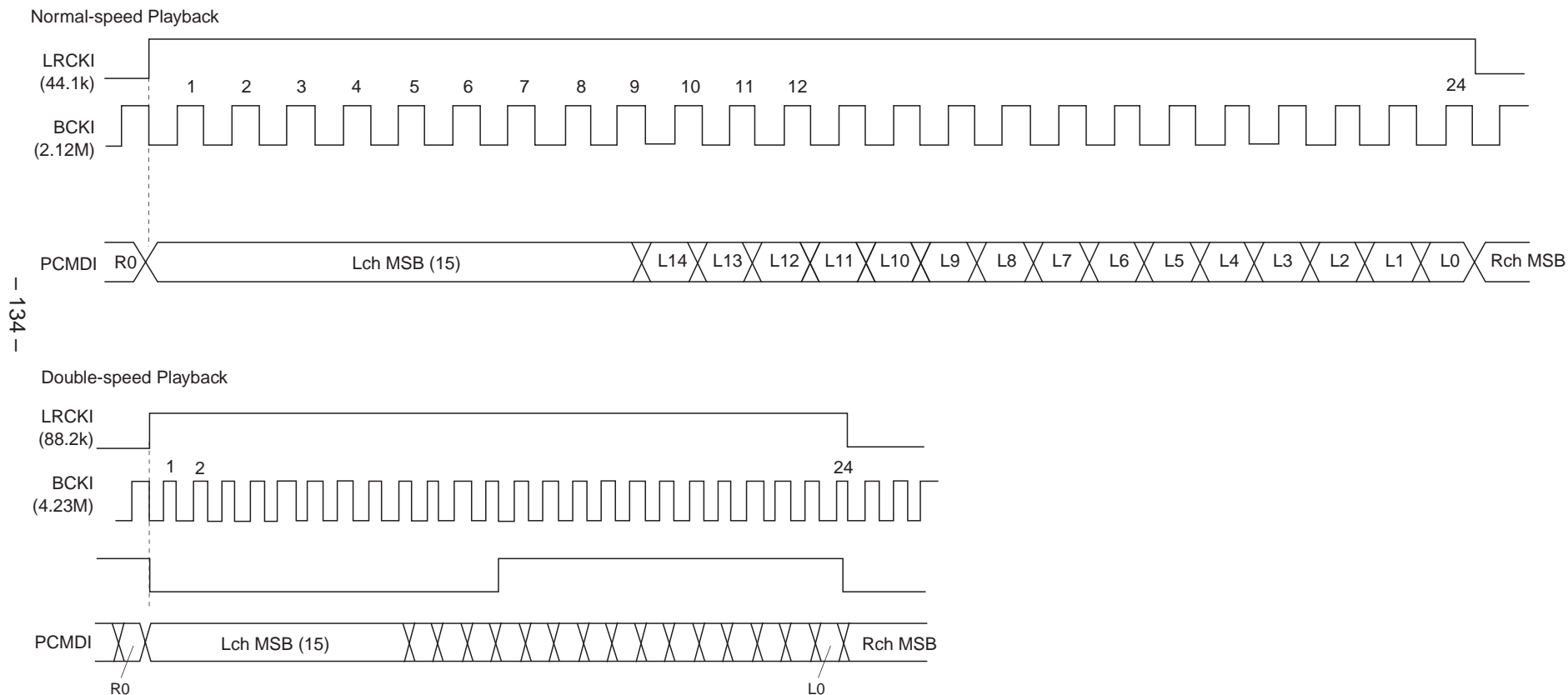
Also, when not using the shock-proof memory controller, the data can be input directly from the CD-DSP block to the DAC block.

The DAC block output format supports 16, 18 or 20 bits.

§4-10. DAC Block Input Timing

Fig. 4-13 shows the input timing chart to the DAC block.

The CXD3048R can transfer data from the CD-DSP block to the DAC block via an external route. This allows the data to be sent to the DAC block via an audio DSP, etc.



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Fig. 4-13. Input Timing to the DAC Block

§4-11. Description of DAC Block Functions

Zero Data Detection

When the condition where the lower 4 bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued for about 300ms (16384/44.1kHz), zero data is detected. Zero data detection is performed independently for the left and right channels.

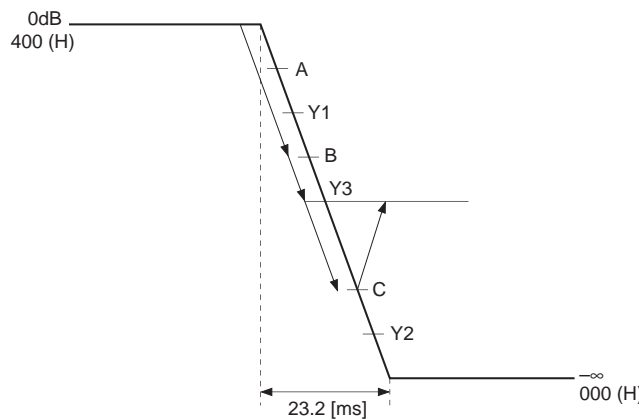
Mute flag output

The LRMU pin goes active when any one of the following conditions is met. (when \$AA command ORMU = 0)
 The polarity can be selected by the \$A5X command ZDPL.

- When zero data is detected
- When a high signal is input to the SYSM pin and the state continues for approximately 300ms
- When the \$A5 command SMUT is set and the state continues for approximately 300ms

Attenuation Operation

Assuming the attenuation commands X1, X2 and X3, the corresponding audio outputs are Y1, Y2 and Y3 (Y1 > Y3 > Y2). First, the command X1 is sent and then the audio output approaches Y1. When the command X2 is sent before the audio output reaches Y1 (A in the figure), the audio output passes Y1 and approaches Y2. And, when the command X3 is sent before the audio output reaches Y2 (B or C in the figure), the audio output approaches Y3 from the value (B or C in the figure) at that point.

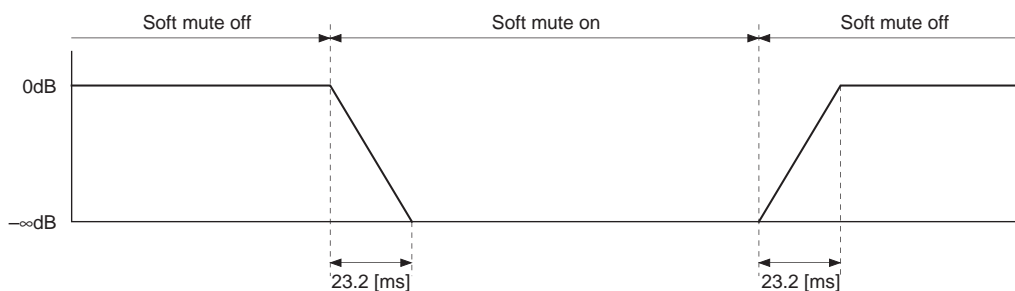


DAC Block Mute Operation

Soft mute

Soft mute results and the input data is attenuated to zero when any one of the following conditions is met.

- When attenuation data of 000 (h) is set
- When \$A5 command SMUT is set to "1"
- When a high signal is input to the SYSM pin



Zero detection mute

Analog mute is applied to the respective channel when \$AX command ZMUTA is set to "0" and zero data is detected for the left or right channel. (See "Zero data detection".)

When \$AX command ZMUTA is set to "0", analog mute is applied even if the mute flag output condition is met.

LRCK Synchronization

Synchronization is performed at the first rising edge of the LRCK input when reset.

After that, synchronization is lost when the LRCK input frequency changes, etc., so resynchronization must be performed.

The LRCK input frequency changes when the master clock of the LSI is switched and the playback speed changes such as the following cases.

- When the XTSL pin switches between high and low
- When the \$9 command DSPB setting changes
- When the \$A4 command MCSL setting changes
- When operation switches between CLV mode and CAV mode

For resynchronization, set the \$A5 command XWOC to "1", wait for one LRCK cycle or more, and then set XWOC to "0".

Digital High and Bass Boost

High and bass boost without external parts is possible using the built-in digital filter.

Perform the following operations when turning boost off or when lowering the current boost level.

1. Set \$A5X command BSTCL to "1".
2. Wait 20ms or more, set the boost level or turn boost off, then set \$A5X command BSTCL to "0".

High-cut Filter

This filter lowers the high-frequency level by approximately 8dB.

The frequency response is shown in Fig. 4-14.

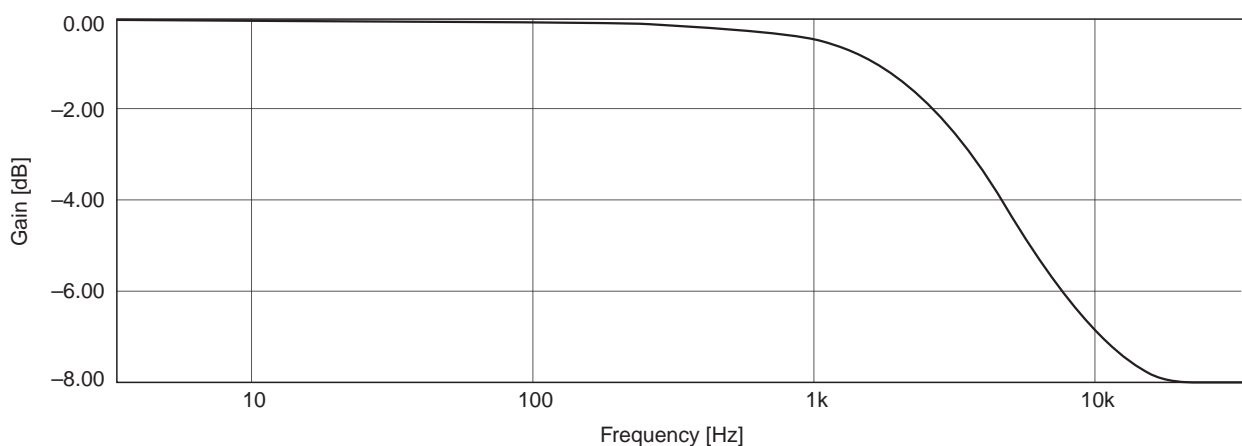


Fig. 4-14. High-Cut Filter Frequency Response

Compressor, Dynamic High and Bass Boost

1. Frequency Response and I/O Characteristics

Fig. 4-15 shows the frequency response for dynamic high boost and bass boost.

This figure shows the frequency response for a high boost turnover frequency of 5kHz and a bass boost turnover frequency of 160Hz. The boost level and turnover frequency can be set independently for high boost and bass boost. In addition, all frequencies are lowered by approximately 2dB in order to prevent clipping, so the medium frequencies are -2dB output. The high boost and bass boost levels indicate the relative values from this level.

Next, the compressor, high boost and bass boost I/O characteristics are shown in Fig. 4-17.

As shown in this figure, the compressor characteristics span all frequencies. In addition, the high boost and bass boost characteristics are for when the input signal is sufficiently higher or lower than the turnover frequency.

The boost levels can be set independently. Uth and Lth on the vertical axis are the gain control threshold values, and the desired output value can be taken from the area enclosed by the parallelograms near these levels. The Uth and Lth settings are described hereafter.

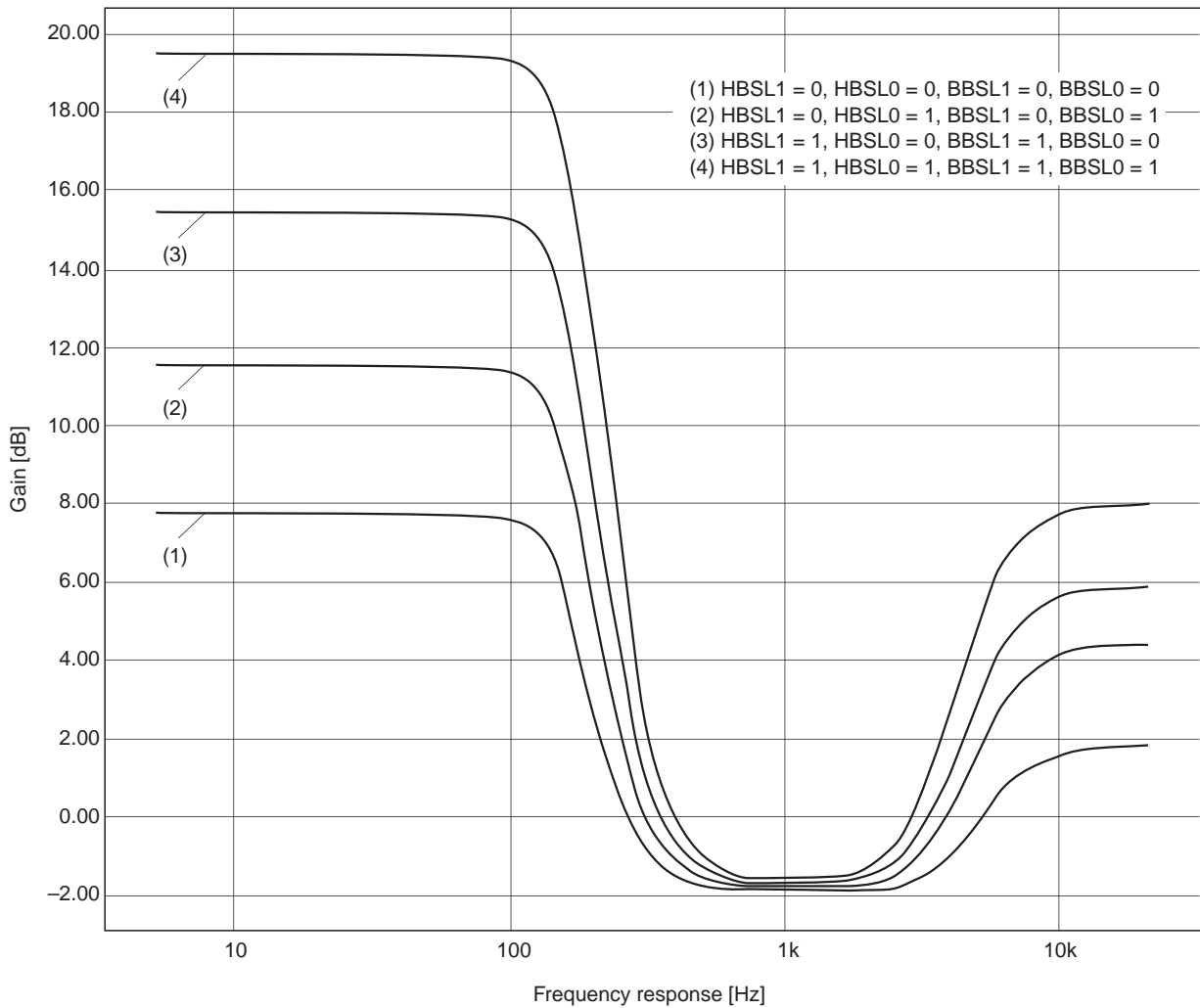


Fig. 4-15. Digital Bass Boost Frequency Response

2. Settings

When performing dynamic processing, the auditory volume and other characteristics change according to the boost levels and various other settings. The values that can be set by the serial commands and the resulting effects are described below.

2-1. Boost Level

The boost level can be set independently for the compressor, high boost and bass boost. Boost level here refers to the maximum boost level when a low level signal is input. The boost level changes over time when a high level signal is input in order to prevent clipping.

2-2. Gain Control Thresholds

The gain control thresholds are Uth and Lth. When the level exceeds Uth, the gain is reduced; when the level falls below Lth, the gain is increased. If both Uth and Lth are set to large values, the volume increases and the respective boost effects are emphasized. On the other hand, some sources may be clipped due to the balance with the boost level. These values can be set independently for the compressor and high/bass boost. The same values are shared for high and bass boost.

2-3. Attack Time, Release Time

The attack time represents the speed at which the gain is reduced after high level input, and the release time represents the speed at which the gain is increased when the input level suddenly becomes smaller. If these values are set to "fast", the boost effects increase. Like the gain control thresholds, these values can be set independently for the compressor and high/bass boost.

2-4. Envelope Detection Release Time

This sets the output signal envelope coefficient used for gain control. When set to "fast", the boost effects increase. This setting is shared by compressor and high/bass boost.

| High boost | Bass boost | Attack time | Release time | Lch | Uch |
|------------|------------|-------------|--------------|-------|--------|
| * | +10dB | Standard | Standard | -12dB | -1.9dB |
| * | +14dB | Slow | Standard | -12dB | -1.9dB |
| * | +18dB | Slow | Standard | -12dB | -1.9dB |
| * | +22dB | Slow | Standard | -12dB | -1.9dB |

Table 4-16. Recommended Dynamic Bass and High Boost Settings

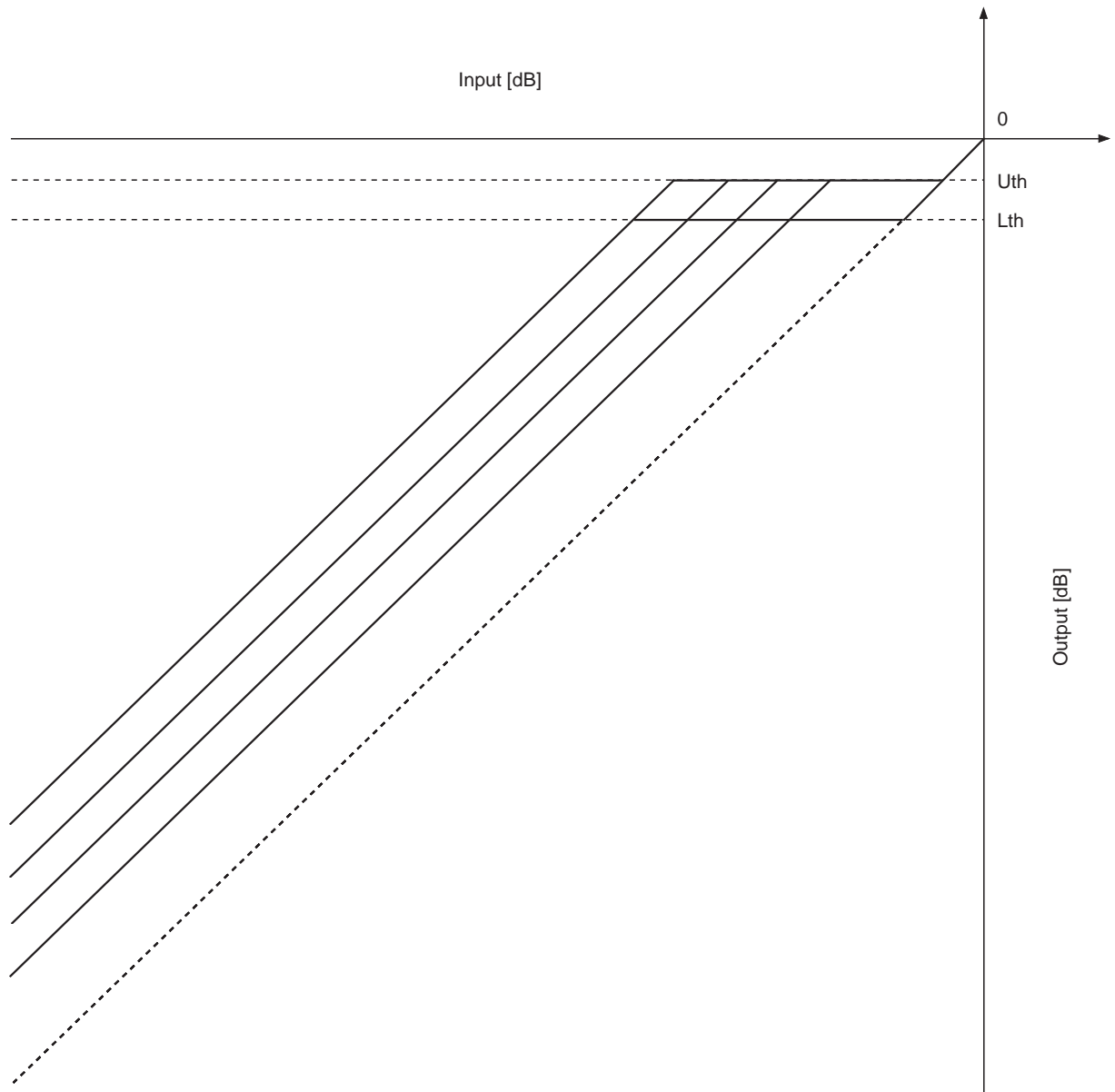


Fig. 4-17. Dynamic Processing I/O Characteristics

| | Uth [dB] | Lth [dB] | Boost level [dB] |
|------------|-----------|----------|------------------|
| Compressor | -8.0 | -23 | 6 |
| High boost | -1.9/-0.9 | -12/-4.4 | 4/6/8/10 |
| Bass boost | -1.9/-0.9 | -12/-4.4 | 10/14/18/22 |

§4-12. LPF Block

The CXD3048R contains a secondary active LPF.
The LPF block application circuit is shown in Fig. 4-18.

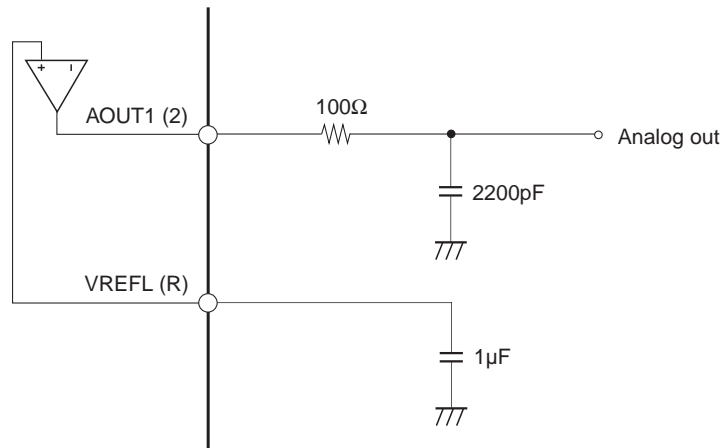


Fig. 4-18. LPF External Circuit

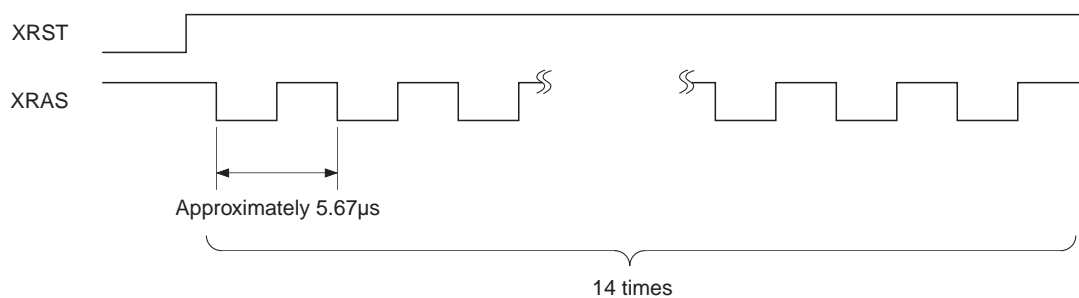
§4-13. Description of Shock-proof Memory Controller Block Functions

§4-13-1. DRAM I/F

A 4M DRAM or 16M DRAM can be selected as the external buffer RAM. The 16M DRAM supports either row address 2^{12} and column address 2^{10} or row address 2^{11} and column address 2^{11} .

Refresh is performed by data access, and the refresh cycle is approximately 11.6ms when 4M DRAM is selected, or approximately 46.4ms ($2^{10} \times 2^{12}$) or 23.2ms ($2^{11} \times 2^{11}$) when 16M DRAM is selected.

In addition, XRAS-only-refresh is executed 14 times in order to initialize the RAM after the power is turned on and the DRAM, which is to be used by the \$A4X commands RSL1 and RSL0, is selected. Data access to the DRAM is not possible during this period.



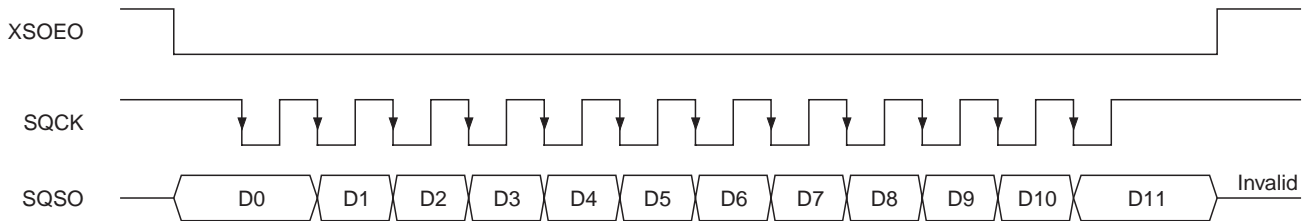
§4-13-2. Switching from Data Through Mode to Shock-proof

The CXD3048R performs refresh by data access.

When switching from (1) Shock-proof mode to (2) data through mode to (3) Shock-proof mode, be sure to reset all of WA, VWA and RA before performing data access for (3).

§4-13-3. CPU Serial Data Output (when \$A7X STASEL = 1)

Data is read out by setting the XSOEO command low and inputting SQCK. The data contents at the falling edge of the XSOEO command are output from the SQSO pin at the falling edge of SCK.



- D0: XWPHD Data write to DRAM prohibited signal (low for $XFUL + \overline{ROF} + WRNG$)
- D1: QRCVD Indicates whether XQOK was registered as a defined address after it was sent.
(High = registration OK)
- D2: XEMP Low when the DRAM is empty of valid data. (VWA = RA)
- D3: AM15 Address monitor; indicates the amount of valid data remaining.
- D4: AM16 Address monitor; indicates the amount of valid data remaining.
- D5: AM17 Address monitor; indicates the amount of valid data remaining.
- D6: AM18 Address monitor; indicates the amount of valid data remaining.
- D7: AM19 Address monitor; indicates the amount of valid data remaining.
- D8: AM20 Address monitor; indicates the amount of valid data remaining.
- D9: AM21 Address monitor; indicates the amount of valid data remaining.
- D10: XFUL Low when the DRAM is full and there is no write area.
- D11: ROF High when the DSP RAM has overflowed.

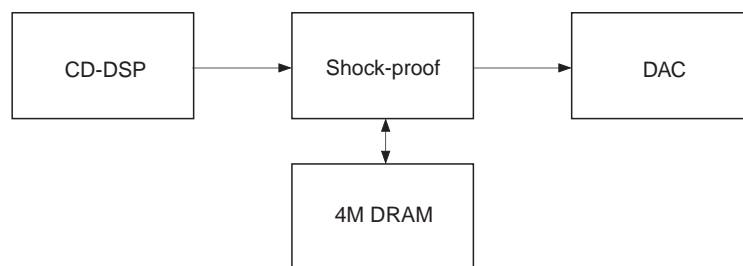
Note) When GRSCOR is low, QRCVD is high when data write to the DRAM is enabled, even if a negative pulse is input to XQOK.

§4-13-4. Data Linking

In order to restart write after PCM data write to the DRAM has been interrupted due to sound skipping or other factors, continuity must be maintained between the data written last and the subsequent data to be written. Conventional systems fix an aim at the data linking point, compare the preceding DRAM reference data with the data read from the disc, and then link the data when matching data is detected. However, when using music software where a fixed pattern is repeated, this system may link the data at an incorrect point. In addition, if pre-value hold or interpolation is performed at the point to be linked, data linking may not be possible at all. In order to eliminate these data linking errors, the CXD3048R generates a crystal accuracy SCOR (= GRSCOR) synchronized to the PCM data to allow data linking along the time axis, thus greatly increasing the data linking accuracy.

§4-13-5. Data Processing

The CXD3048R accumulates PCM data from the CD-DSP block in an external buffer and then inputs the data to the DAC block in sync with the internally generated Fs system clock. At this time, the PCM data is loaded and read out at the same rate during normal playback, so data does not accumulate in the buffer RAM. Therefore, the loading rate must be increased. This is accomplished by setting the CD-DSP block to double-speed mode and doubling the loading rate until the RAM is full. When the RAM becomes full, data regeneration from the disc stops temporarily and the RAM data is read out to create an empty area, at which point loading is restarted. These operations are then repeated to effectively use the entire area inside the RAM.



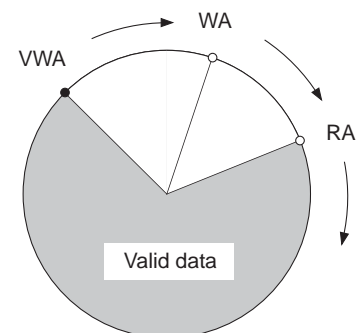
PCM Data Flow (Example for 4M × 1 mode)

§4-13-6. System Outline (when SLXQOK = 1 and SLXWRE = 1)

The addresses for accessing the buffer RAM data consist of a readout address (RA) and a write address (WA). The data to be written is not always correct, and the subcodes, etc. must be constantly checked to make sure the data is correct and there is no sound skipping. The CXD3048R checks subcode-Q using the CPU, and defines the data by inputting a negative pulse to the XQOK pin. This defined address (VWA) is loaded to the internal register and the data between VWA and RA is treated as valid data. WA advances at a speed twice that of RA, and RA is written by WA and read out sequentially in the order registered by VWA. When RA catches up to VWA, there is no more valid data and readout is prohibited (XEMP = low). In addition, when WA catches up to RA, the buffer is full and write is prohibited (XWIH = low). In this manner, write to the RAM is interrupted when the RAM becomes full and there is no write area or when sound skipping caused by scratches, external disturbances or other factors is detected. Data continuity must be ensured in order to restart write. Therefore, the CXD3048R returns to the last defined address, and the CPU accesses the defined address point it sent last (actually the data slightly before that point) and reads the subcode-Q after the rising edge of SCOR. If the subcode-Q matches the last defined address, XWRE is made to fall and write is restarted when GRSCOR comes high within 7ms.

Note 1) If XWRE is made to fall when GRSCOR is low, XWIH goes low and the write prohibited state results.

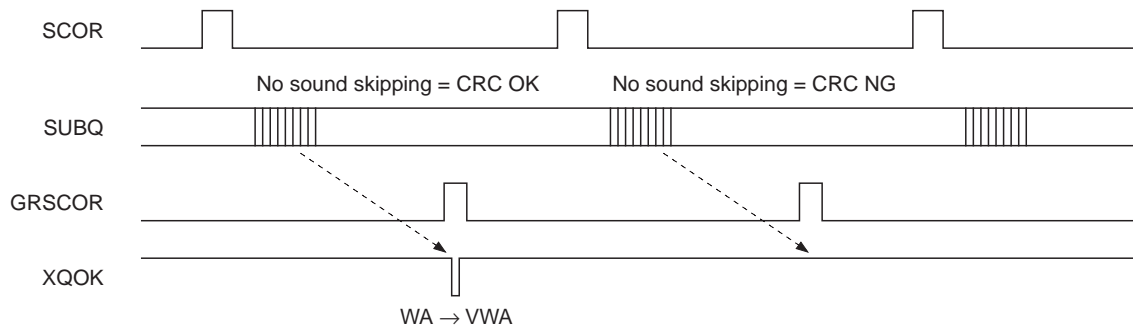
Note 2) When GRSCOR is low, VWA is not updated even if a negative pulse is input to XQOK. Therefore, set XQOK high while GRSCOR is low.



§4-13-7. Data Write (when SLXQOK = 1 and SLXWRE = 1)

The PCM data input from the DSP is loaded according to the Fs system clock inputs (BCKI, WDCI and LRCI), and is written sequentially to the external DRAM according to WA when the XWRE pin input goes low and internal write is enabled (XWIH pin output = high).

The written data must be checked by some means or other. The CXD3048R assumes data checking with subcode-Q. In this case, the CPU reads subcode-Q triggered by the SCOR signal output from the DSP to determine whether sound skipping occurred. If sound skipping is not detected, the CPU inputs a negative pulse to the XQOK pin during the GRSCOR high interval which comes within 7ms, and the data written to WA thus far is registered to VWA as data without sound skipping.



Write prohibition is determined by the internal status or by an external command. When prohibited by the internal status, the XWIH pin goes low, and this status is established when any one of the following conditions is met.

- | | |
|--|--|
| 1. There is no empty area in the DRAM. | XFUL = low |
| 2. The DSP RAM has overflowed. | ROF = high |
| 3. XWRE was made to fall when GRSCOR is low. | WRNG = high |
| 4. The DRAM write speed exceeds the set value. | SPOVER = high |
| | (when \$A7 command XWIH1 = 1) |
| 5. Access to DRAM in the shock-proof memory controller block failed. | NOWR = high |
| | (when \$A7 command XWIH2 = 1) |
| 6. The number of C2PO errors exceeds the set value. | monC2PO = high |
| | (\$AE command WTC C2PO = 1) |
| 7. Write is prohibited by the external input (A11 pin). | (when \$A7 command A11 SEL = 1 and \$AE command WTC C2PO = 1) |

When the XWIH pin goes low due to the above conditions, the CPU must set the XWRE pin high and then the XWIH pin high.

After the CPU sends XQOK, it must check whether XQOK was registered as a defined address. This is because if the above conditions arise at the same time XQOK is sent, XQOK becomes invalid and the addresses defined by the CPU and the CXD3048R may not match. Therefore, the XWIH pin output is used as the XQOK recognition signal (QRCVD) while XQOK is low. When QRCVD is high, this indicates that XQOK was correctly registered as a defined address (VWA was updated). When QRCVD is low, this indicates one of the following conditions.

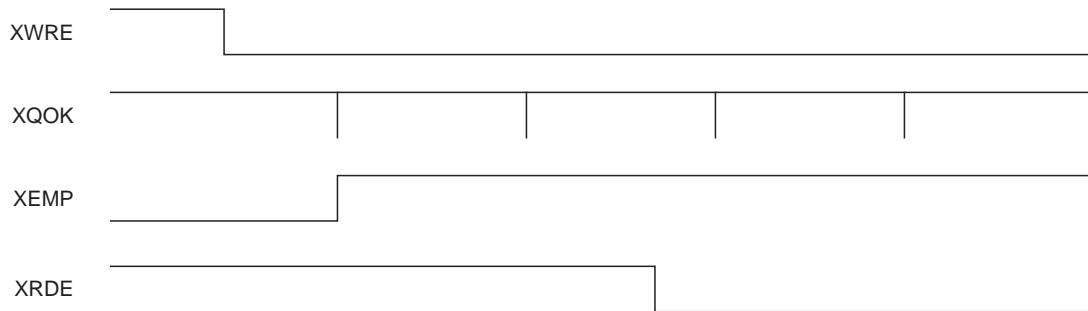
1. Write is prohibited due to the above conditions.
2. XWRE is high.

Regarding condition 2, if XQOK is sent while the XWRE pin is high, WA, VWA and RA are all reset (when GRSCOR is high).

§4-13-8. Data Readout (when SLXQOK = 1 and SLXWRE = 1)

When data write starts, there is no valid data in the RAM so the XEMP pin is low. The XWRE pin goes from high to low, and if there is no sound skipping or other problems with the CRC check at the next SCOR, XQOK is sent during the GRSCOR high interval which comes within 7ms, and the defined address and valid data are registered. At this point, the XEMP pin goes high for the first time and readout is enabled. Data readout follows RA, and is performed in sync with the internally generated Fs system clocks. The readout data and the Fs system clocks are output from the DATA and the BCK and LRCK pins, respectively.

RA is the address for reading out the written data that has been validated by VWA, and the area from VWA to RA is the amount of valid data ($|VWA - RA|$). The upper 5 bits are output as AM21 to AM17. When RA catches up to VWA and there is no more valid data ($|VWA - RA| = 0$), the XEMP pin goes low and readout is prohibited. When this state occurs, the CPU must set the XRDE pin high to prohibit readout. To restart readout, valid data must be registered as described above. The XEMP pin is held low until valid data is registered.



Note) After the XWRE pin goes from high to low, readout is enabled when valid data is registered by the first XQOK. However, ensuring some difference between VWA and RA is recommended in consideration of CRC NG, etc.

See also "Application Notes" for the control of the shock-proof memory controller block.

§4-14. CPU to DRAM Access Function

The CXD3048R can establish a special area in the DRAM. This allows a microcomputer to read and write optional 16-bit data to a portion of the DRAM area.

This function can be used to store and optionally read out demodulated CD TEXT data, etc.

The range of this special area is set by \$A7, and can be selected in 8 steps from 32K to 2M bits.

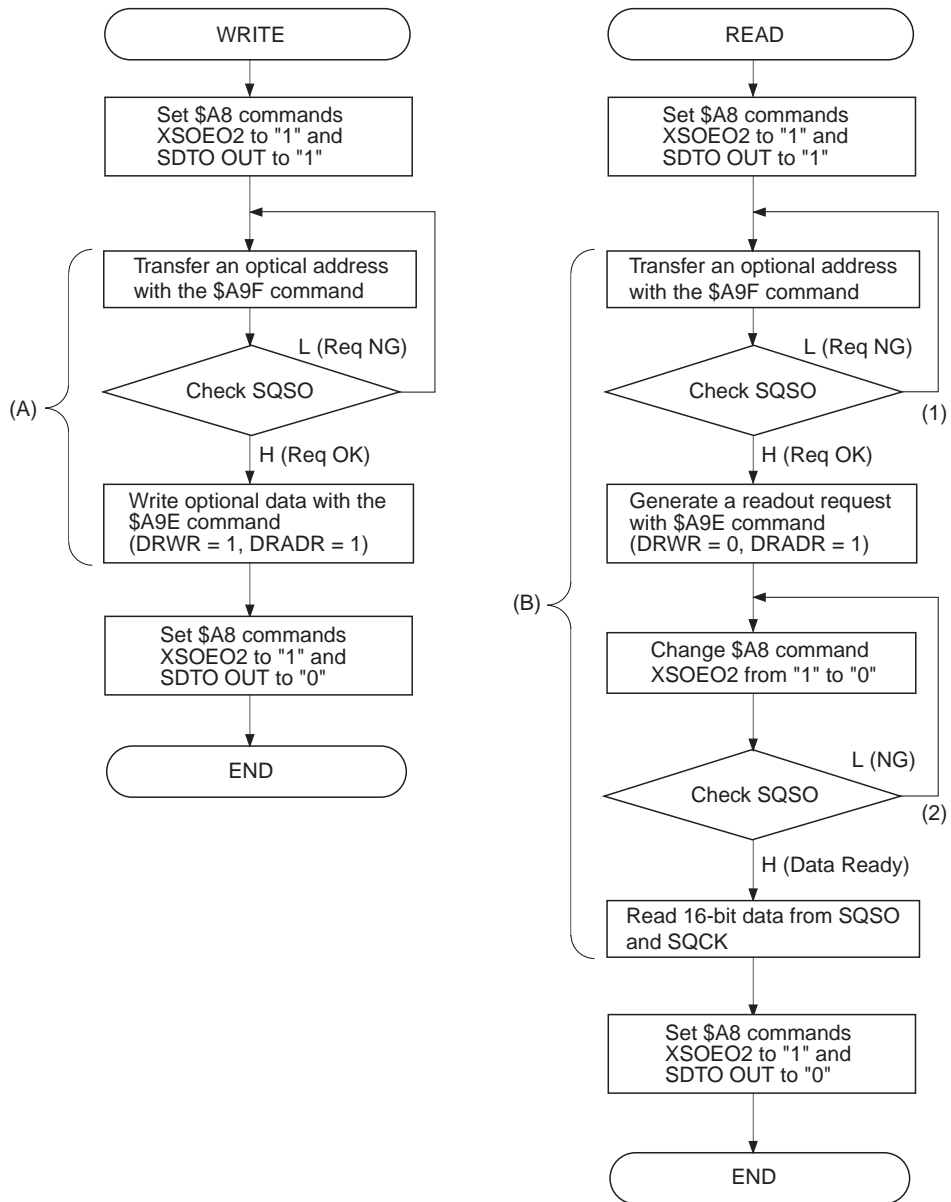
Table 4-19 shows the addresses which can be specified according to the used DRAM capacity and the special area setting value.

In addition, the address specification method can be selected from absolute and relative specification.

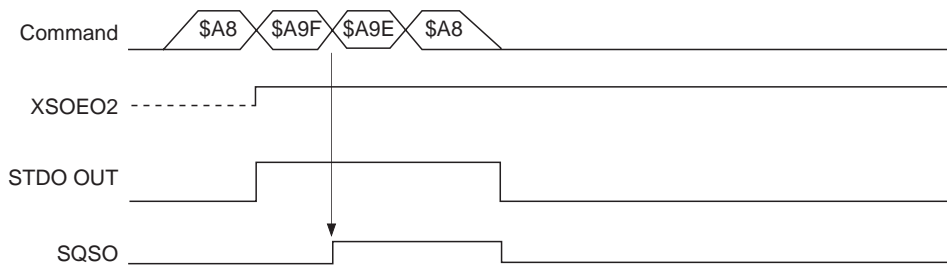
| | RSL 1 0 | MSL 2 1 0 | DRDR19 to DRDR0 specification range |
|-------------|------------|--------------|--|
| 4M setting | 0 0 | 0 0 0 | ----- |
| | | 0 0 1 | 00000 to 007FF |
| | | 0 1 0 | 00000 to 00FFF |
| | | 0 1 1 | 00000 to 01FFF |
| | | 1 0 0 | 00000 to 03FFF |
| | | 1 0 1 | 00000 to 07FFF |
| | | 1 1 0 | 00000 to 0FFFF |
| | | 1 1 1 | 00000 to 1FFFF |
| 16M setting | 1 1 | 0 0 0 | ----- |
| | | 0 0 1 | 00000 to 007FF |
| | | 0 1 0 | 00000 to 00FFF |
| | | 0 1 1 | 00000 to 01FFF |
| | | 1 0 0 | 00000 to 03FFF |
| | | 1 0 1 | 00000 to 07FFF |
| | | 1 1 0 | 00000 to 0FFFF |
| | | 1 1 1 | 00000 to 1FFFF |

Table 4-19.

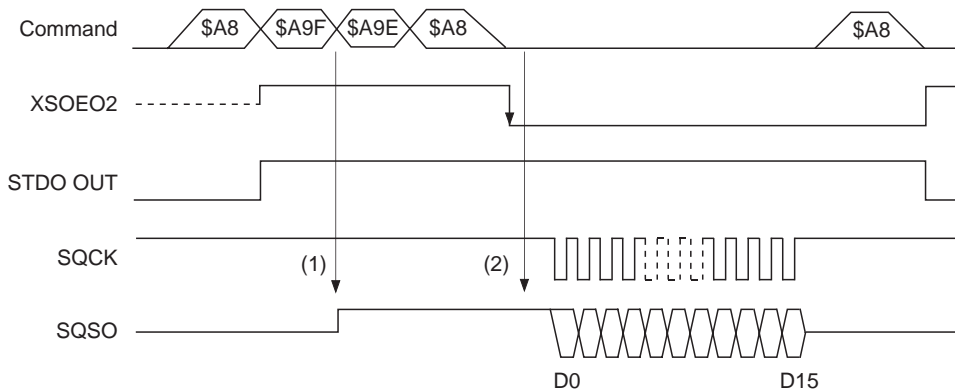
Write and Read by Absolute Address Specification



Write Communication Timing



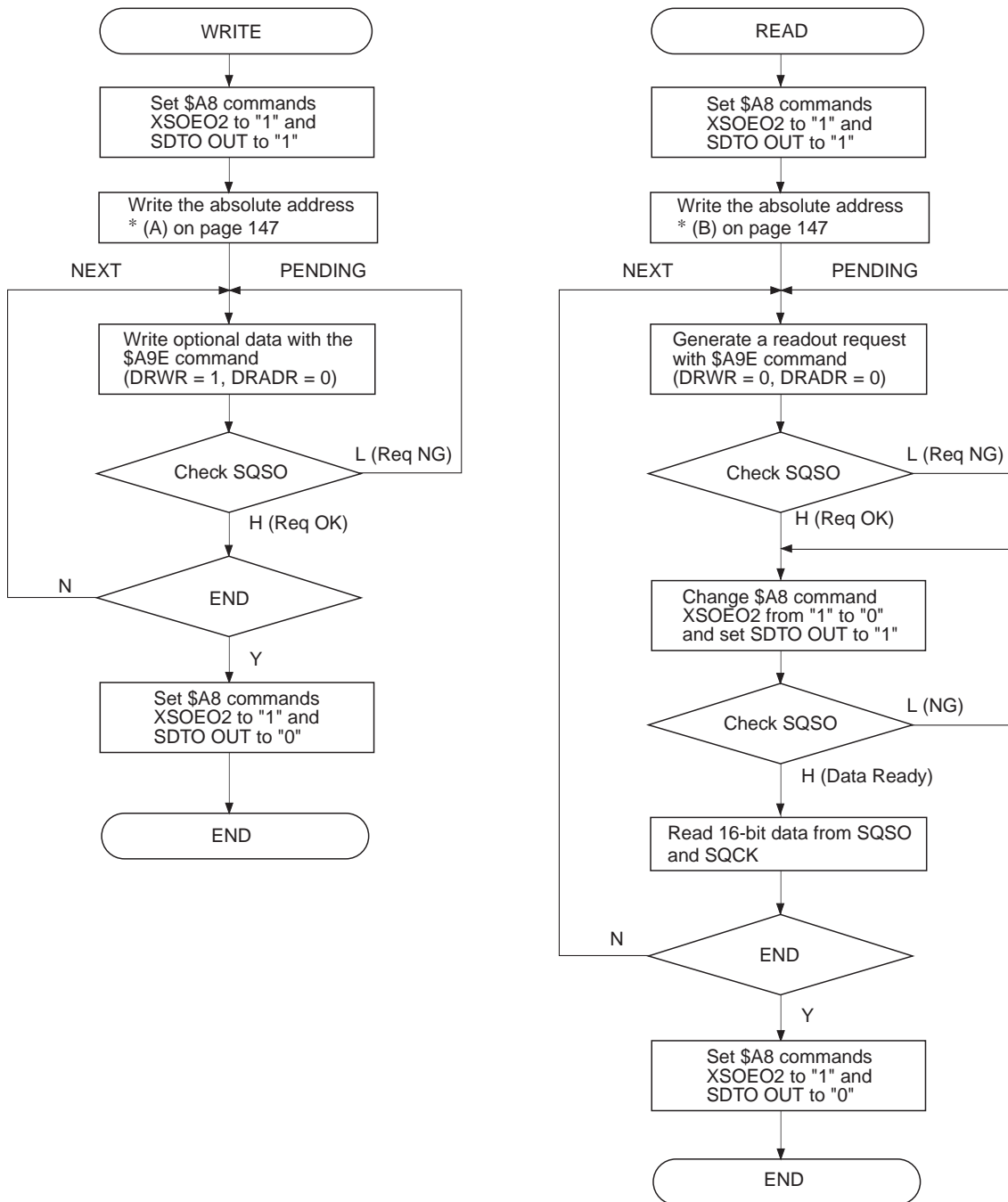
Readout Communication Timing



Readout Communication Operation

- (1) Set STDO OUT to "1" to switch the serial communication line for special memory.
- (2) Send the address command (\$A9F), then check whether the DRAM related processing has completed using the SQSO pin.
- (3) The data read out from the DRAM is loaded to the communication block inside the LSI by sending the read command (\$A9E) and causing XSOEO2 to fall (\$A8). However, the DRAM related processing requires a check as to whether the data was loaded properly using the SQSO pin.
- (4) The readout data is output from the SQSO pin by inputting 16 clocks from the SQCK pin.

Write and Read by Relative Address Specification



§4-15. Asymmetry Correction

Fig. 4-20 shows the block diagram and circuit example.

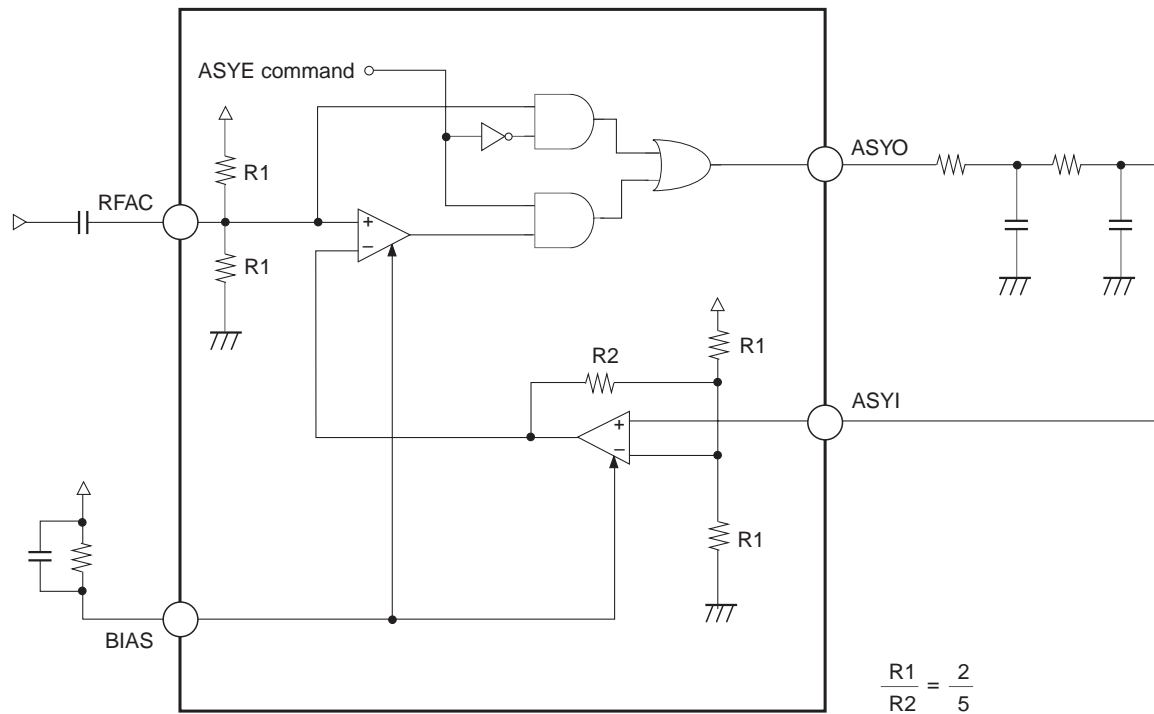


Fig. 4-20. Asymmetry Correction Application Circuit

§4-16. CD TEXT Data Demodulation

- In order to demodulate the CD TEXT data, set the command \$8 Data 6 D3 TXON to "1". While TXON is "1", the CD TEXT demodulation circuit occupies the EXCK and SBSO pins, so connect EXCK to low and do not use the data output from SBSO. Also, 26.7ms (max.) are required to demodulate the CD TEXT data correctly after TXON is set to "1".
- The CD TEXT data is output by switching the SQSO pin with the command. The CD TEXT data output is enabled by setting the command \$8 Data 6 D2 TXOUT to "1". To read data, the readout clock should be input to SQCK.
- The readable data are the CRC counting results for each pack and the CD TEXT data (16 bytes) except for CRC data.
- When the CD TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Data which can be stored in the LSI is 1 packet (4 packs).

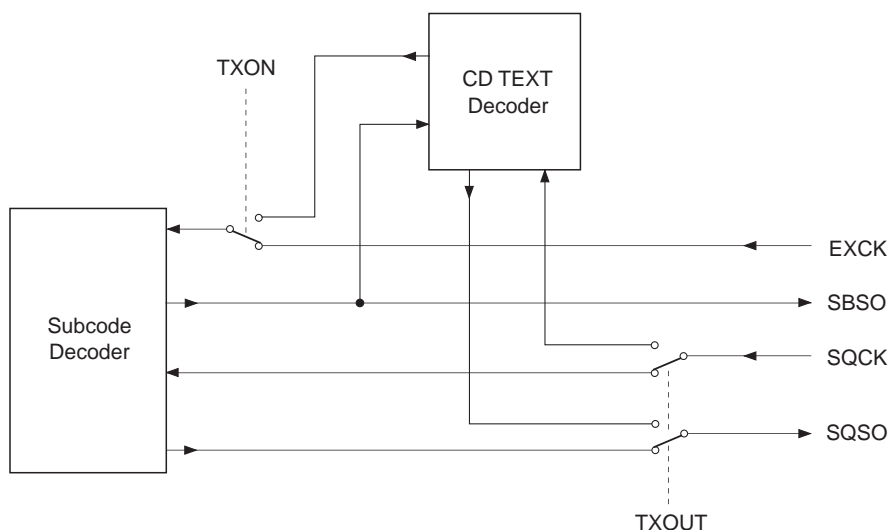


Fig. 4-21. Block Diagram of CD TEXT Demodulation Circuit

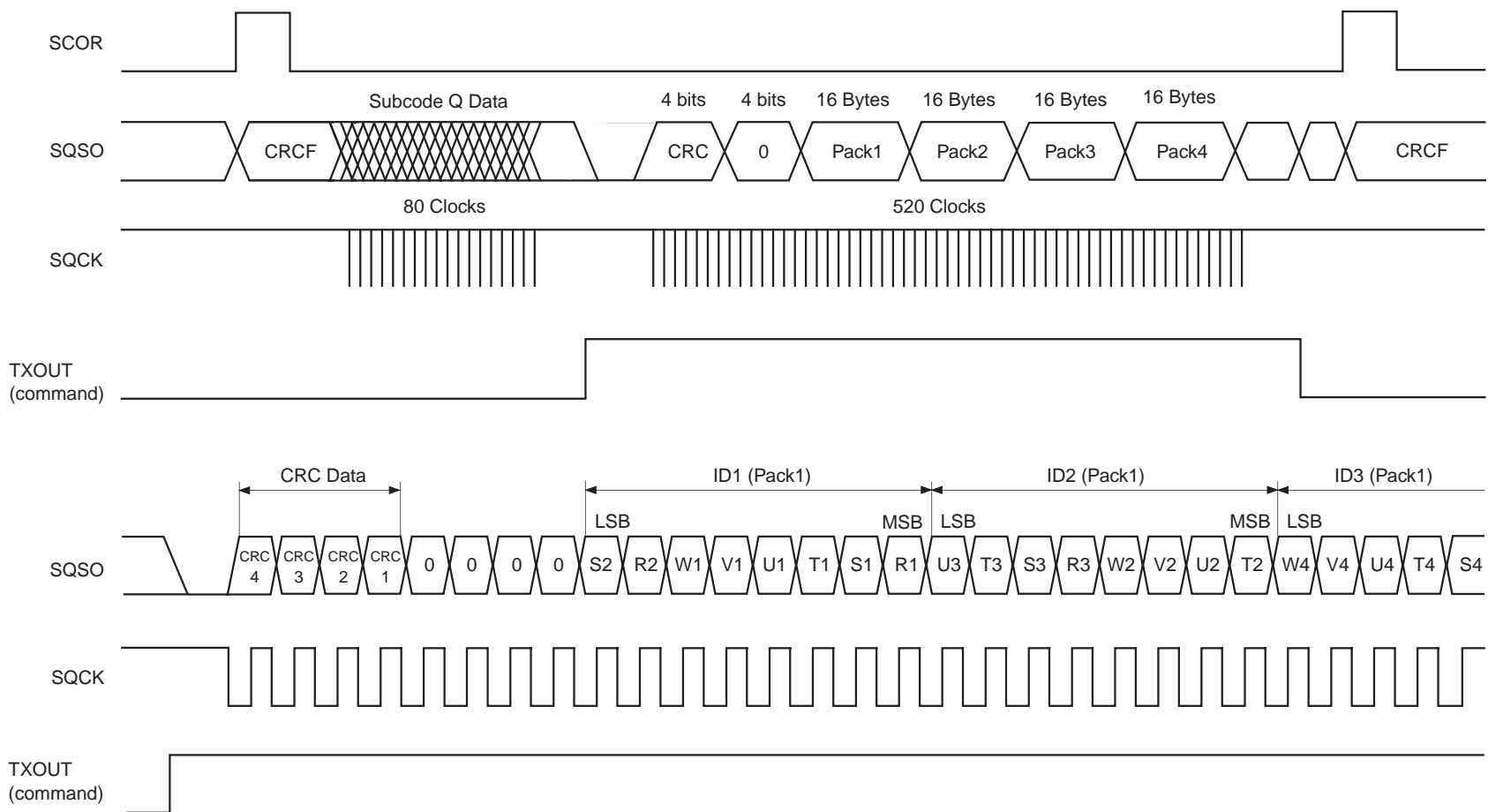


Fig. 4-22. CDTEXT Data Timing Chart

[5] Description of Servo Signal Processing System Functions and Commands

§5-1. General Description of Servo Signal Processing System (V_{DD} : Supply voltage)

Focus servo

| | |
|----------------|---|
| Sampling rate: | 88.2kHz (when MCK = 128Fs) |
| Input range: | $1/4V_{DD}$ to $3/4V_{DD}$ |
| Output format: | 7-bit PWM |
| Other: | Offset cancel Focus bias adjustment Focus search Gain-down Defect countermeasure Auto gain control |

Tracking servo

| | |
|----------------|--|
| Sampling rate: | 88.2kHz (when MCK = 128Fs) |
| Input range: | $1/4V_{DD}$ to $3/4V_{DD}$ |
| Output format: | 7-bit PWM |
| Other: | Offset cancel E:F balance adjustment Track jump Gain-up Defect countermeasure Drive cancel Auto gain control Vibration countermeasure |

Sled servo

| | |
|----------------|----------------------------|
| Sampling rate: | 345Hz (when MCK = 128Fs) |
| Input range: | $1/4V_{DD}$ to $3/4V_{DD}$ |
| Output format: | 7-bit PWM |
| Other: | Sled move |

FOK, MIRR, DFCT signal generation

| | |
|--------------------------|-------------------------------------|
| RF signal sampling rate: | 1.4MHz (when MCK = 128Fs) |
| Input range: | $1/4V_{DD}$ to $3/4V_{DD}$ |
| Other: | RF zero level automatic measurement |

§5-2. Digital Servo Block Master Clock (MCK)

The clock with 2/3 frequency of the crystal is supplied to the digital servo block.

XT4D and XT2D are \$3F commands, and XT1D is a \$3E command. (Default is "0" for each command)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

| Mode | XTAI | FSTO | XTSL | XT4D | XT2D | XT1D | Frequency division ratio | MCK |
|------|-------|-------|------|------|------|------|--------------------------|-------|
| 1 | 384Fs | 256Fs | — | — | — | 1 | 1 | 256Fs |
| 2 | 384Fs | 256Fs | — | — | 1 | 0 | 1/2 | 128Fs |
| 3 | 384Fs | 256Fs | 0 | 0 | 0 | 0 | 1/2 | 128Fs |
| 4 | 768Fs | 512Fs | — | — | — | 1 | 1 | 512Fs |
| 5 | 768Fs | 512Fs | — | — | 1 | 0 | 1/2 | 256Fs |
| 6 | 768Fs | 512Fs | — | 1 | 0 | 0 | 1/4 | 128Fs |
| 7 | 768Fs | 512Fs | 1 | 0 | 0 | 0 | 1/4 | 128Fs |

Fs = 44.1kHz, —: don't care

Table 5-1.

§5-3. DC Offset Cancel [AVRG (Average) Measurement and Compensation] (See Fig. 5-3.)

The CXD3048R can measure the averages of RFDC, VC, FE and TE and compensate these signals using the measurement results to control the servo effectively. This AVRG measurement and compensation is necessary to initialize the CXD3048R, and is able to cancel the DC offset.

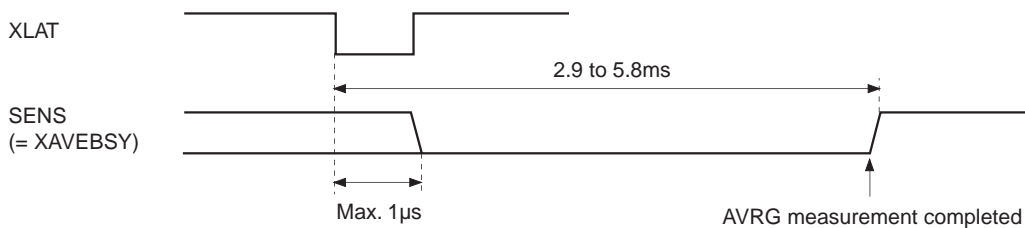
AVRG measurement takes the levels applied to the VC, FE, RFDC and TE pins as the digital average values of 256 samples, and then loads these values into each AVRG register.

The AVRG measurement commands are D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of \$38.

Measurement is on when the respective command is set to "1".

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received.

The completion of AVRG measurement operation can be monitored by the SENS pin. (See Timing Chart 5-2.) Monitoring requires that the upper 8 bits of the command register are 38 (h).



Timing Chart 5-2.

<Measurement>

VC AVRG: The VC DC offset (VC AVRG) which is the center voltage for the system is measured and used to compensate the FE, TE and SE signals.

FE AVRG: The FE DC offset (FE AVRG) is measured and used to compensate the FE and FZC signals.

TE AVRG: The TE DC offset (TE AVRG) is measured and used to compensate the TE and SE signals.

RF AVRG: The RF DC offset (RF AVRG) is measured and used to compensate the RFDC signal.

<Compensation>

- RFLC: (RF signal ÷ RF AVRG) is input to the RF In register.
"00" is input when the RF signal is lower than RF AVRG.
- TCL0: (TE signal ÷ VC AVRG) is input to the TRK In register.
- TCL1: (TE signal ÷ TE AVRG) is input to the TRK In register.
- VCLC: (FE signal ÷ VC AVRG) is input to the FCS In register.
- FLC1: (FE signal ÷ FE AVRG) is input to the FCS In register.
- FLC0: (FE signal ÷ FE AVRG) is input to the FZC register.

Two methods of canceling the DC offset are assumed for the CXD3048R. These methods are shown in Figs. 5-3a and 5-3b.

An example of AVRG measurement and compensation commands is shown below.

- \$38 08 00 (RF AVRG measurement)
- \$38 20 00 (FE AVRG measurement)
- \$38 00 10 (TE AVRG measurement)
- \$38 14 0A (Compensation on [RFLC, FLC0, FLC1, TLC1]; corresponds to Fig. 5-3a.)

See the description of \$38 for these commands.

§5-4. E:F Balance Adjustment Function (See Fig. 5-3.)

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS search, the traverse waveform appears in the TE signal due to disc eccentricity.

In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of \$38 to "1".

The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to "0".

Next, setting D2 (TLC2) of \$38 to "1" compensates the values obtained from the TE and SE input pins with the TRVSC register value (subtraction), allowing the E:F balance offset to be adjusted. (See Fig. 5-3.)

§5-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of \$3A to "1". (See Fig. 5-3.)

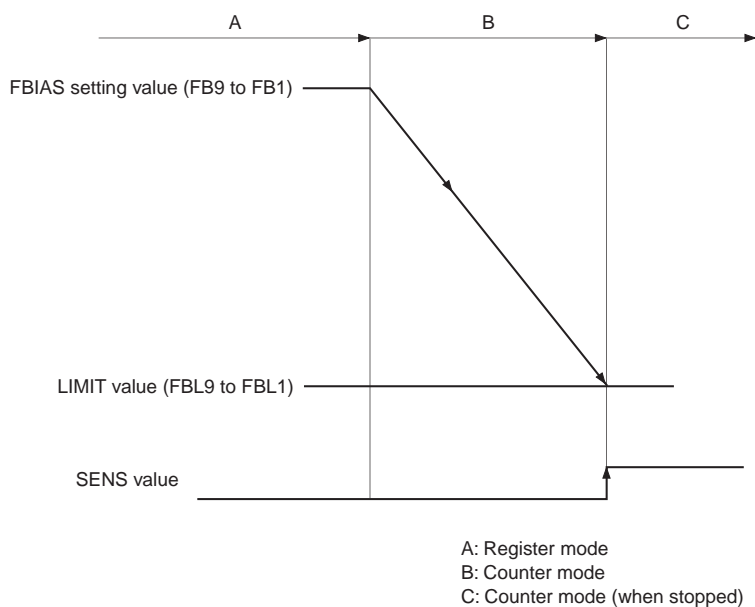
When D11 = 0 and D10 = 1 is set by \$34F, the FBIAS register value can be written using the 9-bit value of D9 to D1 (D9: MSB).

In addition, the RF jitter can be monitored by setting the \$8 command SOCT to "1". (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of \$3A to "1". The FBIAS register functions as an up counter when D12 (FBUP) of \$3A = 1, and as a down counter when D12 (FBUP) of \$3A = 0.

The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of \$3A.

When using the FBIAS register as a counter, the counter stops when the value set beforehand in FBL9 to FBL1 of \$34 matches the FCSBIAS value. Also, if the upper 8 bits of the command register are \$3A at this time, SENS goes high and the counter stop can be monitored.



Here, assume the FBIAS setting value FB9 to FB1 and the FBIAS LIMIT value FBL9 to FBL1 are set in status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the LIMIT value is reached and the FBIAS value matches FBL9 to FBL1, the counter stops and the SENS pin goes high. Note that the up/down counter counts at each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to $1/512 \times V_{DD}/2$.

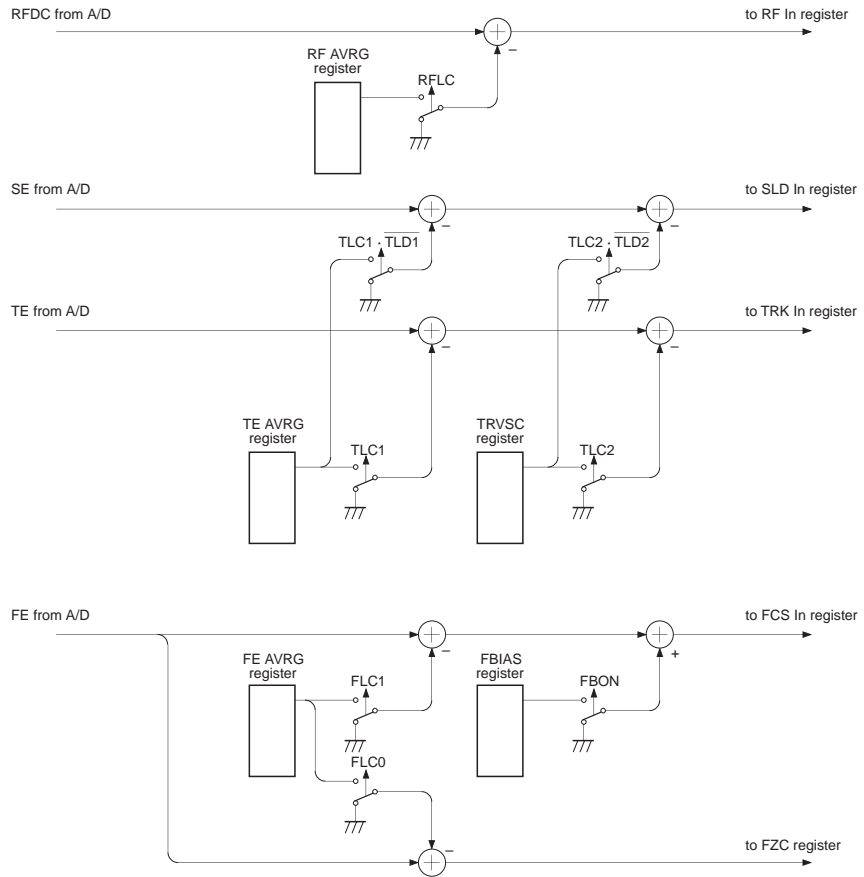


Fig. 5-3a.

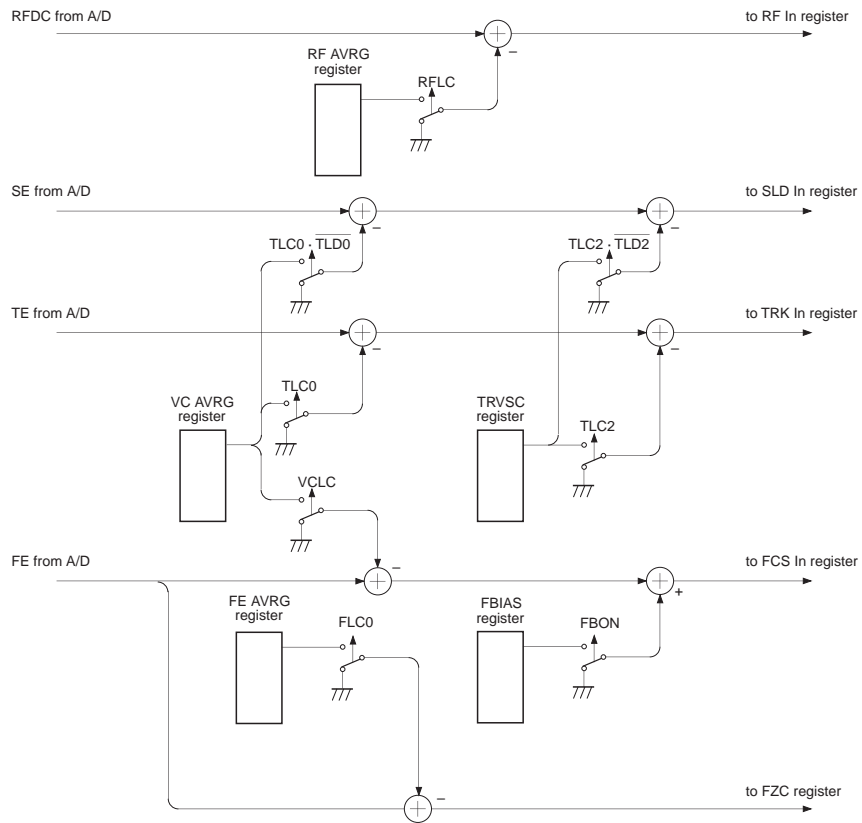


Fig. 5-3b.

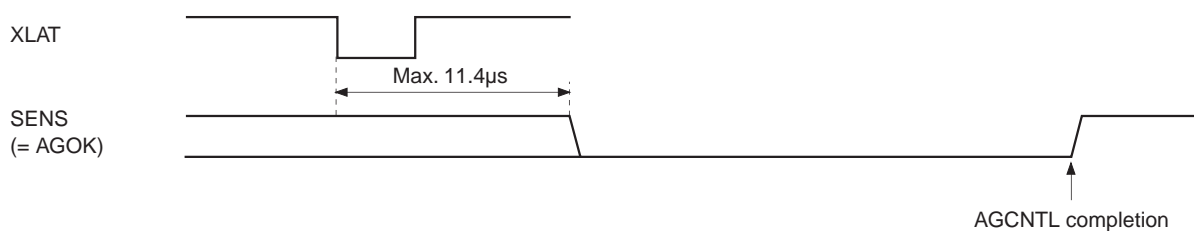
§5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate servo loop gain. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (h), the completion of AGCNTL operation can be confirmed by monitoring the SENS pin. (See Timing Chart 5-4 and "Description of SENS Signals".)

Setting D9 and D8 of \$38 to "1" sets FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 5-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (h), and they must also be set within this range when written externally.

After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with \$35, \$36 and \$37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (h)

TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (h)

AGS; Self-stop on/off

AGJ; Convergence completion judgment time

AGGF; Internally generated sine wave amplitude (AGF)

AGGT; Internally generated sine wave amplitude (AGT)

AGV1; AGCNTL sensitivity 1 (during rough adjustment)

AGV2; AGCNTL sensitivity 2 (during fine adjustment)

AGHS; Rough adjustment on/off

AGHT; Fine adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to FG0 and TG6 to TG0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL default operation has two stages.

In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.

In the second stage, the AGCNTL coefficient is finely adjusted with relatively low sensitivity to further approach the appropriate value. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD3048R confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self-stop mode) This self-stop mode can be canceled by setting AGS to "0".

In addition, the first stage is omitted for AGCNTL operation when AGHS is set to "0".

An example of AGCNTL coefficient transitions during AGCNTL operation with various settings is shown in Fig. 5-5.

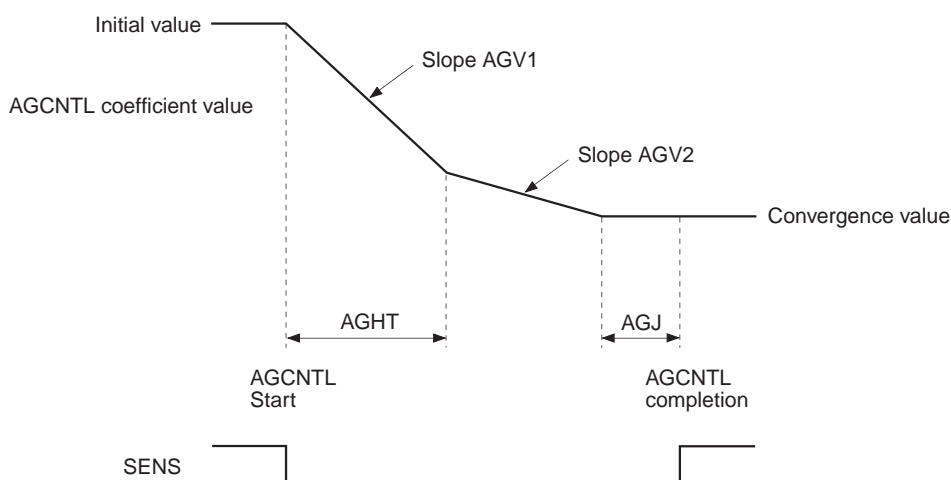


Fig. 5-5.

Note) Fig. 5-5 shows the case where the AGCNTL coefficient converges from the initial value to a smaller value.

§5-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command \$0X. (See Table 5-6.)

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------------|------------|------------|---|
| 0 | FOCUS CONTROL | 0 0 0 0 | 1 0 — — | FOCUS SERVO ON (FOCUS GAIN NORMAL) |
| | | | 1 1 — — | FOCUS SERVO ON (FOCUS GAIN DOWN) |
| | | | 0 — 0 — | FOCUS SERVO OFF, 0V OUT |
| | | | 0 — 0 — | FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT |
| | | | 0 — 0 0 | FOCUS SEARCH VOLTAGE DOWN |
| | | | 0 — 0 0 | FOCUS SEARCH VOLTAGE UP |

—: don't care

Table 5-6.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands \$00 → \$02 → \$03 and performing only FCS search operation. Fig. 5-8 shows the signals for sending \$08 (FCS on) after that.

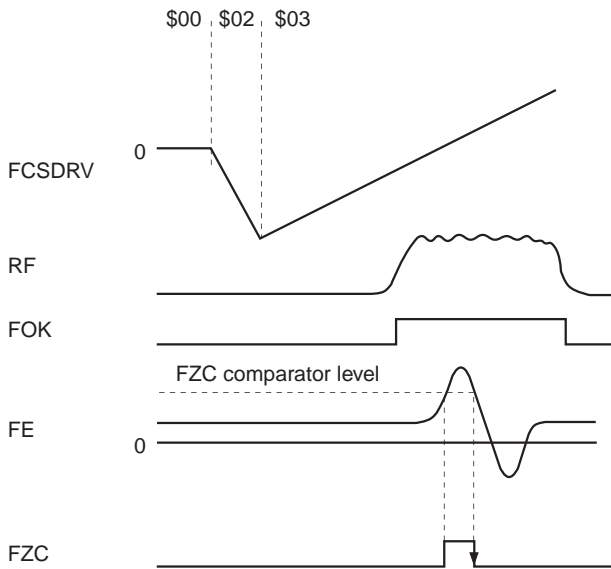


Fig. 5-7.

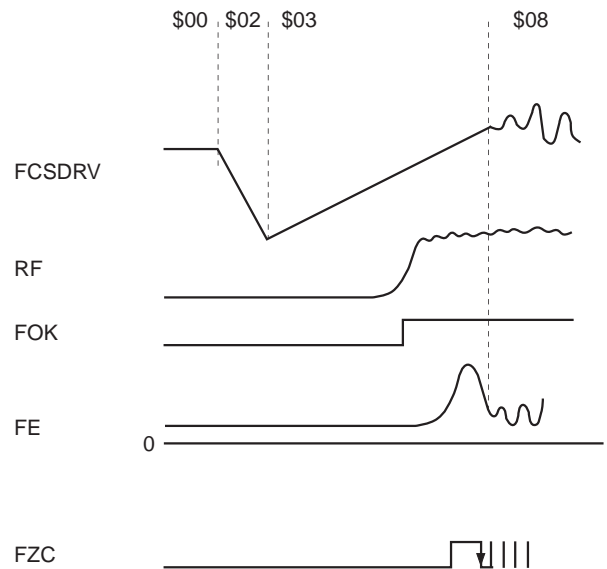


Fig. 5-8.

§5-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command \$2X. (See Table 5-9.)

When the upper 4 bits of the serial data are 2 (h), TZC is output to the SENS pin.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------------|------------|------------|--------------------|
| 2 | TRACKING MODE | 0 0 1 0 | 0 0 — — | TRACKING SERVO OFF |
| | | | 0 1 — — | TRACKING SERVO ON |
| | | | 1 0 — — | FORWARD TRACK JUMP |
| | | | 1 1 — — | REVERSE TRACK JUMP |
| | | | — — 0 0 | SLED SERVO OFF |
| | | | — — 0 1 | SLED SERVO ON |
| | | | — — 1 0 | FORWARD SLED MOVE |
| | | | — — 1 1 | REVERSE SLED MOVE |

—: don't care

Table 5-9.

TRK Servo

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of \$36.

In addition, when the TRK servo is on and D17 of \$1 is set to "1", the TRK servo filter switches to gain-up mode. The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.

The CXD3048R has 2 types of gain-up filter structures in TRK gain-up mode which can be selected by setting D16 of \$1. (See Table 5-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of \$37, is determined by multiplying this value by 1×, 2×, 3×, or 4× set using D17 and D16 when D18 = D19 = 0 is set with \$3. (See Table 5-10.)

SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off. These operations are disabled by setting D6 (LKSW) of \$38 to "1".

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------|------------|------------|------------------------------------|
| 3 | SELECT | 0 0 1 1 | 0 0 0 0 | SLED KICK LEVEL (basic value × ±1) |
| | | | 0 0 0 1 | SLED KICK LEVEL (basic value × ±2) |
| | | | 0 0 1 0 | SLED KICK LEVEL (basic value × ±3) |
| | | | 0 0 1 1 | SLED KICK LEVEL (basic value × ±4) |

Table 5-10.

§5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.

An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.

The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 5-11.)

The bottom hold speed and mirror sensitivity can be selected from four values using D7 and D6, and D5 and D4, respectively, of \$3C.

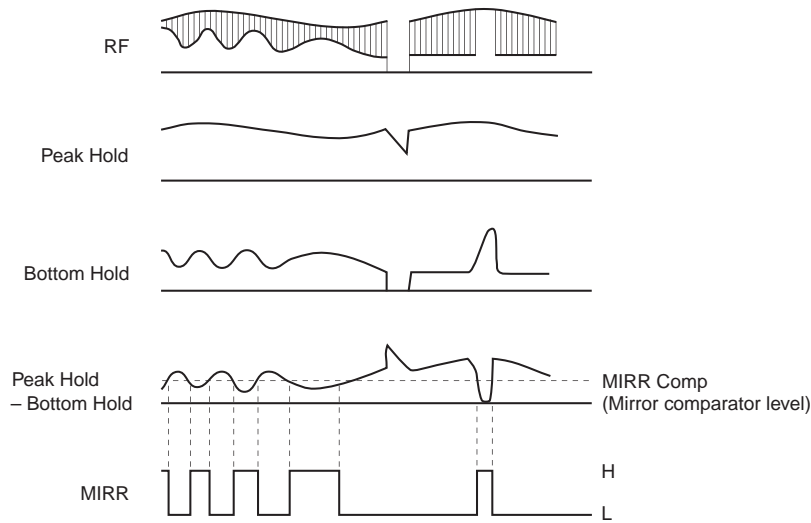


Fig. 5-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)

The DFCT comparator level can be selected from four values using D13 and D12 of \$3B.

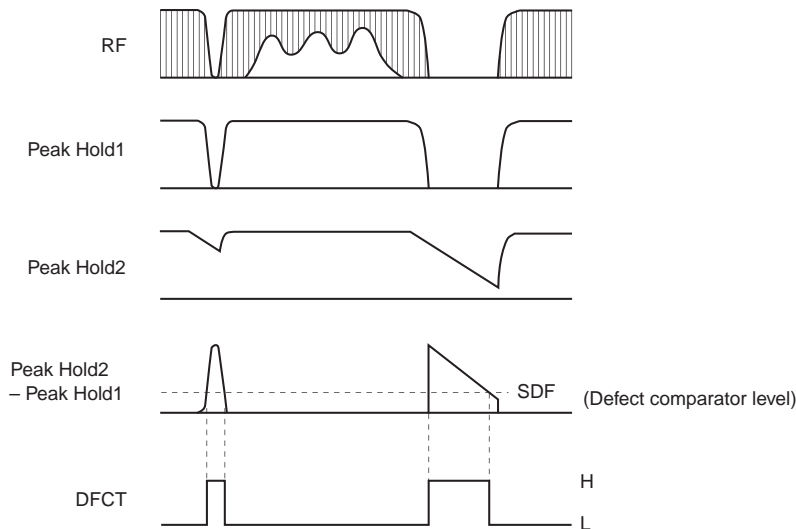


Fig. 5-12.

§5-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, this operation is achieved by detecting scratches and defects with the DFCT signal generation circuit, and when DFCT goes high, applying the low-frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of \$38 to "1".

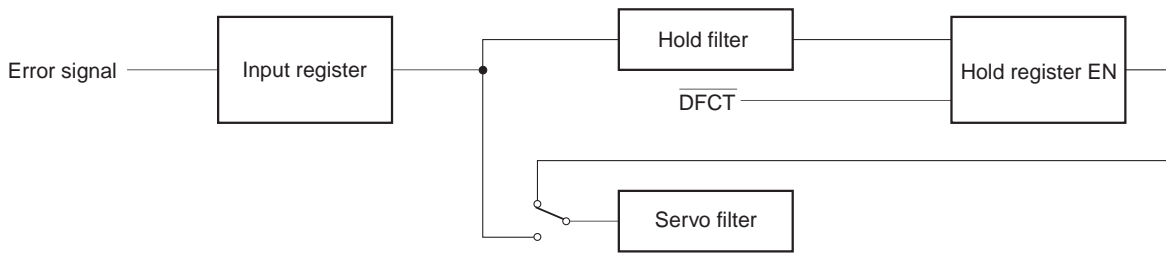


Fig. 5-13.

§5-11. Anti-shock Circuit

When vibrations occur in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures. Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of \$1 when the brake circuit (described hereafter) is off. (See Table 5-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 4 bits of the command register are 1 (h), vibration detection can be monitored from the SENS pin. It can also be monitored from the ATSK pin by setting \$3F command ASOT to "1".

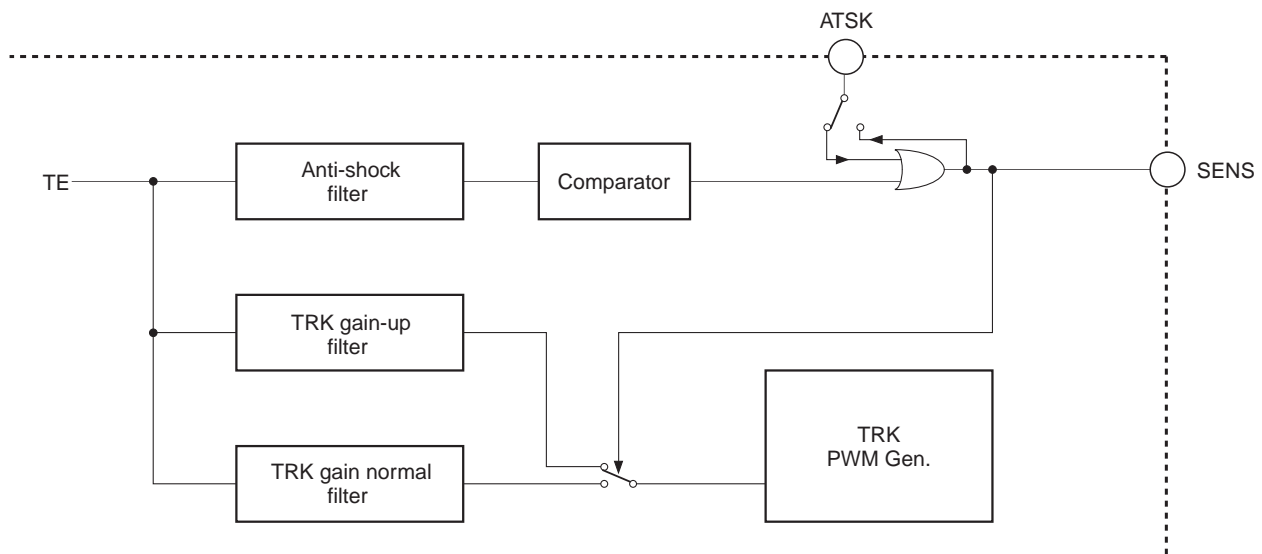


Fig. 5-14.

§5-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, the brake circuit uses the tracking drive as a brake by cutting the unnecessary portions utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of \$1. (See Table 5-17.)

In addition, the low frequency for the tracking drive after masking can be boosted. (SFBK1 and SFBK2 of \$34B)

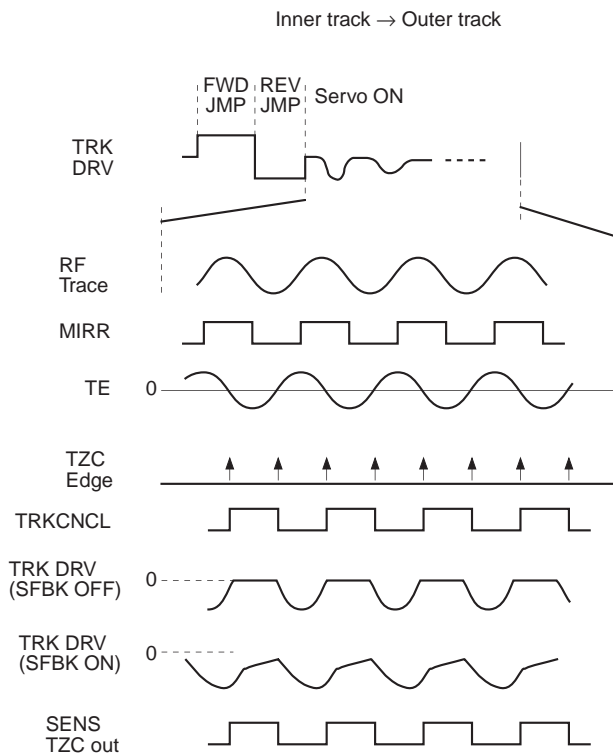


Fig. 5-15.

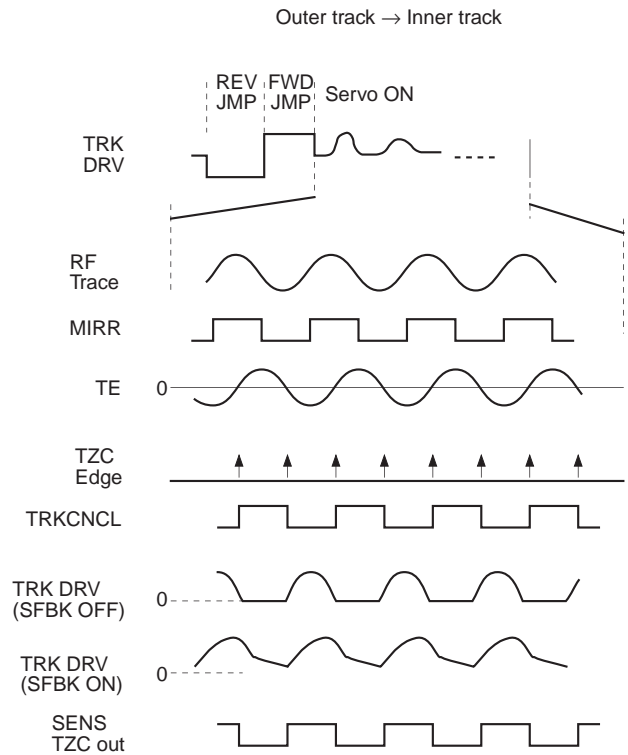


Fig. 5-16.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|------------------|------------|------------|----------------------------------|
| 1 | TRACKING CONTROL | 0 0 0 1 | 1 0 — — | ANTI SHOCK ON |
| | | | 0 — — — | ANTI SHOCK OFF |
| | | | — 1 — — | BRAKE ON |
| | | | — 0 — — | BRAKE OFF |
| | | | — — 0 — | TRACKING GAIN NORMAL |
| | | | — — 1 — | TRACKING GAIN UP |
| | | | — — — 1 | TRACKING GAIN UP FILTER SELECT 1 |
| | | | — — — 0 | TRACKING GAIN UP FILTER SELECT 2 |

—: don't care

Fig. 5-17.

§5-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. The used TZC signal can be selected from among three different phases according to the COUT signal application.

- HPTZC: For 1-track jumps
Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cut-off 1kHz digital HPF; when MCK = 128Fs.)
- STZC: For COUT generation when MIRR is externally input and for applications other than COUT generation.
This is generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
- DTZC: For high-speed traverse
Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.

The COUT signal output method is switched with D15 and D14 of \$3C.

- When D15 = 1: STZC
- When D15 = 0 and D14 = 0: HPTZC
- When D15 = 0 and D14 = 1: DTZC

When DTZC is selected, the delay can be selected from two values with D14 of \$36.

§5-14. Serial Readout Circuit

The measurement and adjustment results specified beforehand by serial command \$39 can be read out from the SENS pin by inputting the readout clock to the SCLK pin. (See Fig. 5-18, Table 5-19 and "Description of SENS Signals".)

Specified commands

See the table on page 180.

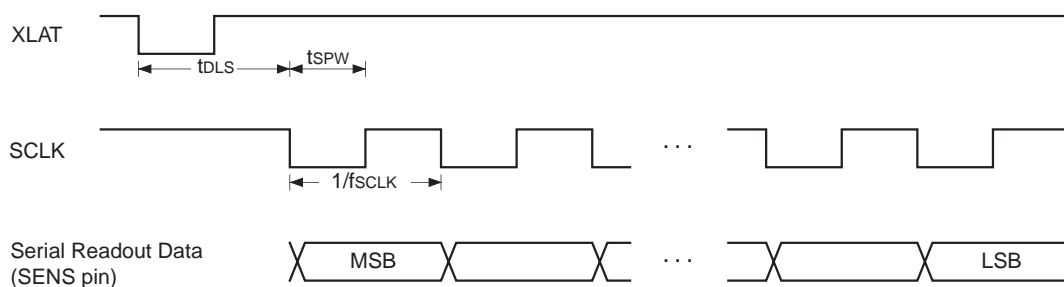


Fig. 5-18.

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------|--------|------|------|------|------|
| SCLK frequency | fSCLK | | | 16 | MHz |
| SCLK pulse width | tSPW | 31.3 | | | ns |
| Delay time | tDLS | 15 | | | µs |

Table 5-19.

During readout, the upper 8 bits of the command register must be 39 (h).

§5-15. Writing to Coefficient RAM

The coefficient RAM can be rewritten by \$34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

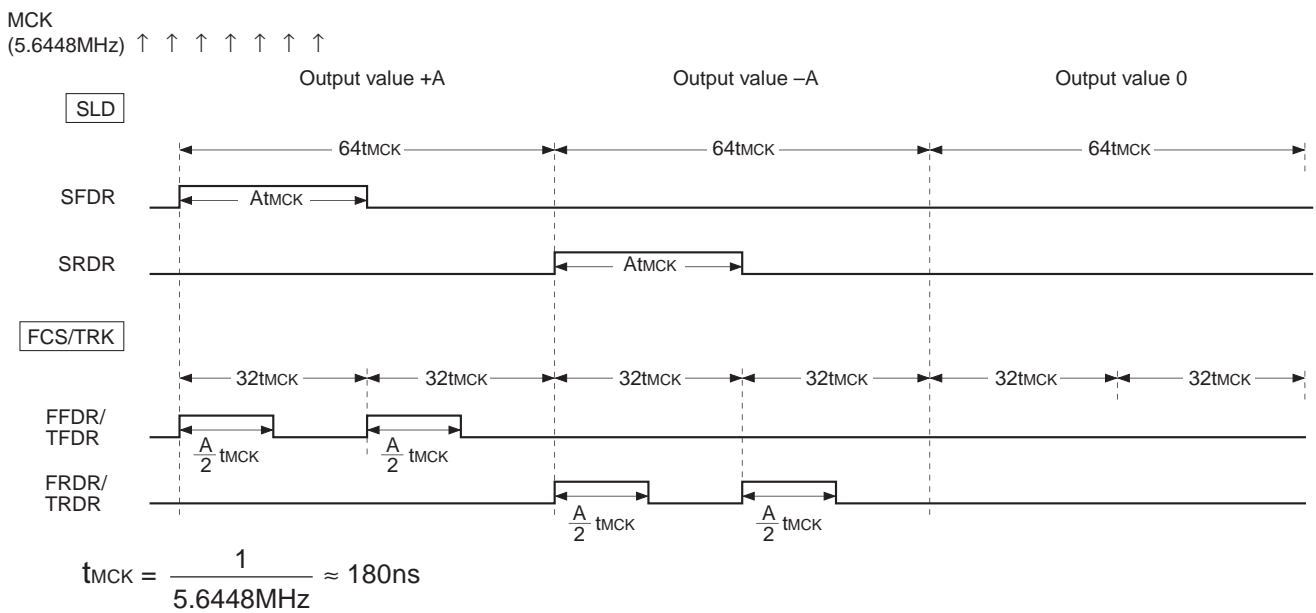
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of \$34 as the address (D15 = 0) and D7 to D0 as the data. Coefficient rewriting is completed 11.3µs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients continuously, be sure to wait 11.3µs (when MCK = 128Fs) before sending the next rewrite command.

§5-16. PWM Output

FCS, TRK and SLD PWM format outputs are described below.

In particular, FCS and TRK use a double oversampling noise shaper.

Timing Chart 5-20 and Fig. 5-21 show examples of output waveforms and drive circuits.



Timing Chart 5-20.

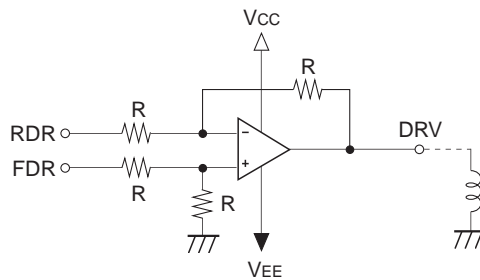


Fig. 5-21. Drive Circuit

§5-17. Servo Status Changes Produced by LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.

Setting D6 (LKSW) of \$38 to "1" deactivates this function.

In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low. This enables microcomputer control.

§5-18. Description of Commands and Data Sets

\$34

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | KA6 | KA5 | KA4 | KA3 | KA2 | KA1 | KA0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 |

When D15 = 0.

KA6 to KA0: Coefficient address

KD7 to KD0: Coefficient data

\$348 (preset: \$348 000)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-------|-------|-------|-------|----|----|----|-----|------|------|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | PGFS1 | PGFS0 | PFOK1 | PFOK0 | 0 | 0 | 0 | MRS | MRT1 | MRT0 | 0 | 0 |

These commands set the GFS signal hold time. The hold time is inversely proportional to the playback speed.

| PGFS1 | PGFS0 | Processing |
|-------|-------|--|
| 0 | 0 | High when the frame sync is at the correct timing, low when not the correct timing. |
| 0 | 1 | High when the frame sync is at the correct timing, low when continuously not the correct timing for 2ms or longer. |
| 1 | 0 | High when the frame sync is at the correct timing, low when continuously not the correct timing for 4ms or longer. |
| 1 | 1 | High when the frame sync is at the correct timing, low when continuously not the correct timing for 8ms or longer. |

These commands set the FOK signal hold time. See \$3B for the FOK slice level.

These are the values when MCK = 128Fs, and the hold time is inversely proportional to the MCK setting.

| PFOK1 | PFOK0 | Processing |
|-------|-------|--|
| 0 | 0 | High when the RFDC value is higher than the FOK slice level, low when lower than the FOK slice level. |
| 0 | 1 | High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 4.35ms or more. |
| 1 | 0 | High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 10.16ms or more. |
| 1 | 1 | High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 21.77ms or more. |

MRS: This command switches the time constant for generating the MIRR comparator level of the MIRR generation circuit.

When "0", the time constant is normal. (default)

When "1", the time constant is longer than normal.

The time during which MIRR = high due to the effects of RFDC signal pulse noise, etc., can be suppressed by setting MRS = 1.

MRT1, MRT0: These commands limit the time while MIRR = high.

| MRT1 | MRT0 | MIRR maximum time [ms] |
|------|------|------------------------|
| 0 | 0 | No time limit |
| 0 | 1 | 1.10 |
| 1 | 0 | 2.20 |
| 1 | 1 | 4.00 |

∗: preset

\$34A (preset: \$34A 150)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|---------|---------|--------|--------|----------|-----------|----------|--------|----------|----|----|----|
| 1 | 0 | 1 | 0 | A/D SEL | COPY EN | EMPH D | CAT b8 | DOUT EN1 | DOUT DMUT | DOUT WOD | WIN EN | DOUT EN2 | 0 | 0 | 0 |

| Command bit | Processing |
|-------------|--|
| A/DSEL = 0 | Bit 1 of the channel status data is output as audio data. |
| A/DSEL = 1 | Bit 1 of the channel status data is output as other than audio data. |

| Command bit | Processing |
|-------------|--|
| COPY EN = 0 | Bit 2 of the channel status data is output as digital copy prohibited. |
| COPY EN = 1 | Bit 2 of the channel status data is output as digital copy enabled. |

| Command bit | Processing |
|-------------|---|
| EMPH D = 0 | Bit 3 of the channel status data is output as without pre-emphasis. |
| EMPH D = 1 | Bit 3 of the channel status data is output as with pre-emphasis. |

| Command bit | Processing |
|-------------|--|
| CAT b8 = 0 | Bit 8 of the channel status data is output as "0". |
| CAT b8 = 1 | Bit 8 of the channel status data is output as "1". |

| Command bit | Processing |
|--------------|---|
| DOUT EN1 = 0 | The DOUT signal, generated from the PCM data read out from the disc, is output. |
| DOUT EN1 = 1 | The DOUT signal, generated from the DA interface input, is output. |

\$34A commands cont.

| Command bit | Processing |
|---------------|---|
| DOUT DMUT = 0 | Digital Out output is normally output. |
| DOUT DMUT = 1 | All the audio data portions are output in zero, with Digital Out output as it is. |

| Command bit | Processing |
|--------------|-----------------------------------|
| DOUT WOD = 0 | The DOUT sync window is not open. |
| DOUT WOD = 1 | The DOUT sync window is open. |

| Command bit | Processing |
|-------------|--|
| WIN EN = 0 | Automatic synchronization to the input LRCK to match the phase with the internal processing is disabled. |
| WIN EN = 1 | Automatic synchronization to the input LRCK to match the phase with the internal processing is disabled. |

| Command bit | Processing |
|--------------|---|
| DOUT EN2 = 0 | Set to "0" when not generating Digital Out from the DA interface input. |
| DOUT EN2 = 1 | Set to "1" when generating Digital Out from the DA interface input. |

| DOUT EN1 | DOUT DMUT | \$B MD2 | Other mute conditions | DOUT Mute | DOUT Mute F | DOUT output |
|----------|-----------|---------|-----------------------|-----------|-------------|--|
| 0 | — | 0 | — | — | — | OFF |
| 0 | — | 1 | 0 | 0 | 0 | 0dB The output from the PCM data read out from a disc. |
| 0 | — | 1 | 0 | 0 | 1 | |
| 0 | — | 1 | 0 | 1 | 0 | -∞dB The output from the PCM data read out from a disc. |
| 0 | — | 1 | 0 | 1 | 1 | |
| 0 | — | 1 | 1 | 0 | 0 | |
| 0 | — | 1 | 1 | 0 | 1 | |
| 0 | — | 1 | 1 | 1 | 0 | |
| 0 | — | 1 | 1 | 1 | 1 | |
| 1 | 0 | — | — | — | — | 0dB The output from the DA interface input. |
| 1 | 1 | — | — | — | — | -∞dB The output from the DA interface input. |

—: don't care

* See "Mute conditions" (1) and (3) to (5) of \$AX commands for the other mute conditions.

* See \$8 commands for DOUT Mute and DOUT Mute F.

\$34B (preset: \$34B 000)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-------|-------|----|----|-------|-------|-------|----|----|----|----|----|
| 1 | 0 | 1 | 1 | SFBK1 | SFBK2 | 0 | 0 | LB1SN | LB2SN | LB2SM | 0 | 0 | 0 | 0 | 0 |

The low frequency can be boosted for brake operation.
See §5-12 for brake operation.

SFBK1: When "1", brake operation is performed by setting the LowBooster-1 input to "0".

This is valid only when TLB1ON = 1. Preset is "0".

SFBK2: When "1", brake operation is performed by setting the LowBooster-2 input to "0".

This is valid only when TLB2ON = 1. Preset is "0".

See the \$34C command booster setting for LB1SN, LB2SN and LB2SM.

\$34C (preset: \$34C 000)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-------|-------|--------|--------|--------|----|-------|-------|-------|-------|-------|-------|
| 1 | 1 | 0 | 0 | THBON | FHBON | TLB1ON | FLB1ON | TLB2ON | 0 | HBST1 | HBST0 | LB1S1 | LB1S0 | LB2S1 | LB2S0 |

These bits turn on the boost function. (See §5-20. Filter Composition.)

There are five boosters (three for the TRK filter and two for the FCS filter) which can be turned on and off independently.

THBON: When "1", the high frequency is boosted for the TRK filter. Preset is "0".

FHBON: When "1", the high frequency is boosted for the FCS filter. Preset is "0".

TLB1ON: When "1", the low frequency is boosted for the TRK filter. Preset is "0".

FLB1ON: When "1", the low frequency is boosted for the FCS filter. Preset is "0".

TLB2ON: When "1", the low frequency is boosted for the TRK filter. Preset is "0".

The difference between TLB1ON and TLB2ON is the position where the low frequency is boosted.

For TLB1ON, the low frequency is boosted before the TRK jump, and for TLB2ON, after the TRK jump.

The following commands set the boosters. (See §5-20. Filter Composition.)

HBST1, HBST0: TRK and FCS HighBooster setting.

HighBooster has the configuration shown in Fig. 5-22a, and can select three different combinations of coefficients BK1, BK2 and BK3. (See Table 5-23a.)

An example of characteristics is shown in Fig. 5-24a.

These characteristics are the same for both the TRK and FCS filters.

The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB1S1, LB1S0, LB1SN:

TRK and FCS LowBooster-1 setting.

LowBooster-1 has the configuration shown in Fig. 5-22b, and can select six different combinations of coefficients BK4, BK5 and BK6. (See Table 5-23b.)

An example of characteristics is shown in Fig. 5-24b.

These characteristics are the same for both the TRK and FCS filters.

The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB2S1, LB2S0, LB2SN, LB2SM:

TRK LowBooster-2 setting.

LowBooster-2 has the configuration shown in Fig. 5-22c, and can select six different combinations of coefficients BK7, BK8 and BK9. (See Table 5-23c.)

An example of characteristics is shown in Fig. 5-24c.

This booster is used exclusively for the TRK filter.

The sampling frequency is 88.2kHz (when MCK = 128Fs).

Note) Fs = 44.1kHz

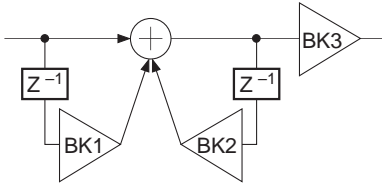


Fig. 5-22a.

| HBST1 | HBST0 | HighBooster setting | | |
|-------|-------|---------------------|---------|-----|
| | | BK1 | BK2 | BK3 |
| 0 | — | -120/128 | 96/128 | 2 |
| 1 | 0 | -124/128 | 112/128 | 2 |
| 1 | 1 | -126/128 | 120/128 | 2 |

Table. 5-23a.

—: don't care

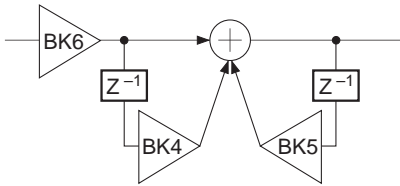


Fig. 5-22b.

| LB1S1 | LB1S0 | LB1SN | LowBooster-1 setting | | | Characteristic diagram*1 |
|-------|-------|-------|----------------------|-----------|-----|--------------------------|
| | | | BK4 | BK5 | BK6 | |
| 0 | — | 0 | -255/256 | 1023/1024 | 1/4 | ① |
| 1 | 0 | 0 | -511/512 | 2047/2048 | 1/4 | ② |
| 1 | 1 | 0 | -1023/1024 | 4095/4096 | 1/4 | ③ |
| 0 | — | 1 | -127/128 | 255/256 | 1 | ④ |
| 1 | 0 | 1 | -255/256 | 511/512 | 1 | ⑤ |
| 1 | 1 | 1 | -511/512 | 1023/1024 | 1 | ⑥ |

Table. 5-23b.

—: don't care

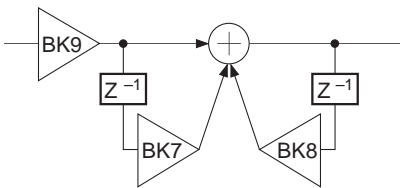


Fig. 5-22c.

| LB2S1 | LB2S0 | LB2SN | LB2SM | LowBooster-2 setting | | | Characteristic diagram*1 |
|-------|-------|-------|-------|----------------------|-----------|-----|--------------------------|
| | | | | BK7 | BK8 | BK9 | |
| 0 | — | 0 | 0 | -255/256 | 1023/1024 | 1/4 | ① |
| 1 | 0 | 0 | 0 | -511/512 | 2047/2048 | 1/4 | ② |
| 1 | 1 | 0 | 0 | -1023/1024 | 4095/4096 | 1/4 | ③ |
| 0 | — | 1 | 0 | -31/32 | 127/128 | 1 | ④ |
| 1 | 0 | 1 | 0 | -63/64 | 255/256 | 1 | ⑤ |
| 1 | 1 | 1 | 0 | -127/128 | 511/512 | 1 | ⑥ |
| 0 | — | 0 | 1 | -255/256 | 1023/1024 | 1 | ⑦ |
| 1 | 0 | 0 | 1 | -511/512 | 2047/2048 | 1 | ⑧ |
| 1 | 1 | 0 | 1 | -1023/1024 | 4095/4096 | 1 | ⑨ |

Table. 5-23c.

—: don't care

*1 ① to ⑥ correspond to ① to ⑥ in Fig. 5-23b respectively.

*2 ① to ⑨ correspond to ① to ⑨ in Fig. 5-23c respectively.

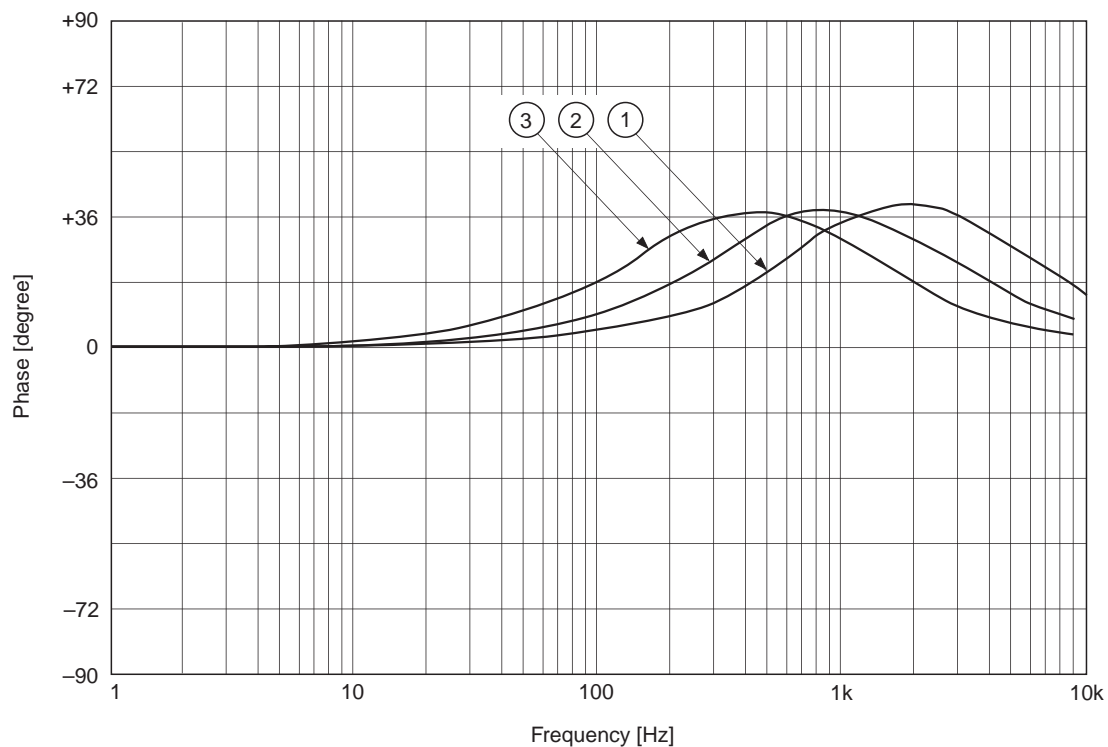
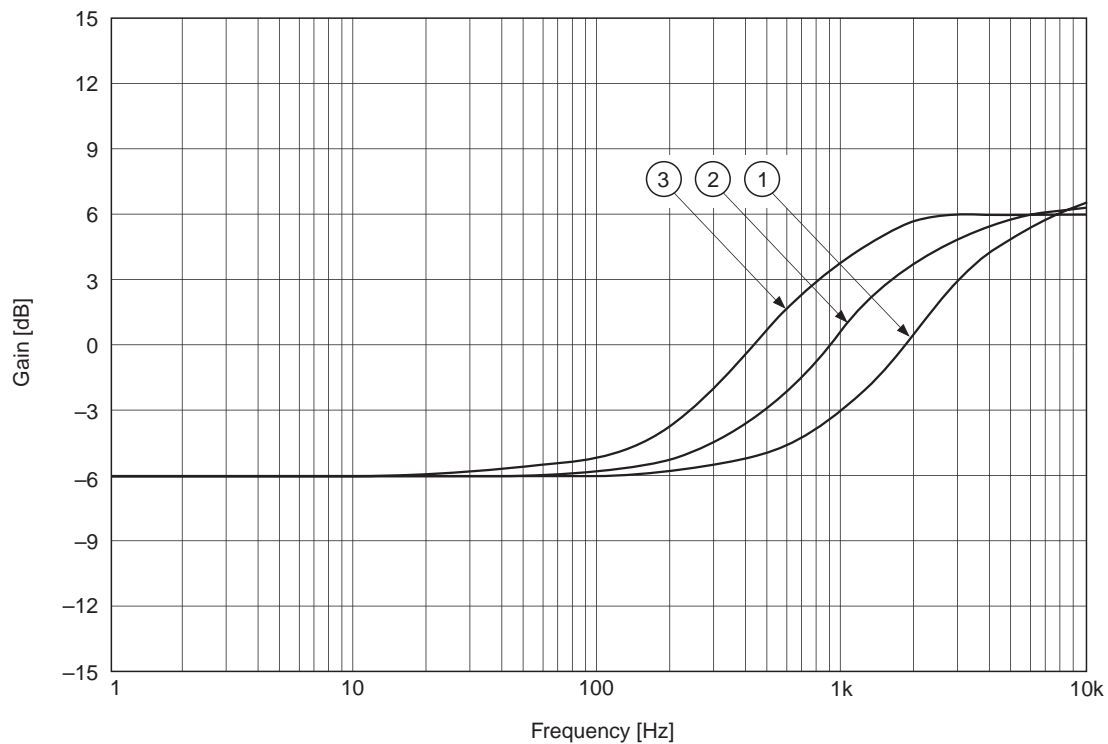


Fig. 5-24a. Servo HighBooster characteristics [FCS, TRK] (MCK = 128Fs)

- ① HBST1 = 0
- ② HBST1 = 1, HBST0 = 0
- ③ HBST1 = 1, HBST0 = 1

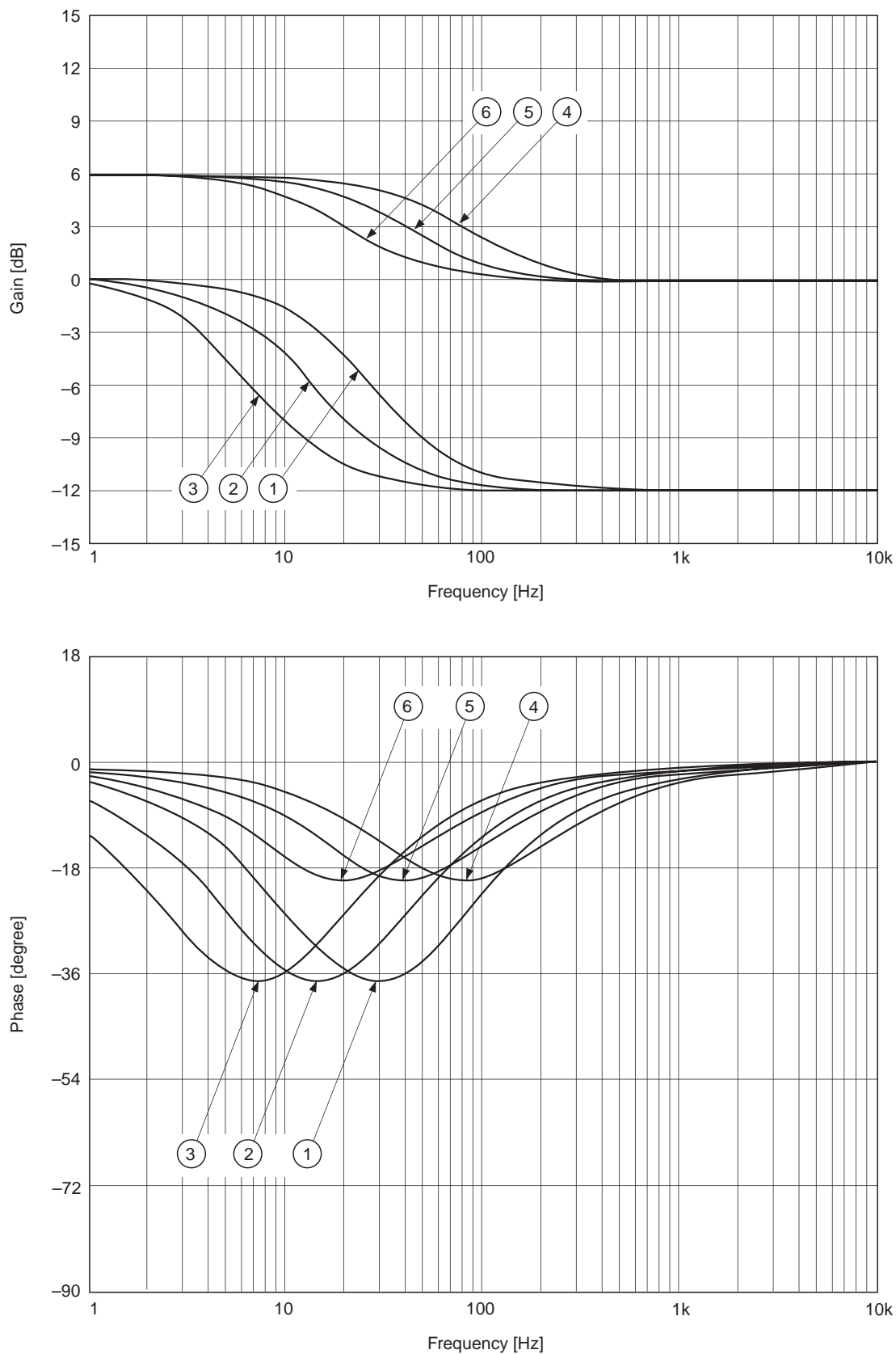


Fig. 5-24b. Servo LowBooster-1 characteristics [FCS, TRK] (MCK = 128Fs)

(① to ⑥ correspond to ① to ⑥ in Table 5-23b respectively.)

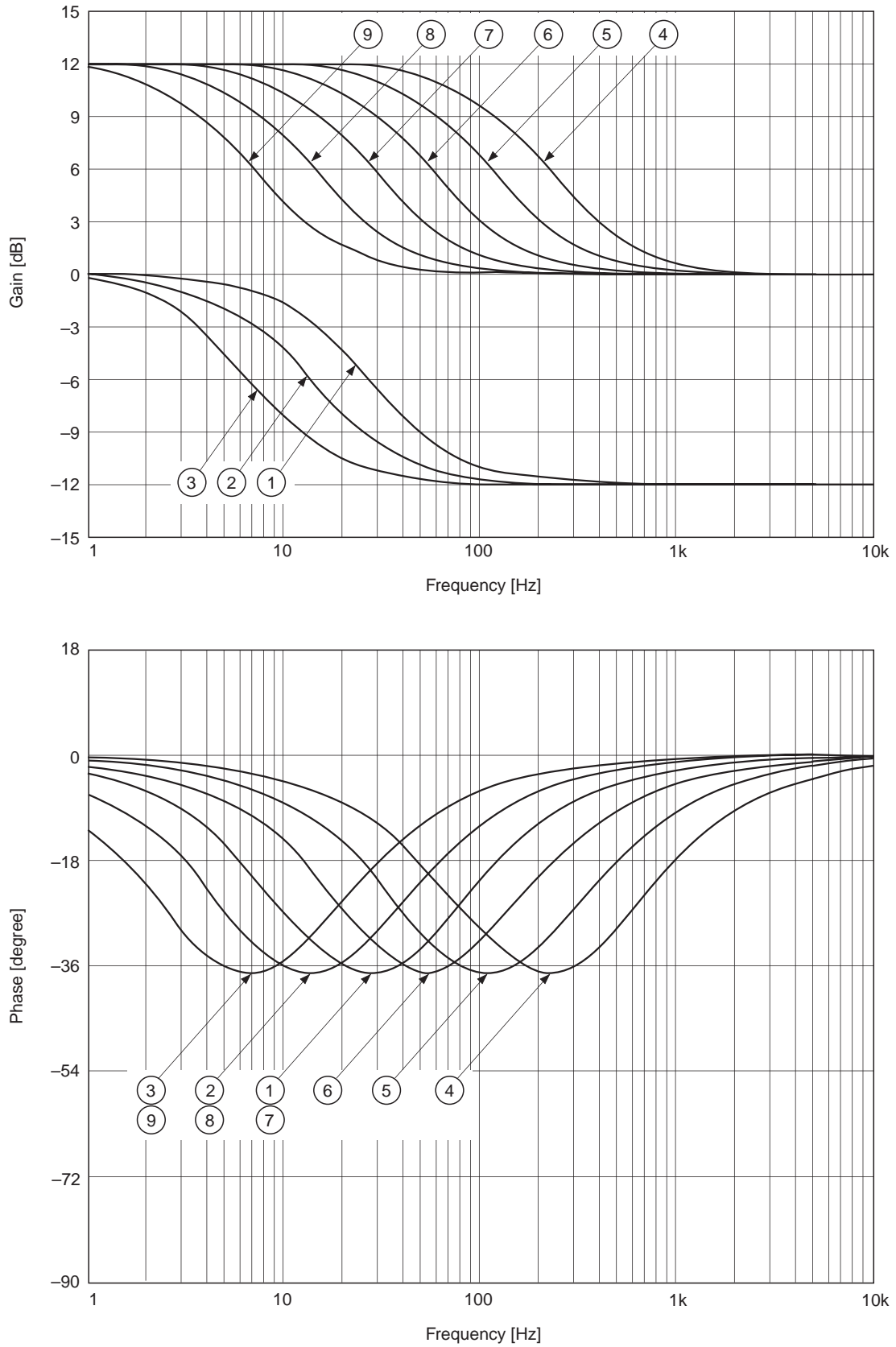


Fig. 5-24c. Servo LowBooster-2 characteristics [TRK] (MCK = 128Fs)

((① to ⑨ correspond to ① to ⑨ in Table 5-23c respectively.)

\$34E (preset: \$34E000)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|--------|--------|--------|--------|----|-------|-------|-------|----|----|-------|---------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 0 | IDFSL3 | IDFSL2 | IDFSL1 | IDFSL0 | 0 | DFSL5 | IDFT1 | IDFT0 | 0 | 0 | LPDF0 | INVRFDC |

IDFSL3: New DFCT detection output setting.
 When "0", only the DFCT signal described in §5-9 is detected and output from the DFCT pin. (default)
 When "1", the DFCT signal described in §5-9 and the new DFCT signal are switched and output from the DFCT pin.
 The switching timing is as follows.
 When the §5-9 DFCT signal is low, the new DFCT signal is output from the DFCT pin.
 When the §5-9 DFCT signal is high, this DFCT signal is output from the DFCT pin.
 In addition, the time at which the new DFCT signal can be output after the §5-9 DFCT signal switches to low can also be set. (See IDFT1 and IDFT0 of \$34E.)

| IDFSL3 | §5-9 DFCT | DFCT pin |
|--------|-----------|-----------|
| 0 | L | §5-9 DFCT |
| 0 | H | §5-9 DFCT |
| 1 | L | New DFCT |
| 1 | H | §5-9 DFCT |

IDFSL2: New DFCT detection time setting.
 DFCT = high is held for a certain time after new DFCT detection. This command sets that time.
 When "0", a long hold time. (default)
 When "1", a short hold time.

IDFSL1: New DFCT detection sensitivity setting.
 When "0", a high detection sensitivity. (default)
 When "1", a low detection sensitivity.

IDFSL0: New DFCT release sensitivity setting.
 When "0", a high release sensitivity. (default)
 When "1", a low release sensitivity.

DFSL5: DFCT slice level setting mode switching.
 When "0", the two bits of \$3B commands SDF2 and SDF1 are used to set the DFCT slice level as usual. (default)
 When "1", the six bits of \$3D commands SDF6 to SDF3 and \$3B commands SDF2 and SDF1 are used to set the DFCT slice level.

IDFT1, IDFT0: These commands set the time at which the new DFCT signal can be output (output prohibited time) after the §5-9 DFCT signal switches to low.

| | IDFT1 | IDFT0 | New DFCT signal output prohibited time |
|---|-------|-------|--|
| * | 0 | 0 | 204.08µs |
| | 0 | 1 | 294.78µs |
| | 1 | 0 | 408.16µs |
| | 1 | 1 | 612.24µs |

*: preset

LPDF0: DFCT signal generation mode switching.
 When "0", the rise time constant of the DFCT generation circuit peak hold value is as usual. (default)
 When "1", the rise time constant of the DFCT generation circuit peak hold value is weighed.

INVRFDC: RFDC signal polarity inverted input setting.
 When "0", the RFDC signal polarity is set to non-inverted. (default)
 When "1", the RFDC signal polarity is set to inverted.

\$34F

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|------|------|----|
| 1 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | — |

When D15 = D14 = D13 = D12 = D11 = 1 (\$34F)

D10 = 0

FBIAS LIMIT register write

FBL9 to FBL1: Data; data compared with FB9 to FB1, FBL9 = MSB.

When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to FB1 matches with FBL9 to FBL1.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|
| 1 | 1 | 1 | 1 | 0 | 1 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | — |

When D15 = D14 = D13 = D12 = 1 (\$34F)

D11 = 0, D10 = 1

FBIAS register write

FB9 to FB1: Data; two's complement data, FB9 = MSB.

For FE input conversion, FB9 to FB1 = 011111111 corresponds to $255/256 \times V_{DD}/4$ and FB9 to FB1 = 100000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD} : supply voltage)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | 1 | 1 | 0 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 |

When D15 = D14 = D13 = D12 = 1 (\$34F)

D11 = 0, D10 = 0

TRVSC register write

TV9 to TV0: Data; two's complement data, TV9 = MSB.

For TE input conversion, TV9 to TV0 = 00111111111 corresponds to $255/256 \times V_{DD}/4$ and TV9 to TV0 = 11000000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD} : supply voltage)

- Notes)**
- When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit TV8 to TV0 during external write are read out.
 - When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

\$35 (preset: \$35 58 2D)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FT1 | FT0 | FS5 | FS4 | FS3 | FS2 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 |

FT1, FT0, FTZ: Focus search-up speed

Default value: 010 ($0.673 \times V_{DD}$ /s)

Focus drive output conversion

| FT1 | FT0 | FTZ | Focus search speed [V/s] |
|-----|-----|-----|--------------------------|
| 0 | 0 | 0 | $1.35 \times V_{DD}$ |
| * 0 | 1 | 0 | $0.673 \times V_{DD}$ |
| 1 | 0 | 0 | $0.449 \times V_{DD}$ |
| 1 | 1 | 0 | $0.336 \times V_{DD}$ |
| 0 | 0 | 1 | $1.79 \times V_{DD}$ |
| 0 | 1 | 1 | $1.08 \times V_{DD}$ |
| 1 | 0 | 1 | $0.897 \times V_{DD}$ |
| 1 | 1 | 1 | $0.769 \times V_{DD}$ |

*: preset, V_{DD} : PWM driver supply voltage

FS5 to FS0: Focus search limit voltage

Default value: 011000 ($(1 \pm 24/64) \times V_{DD}/2$, V_{DD} : PWM driver supply voltage)

Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value

Default value: 0101101

\$36 (preset: \$36 0E 2E)

| | | | | | | | | | | | | | | | |
|------|------|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TDZC | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 |

TDZC: Selects the TZC signal for generating the TRKCNCL signal during brake circuit operation. When "0", the edge of the HPTZC or STZC signal, whichever has the faster phase, is used. When "1", the edge of the HPTZC, STZC signal or the tracking drive signal zero-cross, whichever has the faster phase, is used. (See §5-12.)

DTZC: DTZC delay ($8.5/4.25\mu\text{s}$, when $MCK = 128Fs$)

Default value: 0 ($4.25\mu\text{s}$)

TJ5 to TJ0: Track jump voltage

Default value: 001110 ($(1 \pm 14/64) \times V_{DD}/2$, V_{DD} : PWM driver supply voltage)

Tracking drive output conversion

SFJP: Surf jump mode on/off

The tracking PWM output is generated by adding the tracking filter output and TJReg (TJ5 to TJ0), by setting D7 to "1" (on)

TG6 to TG0: AGT convergence gain setting value

Default value: 0101110

\$37 (preset: \$37 50 BA)

| | | | | | | | | | | | | | | | |
|------|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGGT | AGV1 | AGV2 | AGHS | AGHT |

FZSH, FZSL: FZC (Focus Zero Cross) slice level
 Default value: 01 ($1/8 \times V_{DD}/2$, V_{DD} : supply voltage); FE input conversion

| | FZSH | FZSL | Slice level |
|---|------|------|------------------------|
| | 0 | 0 | $1/4 \times V_{DD}/2$ |
| * | 0 | 1 | $1/8 \times V_{DD}/2$ |
| | 1 | 0 | $1/16 \times V_{DD}/2$ |
| | 1 | 1 | $1/32 \times V_{DD}/2$ |

*: preset

SM5 to SM0: Sled move voltage
 Default value: 010000 ($(1 \pm 16/64) \times V_{DD}/2$, V_{DD} : PWM driver supply voltage)
 Sled drive output conversion

AGS: AGCNTL self-stop on/off
 Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment
 (31/63ms, when MCK = 128Fs)
 Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)
 Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)
 Default value: 1 (large)

| | | FE/TE input conversion |
|------|-------------------------|--|
| AGGF | 0 (small) 1 (large)* | $1/32$ to $V_{DD}/2$ $1/16$ to $V_{DD}/2$ |
| AGGT | 0 (small) 1 (large)* | $1/16$ to $V_{DD}/2$ $1/8$ to $V_{DD}/2$ |

*: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low
 Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low
 Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off
 Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)
 Default value: 0 (256ms)

\$38 (preset: \$38 00 00)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|-----|------|------|------|-----|-----|------|------|------|------|------|------|------|------|
| VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 |

DC offset cancel. See §5-3.

- * VCLM: VC level measurement (on/off)
- VCLC: VC level compensation for FCS In register (on/off)
- * FLM: Focus zero level measurement (on/off)
- FLC0: Focus zero level compensation for FZC register (on/off)
- * RFLM: RF zero level measurement (on/off)
- RFLC: RF zero level compensation (on/off)

Automatic gain control. See §5-6.

- AGF: Focus auto gain adjustment (on/off)
- AGT: Tracking auto gain adjustment (on/off)

Misoperation prevention circuit

- DFSW: Defect disable switch (on/off)
Setting this switch to "1" (on) disables the defect countermeasure circuit.
- LKSW: Lock switch (on/off)
Setting this switch to "1" (on) disables the sled free-running prevention circuit.

DC offset cancel. See §5-3.

- TBLM: Traverse center measurement (on/off)
- * TCLM: Tracking zero level measurement (on/off)
- FLC1: Focus zero level compensation for FCS In register (on/off)
- TLC2: Traverse center compensation (on/off)
- TLC1: Tracking zero level compensation (on/off)
- TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with * are accepted every 2.9ms. (when MCK = 128Fs)
All commands are on when "1".

\$39 (preset: \$390000)

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |

When \$3A command SVDA = 0

DAC: Serial data readout DAC mode setting.
 When "0", serial data cannot be read out. (default)
 When "1", serial data can be read out.

SD6 to SD0: These bits select the serial readout data.

| D14 | D13 | D12 | D11 | D10 | D9 | D8 | Readout data | Readout data length |
|-----|-------------------------|------------------|-----|-----|-----|-----|----------------------|---------------------|
| SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | | |
| 1 | Coefficient RAM address | | | | | | Coefficient RAM data | 8 bits |
| 0 | 1 | Data RAM address | | | | | Data RAM data | 16 bits |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | RF AVRG register | 8 bits |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | RFDC input signal | 8 bits |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | FCS Bias register | 9 bits |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | TRVSC register | 9 bits |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | DFCT count | 8 bits |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | RFDC (Bottom) | 8 bits |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | RFDC (Peak) | 8 bits |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | RFDC (Peak – Bottom) | 8 bits |
| 0 | 0 | 0 | 1 | 1 | — | — | VC AVRG register | 9 bits |
| 0 | 0 | 0 | 1 | 0 | — | — | FE AVRG register | 9 bits |
| 0 | 0 | 0 | 0 | 1 | — | — | TE AVRG register | 9 bits |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | FE input signal | 8 bits |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | TE input signal | 8 bits |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | SE input signal | 8 bits |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | VC input signal | 8 bits |

—: don't care

Note) When \$3A SVDA is changed, select the readout data again.

When \$3A command SVDA = 1

DAC: This command selects whether to set readout data for the left or right channel.

When "0", right channel readout data is selected. (default)

When "1", left channel readout data is selected.

SD6 to SD0: These bits select the data to be output from the left or right channel.

| D14 | D13 | D12 | D11 | D10 | D9 | D8 | Readout data | Readout data length |
|-----|-----|------------------|-----|-----|-----|-----|----------------------|---------------------|
| SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | | |
| 0 | 1 | Data RAM address | | | | | Data RAM data | 16 bits |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | RF AVRG register | 8 bits |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | RFDC input signal | 8 bits |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | FCS Bias register | 9 bits |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | TRVSC register | 9 bits |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | FCS output signal | 8 bits |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | TRK output signal | 8 bits |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | VC AVRG register | 9 bits |
| *1 | 0 | 0 | 0 | 1 | 0 | 0 | FE AVRG register | 9 bits |
| | 0 | 0 | 0 | 0 | 1 | 1 | FE (A-B): FCS in Reg | 9 bits |
| | 0 | 0 | 0 | 0 | 1 | 0 | TE (E-F): TRK in Reg | 9 bits |
| *2 | 0 | 0 | 0 | 0 | 1 | 0 | TE AVRG register | 9 bits |
| | 0 | 0 | 0 | 0 | 0 | 1 | FE input signal | 8 bits |
| | 0 | 0 | 0 | 0 | 0 | 1 | TE input signal | 8 bits |
| | 0 | 0 | 0 | 0 | 0 | 0 | SE input signal | 8 bits |
| | 0 | 0 | 0 | 0 | 0 | 0 | VC input signal | 8 bits |

*1 Right channel preset

*2 Left channel preset

Note) Coefficient RAM data cannot be output from the audio DAC side.

Do not output RFDC (peak, bottom, peak-bottom) or the DFCT count from the audio DAC side.

When \$3A SVDA is changed, select the readout data again.

The DFCT count counts the number of times the DFCT signal rises while \$3994 is set.

Readout outputs the DFCT count at that time.

Memory Readout

The following three memories can be readout without waiting the memory access.

- M02 (Sled filter final memory)
- M12 (Focus hold filter final memory)
- M1A (Track hold filter final memory)

\$3A (D15 = 0) (preset: \$3A0000)

| | | | | | | | | | | | | | | | |
|-----|------|------|------|------|------|-------|------|------|------|------|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | FIFZC | TJDO | FPS1 | FPS0 | TPS1 | TPS0 | SVDA | SJHD | INBK | MTIO |

FBON: FBIAS (focus bias) register operation setting.

| | | | |
|------|------|------|---|
| FBON | FBSS | FBUP | Processing |
| 0 | 0 | — | FBIAS (focus bias) register addition off. |
| 1 | 0 | — | FBIAS (focus bias) register addition on. |
| 1 | 1 | 0 | FBIAS register acts as a down counter. |
| 1 | 1 | 1 | FBIAS register acts as an up counter. |

—: don't care

FBV1, FBV0: FBIAS (focus bias) counter voltage switching.
The number of FCS BIAS count-up/-down steps per cycle is decided by these bits.

| FBV1 | FBV0 | Number of steps per cycle |
|------|------|---------------------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately $1/2^9 \times V_{DD}/2$, V_{DD} = supply voltage.

*: preset

FIFZC: This selects the FZC slice level setting command.
When "0", the FZC slice level is determined by the \$37 FZSH and FZSL setting values. (default)
When "1", the FZC slice level is determined by the \$3F8 FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values.

This allows more detailed setting and the addition of hysteresis compared to the \$37 FZSH and FZSL setting.

TJDO: This sets the tracking servo filter data RAM to "0" when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.

These are effective for increasing the overall gain in order to widen the servo band, etc. Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

| FPS1 | FPS0 | Relative gain | TPS1 | TPS0 | Relative gain |
|------|------|---------------|------|------|---------------|
| 0 | 0 | 0dB | 0 | 0 | 0dB |
| 0 | 1 | +6dB | 0 | 1 | +6dB |
| 1 | 0 | +12dB | 1 | 0 | +12dB |
| 1 | 1 | +18dB | 1 | 1 | +18dB |

*: preset

SVDA: This allows the data set by the \$39 command to be output through the audio DAC.
When "0", audio is output. (default)

When "1", the data set by the \$39 command is output.

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When INBK = 0 (off), the brake circuit masks the tracking drive signal with the TRKCNCL signal which is generated by taking the MIRR signal at the TZC edge. When INBK = 1 (on), the tracking filter input is masked instead of the drive output.

MTIO: The tracking filter input is masked when the MIRR signal is high by setting MTIO = 1 (on).

\$3A8 (preset : \$3A 80 00)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-------|-------|-------|-------|----|----|----|----|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | FPGS1 | FPGS0 | TPGS1 | TPGS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FPGS1, FPGS0: These increase +6dB, +12dB and +18dB immediately before FCS SRCH.

TPGS1, TPGS0: These increase +6dB, +12dB and +18dB immediately before TRK JMP.

| | FPGS1 | FPGS0 | Gain |
|---|-------|-------|-------|
| * | 0 | 0 | 0dB |
| | 0 | 1 | +6dB |
| | 1 | 0 | +12dB |
| | 1 | 1 | +18dB |

| | TPGS1 | TPGS0 | Gain |
|---|-------|-------|-------|
| * | 0 | 0 | 0dB |
| | 0 | 1 | +6dB |
| | 1 | 0 | +12dB |
| | 1 | 1 | +18dB |

*: preset

*: preset

\$3A9 (preset : \$3A 90 00)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|-------|----|----|----|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | UDFZC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

UDFZC: This detects FZC not depending on the search direction.
 When "0", FZC is detected for UP search. (conventional system: default)
 When "1", FZC is detected not depending on the search direction.

\$3AFF (preset : \$3A FF 00)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|------|------|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | SRQ1 | SRQ0 | 0 | 0 |

SRQ1, SRQ0: These bits select the ASYO output delay time.

| | SRQ1 | SRQ0 | ASYO output delay time |
|---|------|------|------------------------|
| * | 0 | 0 | Approx. 0ns |
| | 0 | 1 | Approx. 5ns |
| | 1 | 0 | Approx. 10ns |
| | 1 | 1 | Approx. 15ns |

*: preset

\$3B (preset: \$3B E0 50)

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|-----|------|------|------|------|------|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 |

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 ($28/256 \times V_{DD}/2$, V_{DD} = supply voltage)

RFDC input conversion

| SFOX | SFO2 | SFO1 | Slice level |
|------|------|------|--------------------------|
| 0 | 0 | 0 | $16/256 \times V_{DD}/2$ |
| 0 | 0 | 1 | $20/256 \times V_{DD}/2$ |
| 0 | 1 | 0 | $24/256 \times V_{DD}/2$ |
| * 0 | 1 | 1 | $28/256 \times V_{DD}/2$ |
| 1 | 0 | 0 | $32/256 \times V_{DD}/2$ |
| 1 | 0 | 1 | $40/256 \times V_{DD}/2$ |
| 1 | 1 | 0 | $48/256 \times V_{DD}/2$ |
| 1 | 1 | 1 | $56/256 \times V_{DD}/2$ |

*: preset

SDF2, SDF1: DFCT slice level

Default value: 10 ($0.0313 \times V_{DD}$)

RFDC input conversion

| SFO2 | SFO1 | Slice level |
|------|------|------------------------|
| 0 | 0 | $0.0156 \times V_{DD}$ |
| 0 | 1 | $0.0234 \times V_{DD}$ |
| * 1 | 0 | $0.0313 \times V_{DD}$ |
| 1 | 1 | $0.0391 \times V_{DD}$ |

*: preset, V_{DD} : supply voltage

See the \$34E command DFSLs and \$3D commands SDF6 to SDF3.

MAX2, MAX1: DFCT maximum time (MCK = 128Fs)

Default value: 00 (no timer limit)

| MAX2 | MAX1 | DFCT maximum time |
|------|------|-------------------|
| * 0 | 0 | No timer limit |
| 0 | 1 | 2.00ms |
| 1 | 0 | 2.36ms |
| 1 | 1 | 2.72ms |

*: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation

On/off (default: off)

On when "1".

D2V2, D2V1: Peak hold 2 for DFCT signal generation

Count-down speed setting

Default value: 01 ($0.086 \times V_{DD}/\text{ms}$, 44.1kHz)

[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| D2V2 | D2V1 | Count-down speed | |
|------|------|------------------------|-------|
| | | [V/ms] | [kHz] |
| 0 | 0 | $0.0431 \times V_{DD}$ | 22.05 |
| * 0 | 1 | $0.0861 \times V_{DD}$ | 44.1 |
| 1 | 0 | $0.172 \times V_{DD}$ | 88.2 |
| 1 | 1 | $0.344 \times V_{DD}$ | 176.4 |

*: preset, V_{DD} : supply voltage

D1V2, D1V1: Peak hold 1 for DFCT signal generation

Count-down speed setting

Default value: 01 ($0.688 \times V_{DD}/\text{ms}$, 352.8kHz)

[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| D1V2 | D1V1 | Count-down speed | |
|------|------|-----------------------|--------|
| | | [V/ms] | [kHz] |
| 0 | 0 | $0.344 \times V_{DD}$ | 176.4 |
| * 0 | 1 | $0.688 \times V_{DD}$ | 352.8 |
| 1 | 0 | $1.38 \times V_{DD}$ | 705.6 |
| 1 | 1 | $2.75 \times V_{DD}$ | 1411.2 |

*: preset, V_{DD} : supply voltage

RINT: This initializes the initial-stage registers of the circuits which generate MIRR, DFCT and FOK.

\$3C (preset: \$3C 00 80)

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|----|------|------|------|------|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| COSS | COTS | CETZ | CETF | COT2 | COT1 | MOT2 | 0 | BTS1 | BTS0 | MRC1 | MRC0 | 0 | 0 | 0 | 0 |

COSS, COTS: These select the TZC signal used when generating the COUT signal.

| COSS | COTS | TZC |
|------|------|-------|
| 1 | — | STZC |
| 0 | 0 | HPTZC |
| 0 | 1 | DTZC |

*: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
 DTZC is the delayed phase STZC. (The delay time can be selected by D14 of \$36.)
 HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
 See §5-13.

CETZ: Normally, the input from the TE pin enters the TRK filter and is used to generate the TZC signal. However, the input from the CE pin can also be used. This function is for the center error servo.

When "0", the TZC signal is generated by using the signal input to the TE pin.
 When "1", the TZC signal is generated by using the signal input to the CE pin.

CETF: When "0", the signal input to the TE pin is input to the TRK servo filter.
 When "1", the signal input to the CE pin is input to the TRK servo filter.

These commands output the TZC signal.

COT2, COT1: The COUT signal is replaced by the TZC signal. Concretely, the TZC signal is output from the COUT pin and the TZC signal is used for auto sequence instead of the COUT signal.

| COT2 | COT1 | COUT pin output |
|------|------|-----------------|
| 1 | — | STZC |
| 0 | 1 | HPTZC |
| 0 | 0 | COUT |

*: preset, —: don't care

MOT2: The MIRR signal is replaced by the STZC signal. Concretely, the STZC signal is output from the MIRR pin and the STZC signal is used for generating the COUT signal instead of the MIRR signal.

These commands set the MIRR signal generation circuit.

BTS1, BTS0: These set the count-up speed for the bottom hold value of the MIRR generation circuit. The time per step is approximately 708ns (when MCK = 128Fs). The preset value is BTS1 = 1, BTS0 = 0 like the CXD2586R. These bits are valid only when BTF of \$3B is "0".

MRC1, MRC0: These set the minimum pulse width for masking the MIRR signal of the MIRR generation circuit. As noted in §5-9, the MIRR signal is generated by comparing the waveform obtained by subtracting the bottom hold value from the peak hold value with the MIRR comparator level. Strictly speaking, however, for MIRR to become high, these levels must be compared continuously for a certain time. These bits set that time. The preset value is MRC1 = 0, MRC0 = 0 like the CXD2586R.

| BTS1 | BTS0 | Number of count-up steps per cycle | MRC1 | MRC0 | Setting time [μs] |
|------|------|------------------------------------|------|------|-------------------|
| 0 | 0 | 1 | 0 | 0 | 5.669* |
| 0 | 1 | 2 | 0 | 1 | 11.338 |
| 1 | 0 | 4 | 1 | 0 | 22.675 |
| 1 | 1 | 8 | 1 | 1 | 45.351 |

*: preset (when MCK = 128Fs)

\$3D (preset: \$3D 00 00)

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|------|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SFID | SFSK | THID | THSK | ABEF | TLD2 | TLD1 | TLD0 | SDF6 | SDF5 | SDF4 | SDF3 | 0 | 0 | 0 | 0 |

- SFID:** SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When the low frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.
- SFSK:** Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.
- THID:** TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as TRK hold filter input.
- THSK:** Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.
* See "\$5-20. Filter Composition" regarding the SFID, SFSK, THID and THSK commands.
- ABEF:** The focus error (FE) and tracking error (TE) can be generated internally.
When 0, the FE and TE signal input mode results. Input each error signal through the FE and TE pins. (default)
When 1, the FE and TE signal generation mode results and the FE and TE signals are generated internally.
- TLD2 to TLD0:** These turn on and off SLD filter correction independently of the TRK filter.
See \$38 (TLC0 to TLC2) and Fig. 5-3.

| TLC2 | TLD2 | Traverse center correction | |
|------|------|----------------------------|------------|
| | | TRK filter | SLD filter |
| 0 | — | OFF | OFF |
| 1 | 0 | ON | ON |
| | 1 | ON | OFF |

| TLC1 | TLD1 | Tracking zero level correction | |
|------|------|--------------------------------|------------|
| | | TRK filter | SLD filter |
| 0 | — | OFF | OFF |
| 1 | 0 | ON | ON |
| | 1 | ON | OFF |

| TLC0 | TLD0 | VC level correction | |
|------|------|---------------------|------------|
| | | TRK filter | SLD filter |
| 0 | — | OFF | OFF |
| 1 | 0 | ON | ON |
| | 1 | ON | OFF |

*: preset, —: don't care

SDF6 to SDF3: These set the DEFECT slice level when the \$34E command DFSLS = 1.

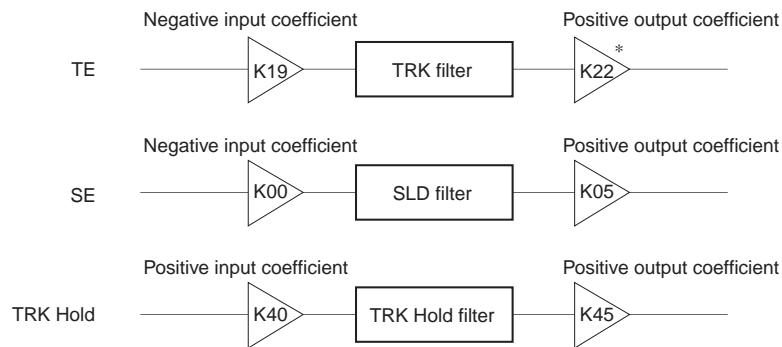
| SDF6 to SDF1 | Slice level |
|--------------|--------------------------|
| 111111 | $63/256 \times V_{DD}/2$ |
| 111110 | $62/256 \times V_{DD}/2$ |
| 111101 | $61/256 \times V_{DD}/2$ |
| : | : |
| * 000010 | $2/256 \times V_{DD}/2$ |
| 000001 | $1/256 \times V_{DD}/2$ |
| 000000 | 0 |

*: preset

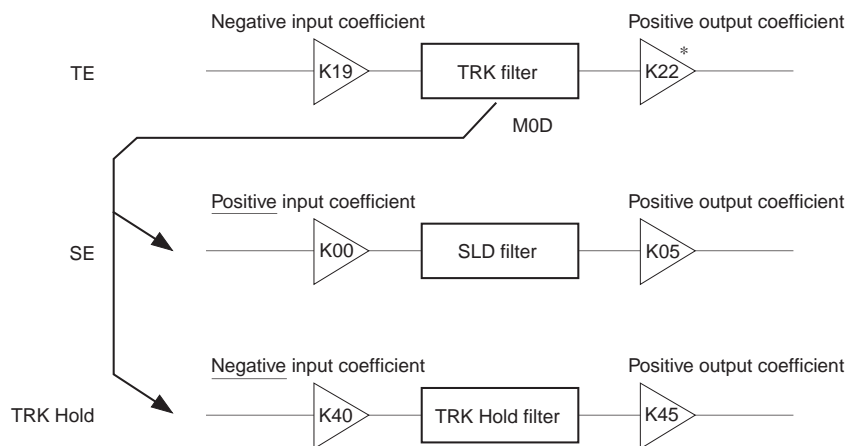
Note) Set SDF2 and SDF1 with the \$3B command.

- Input coefficient sign inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the CXD3048R outputs servo drives which have the reversed phase of input errors.



When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so the SLD input coefficient (K00) sign must be inverted. (For example, inverting the sign for coefficient K00: E0h results in 20h.) For the same reason, when THID = 1, the TRK hold input coefficient (K40) sign must be inverted.



* For TRK servo gain normal
See "\$5-20. Filter Composition".

\$3E (preset: \$3E 00 00)

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|----|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | 0 | LKIN | COIN | MDFI | MIRI | XT1D |

- F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
 On when "1"; default is "0".
 F1NM: Gain normal
 F1DM: Gain down
- T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
 On when "1"; default is "0".
 T1NM: Gain normal
 T1UM: Gain up
- F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
 On when "1"; default is "0".
 Generally, the advance amount of the phase increases by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
 F3NM: Gain normal
 F3DM: Gain down
- T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
 On when "1"; default is "0".
 Generally, the advance amount of the phase increases by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
 T3NM: Gain normal
 T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
 See "\$5-20 Filter Composition" at the end of this specification concerning quasi double accuracy.

- DFIS: FCS hold filter input extraction node selection
 0: M05 (Data RAM address 05); default
 1: M04 (Data RAM address 04)
- TLCD: This command masks the TLC2 command set by D2 of \$38 only when FOK is low.
 On when "1"; default is "0".
- LKIN: When "0", the internally generated LOCK signal is output to the LOCK pin. (default)
 When "1", the LOCK signal can be input from an external source to the LOCK pin.
- COIN: When "0", the internally generated COUT signal is output to the COUT pin. (default)
 When "1", the COUT signal can be input from an external source to the COUT pin.

The MIRR, DFCT and FOK signals can also be input from an external source.

- MDFI: When "0", the MIRR, DFCT and FOK signals are generated internally. (default)
 When "1", the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.
- MIRI: When "0", the MIRR signal is generated internally. (default)
 When "1", the MIRR signal can be input from an external source through the MIRR pin.

| | MDFI | MIRI | |
|---|------|------|---|
| * | 0 | 0 | MIRR, DFCT and FOK are all generated internally. |
| | 0 | 1 | MIRR only is input from an external source. |
| | 1 | — | MIRR, DFCT and FOK are all input from an external source. |

*: preset, —: don't care

- XT1D: The input to the servo master clock is used without being frequency-divided by setting XT1D to "1". This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of \$3F for XT2D and XT4D.

\$3F (preset: \$3F 00 10)

| | | | | | | | | | | | | | | | |
|-----|------|------|------|-----|------|------|------|----|------|-----|----|------|----|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | FTQ | 1 | SRO1 | 0 | AGHF | ASOT |

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
 When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

| AGG4 | AGGF | AGGT | Sine wave amplitude | |
|------|------|------|--------------------------|-------------------------|
| | | | FE input conversion | TE input conversion |
| 0 | 0 | — | $1/32 \times V_{DD}/2$ | — |
| | 1 | — | $1/16 \times V_{DD}/2^*$ | — |
| | — | 0 | — | $1/16 \times V_{DD}/2$ |
| | — | 1 | — | $1/8 \times V_{DD}/2^*$ |
| 1 | 0 | 0 | $1/64 \times V_{DD}/2$ | |
| | 0 | 1 | $1/32 \times V_{DD}/2$ | |
| | 1 | 0 | $1/16 \times V_{DD}/2$ | |
| | 1 | 1 | $1/8 \times V_{DD}/2$ | |

See \$37 for AGGF and AGGT. The presets are AGG4 = 0, AGGF = 1 and AGGT = 1.

*: preset, —: don't care

XT4D, XT2D: MCK (digital servo master clock) frequency division ratio setting
 This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated. See the description of \$3E for XT1D. Also, see "§5-2. Digital Servo Block Master Clock (MCK)".

| | XT1D | XT2D | XT4D | Frequency division ratio |
|---|------|------|------|--------------------------|
| * | 0 | 0 | 0 | According to XTSL |
| | 1 | — | — | 1/1 |
| | 0 | 1 | — | 1/2 |
| | 0 | 0 | 1 | 1/4 |

*: preset, —: don't care

DRR2 to DRR0: Partially clears the Data RAM values ("0" write).
 The following values are cleared when "1" (on) respectively; default is "0".

- DRR2: M08, M09, M0A
- DRR1: M00, M01, M02
- DRR0: M00, M01, M02 only when LOCK = low

Note) Set DRR1 and DRR0 on for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, the FCS servo filter is forcibly set to gain normal status.

On when "1"; default is "0".

FTQ: The slope of the output during focus search is 1/4 the conventional output slope.

On when "1"; default is "0".

SRO1: This command is used to continuously externally output various data inside the digital servo block which have been specified with the \$39 command. (However, D15 (DAC) of \$39 must be set to "1".)
Digital output (SOCK, XOLT and SOUT) can be obtained from three specified pins by setting this command to "1".

| | SRO1 = 1 |
|------|-----------------------|
| SOLK | Output from XPCK pin. |
| XOLT | Output from GFS pin. |
| SOUT | Output from XUGF pin. |

AGHF: This halves the frequency of the internally generated sine wave during AGC.
ASOT: The anti-shock signal, which is internally detected, is output from the ATSK pin.
Output when "1"; default is "0".
Vibration detection when a high signal is output for the anti-shock signal output.

\$3F8 (preset: \$3F8800)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|------|------|------|------|--------|--------|--------|--------|--------|--------|--------|--------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | SYG3 | SYG2 | SYG1 | SYG0 | FIFZB3 | FIFZB2 | FIFZB1 | FIFZB0 | FIFZA3 | FIFZA2 | FIFZA1 | FIFZA0 |

SYG3 to SYG0: These simultaneously set the focus drive, tracking drive and sled drive output gains. See the \$AF and \$CX commands for the spindle drive output gain setting.

| SYG3 | SYG2 | SYG1 | SYG0 | GAIN |
|------|------|------|------|-----------------|
| 0 | 0 | 0 | 0 | 0 (−∞dB) |
| 0 | 0 | 0 | 1 | 0.125 (−18.1dB) |
| 0 | 0 | 1 | 0 | 0.250 (−12.0dB) |
| 0 | 0 | 1 | 1 | 0.375 (−8.5dB) |
| 0 | 1 | 0 | 0 | 0.500 (−6.0dB) |
| 0 | 1 | 0 | 1 | 0.625 (−4.1dB) |
| 0 | 1 | 1 | 0 | 0.750 (−2.5dB) |
| 0 | 1 | 1 | 1 | 0.875 (−1.2dB) |
| * | 1 | 0 | 0 | 1.000 (0.0dB) |
| | 1 | 0 | 1 | 1.125 (+1.0dB) |
| | 1 | 0 | 1 | 1.250 (+1.9dB) |
| | 1 | 0 | 1 | 1.375 (+2.8dB) |
| | 1 | 1 | 0 | 1.500 (+3.5dB) |
| | 1 | 1 | 0 | 1.625 (+4.2dB) |
| | 1 | 1 | 1 | 1.750 (+4.9dB) |
| | 1 | 1 | 1 | 1.875 (+5.5dB) |

*: preset

FIFZB3 to FIFZB0:

This sets the slice level at which FZC changes from high to low.

FIFZA3 to FIFZA0:

This sets the slice level at which FZC changes from low to high.

The FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values are valid only when \$3A FIFZC is "1".

Set so that the FIFZB3 to FIFZB0 ≤ FIFZA3 to FIFZA0.

Hysteresis can be added to the slice level by setting FIFZB3 to FIFZB0 < FIFZA3 to FIFZA0.

$$\text{FZC slice level} = \frac{\text{FIFZB3 to FIFZB0 or FIFZA3 to FIFZA0 setting value}}{32} \times 0.5 \times V_{DD} \text{ [V]}$$

\$3F9 (preset: \$3F9000)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|------|-------|----|----|----|----|------|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | FSUD | FFSUP | 0 | 1 | 0 | 0 | FFS5 | FFS4 | FFS3 | FFS2 | FFS1 | FFS0 |

FSUD, FFSUP: These set the focus search type.

The focus search is started by the \$47 command.

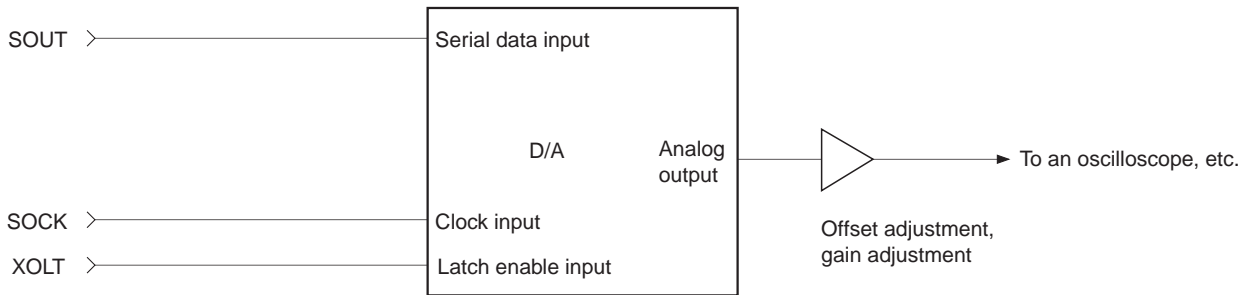
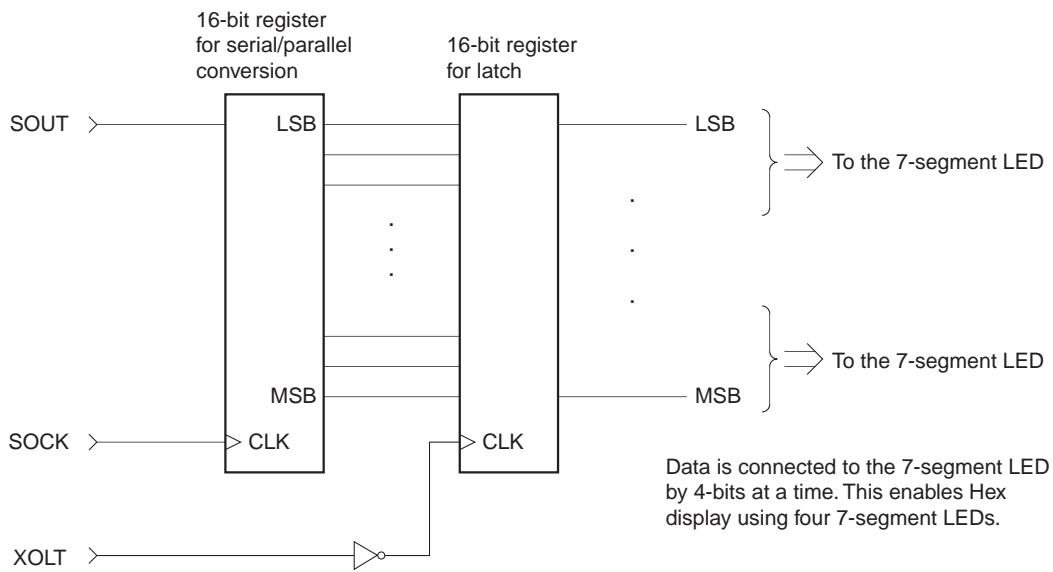
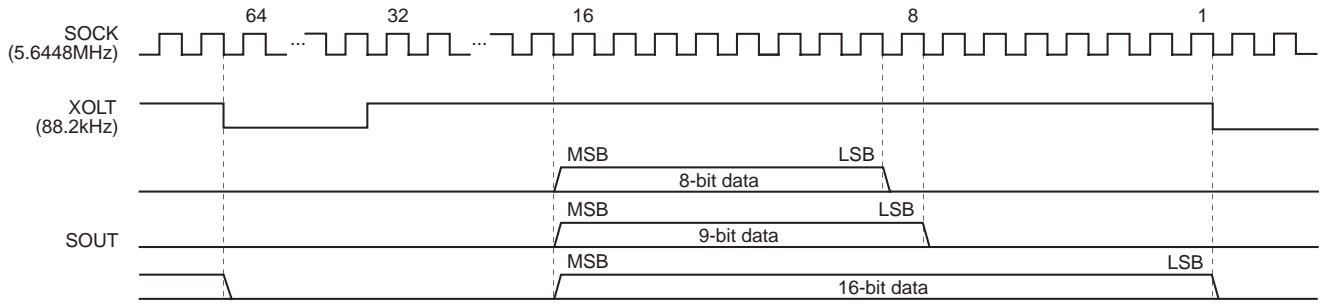
| | FSUD | FFSUP | Focus search type |
|---|------|-------|---|
| * | 0 | 0 | The usual focus search is performed. UP search is performed, and the focus servo is turned on at the FZC falling edge. |
| | 0 | 1 | Do not set. |
| | 1 | 0 | When the upper limit value is reached during the focus search, the focus search stops. After that, when the lower limit value is reached UP/DOWN search is performed. These limit values should be set with the \$35 FS5 to FS0. |
| | 1 | 1 | When the lower limit value is reached during the focus search, the focus search stops. After that, when the upper limit value is reached UP/DOWN search is performed. These limit values should be set with the \$35 FS5 to FS0. |

*: preset

FFS5 to FFS0: These set the focus search amplitude voltage. Valid only when FSUD = 1.

$$\text{Focus search amplitude} = \left(1 \pm \frac{\text{FFS5 to FFS0 setting values}}{64} \right) \times 0.5 \times V_{DD} \text{ [V]}$$

Description of Data Readout



Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

§5-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

| ADDRESS | DATA | CONTENTS |
|---------|------|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | Not used |
| K2F | 00 | Not used |

* Fix indicates that normal preset values should be used.

<Coefficient Preset Value Table (2)>

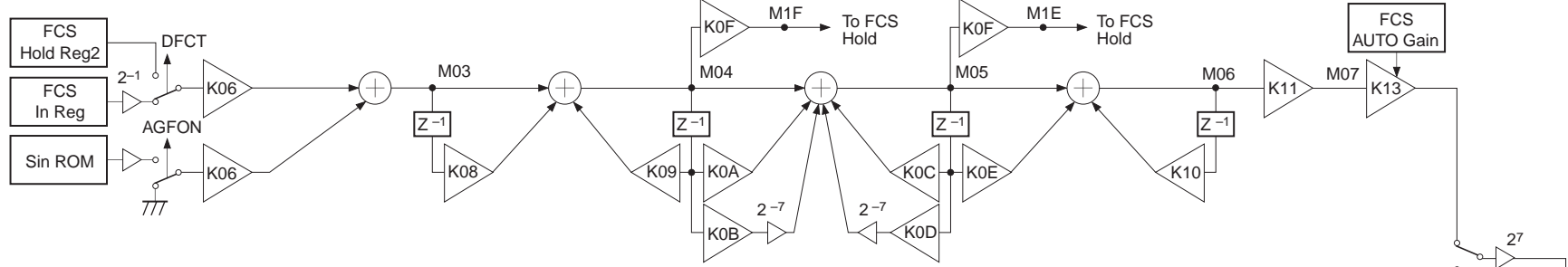
| ADDRESS | DATA | CONTENTS |
|---------|------|--|
| K30 | 80 | SLED INPUT GAIN (Only when TRK gain up2 is accessed with SFSK = 1.) |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | Not used |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | Not used |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | TRACKING HOLD FILTER INPUT GAIN (Only when TRK gain up2 is accessed with THSK = 1.) |
| K47 | 00 | Not used |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | Not used |
| K4F | 00 | Not used |

§5-20. Filter Composition

The internal filter composition is shown below.

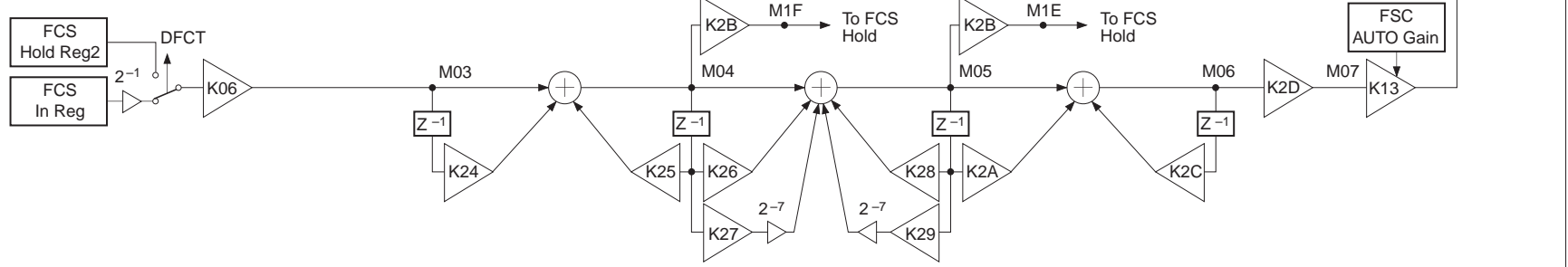
K** : Coefficient RAM address, M** : Data RAM address

FCS Servo Gain Normal fs = 88.2kHz

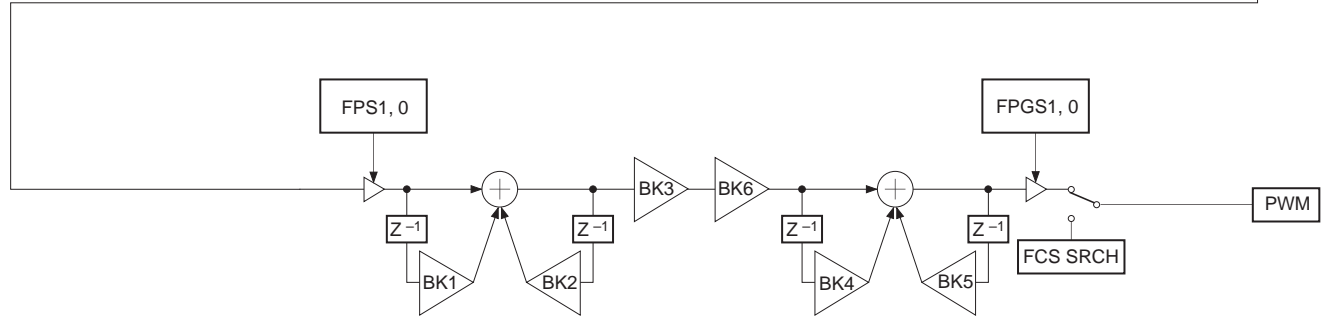


Note) Set the MSB bit of the K0B and K0D coefficients to "0".

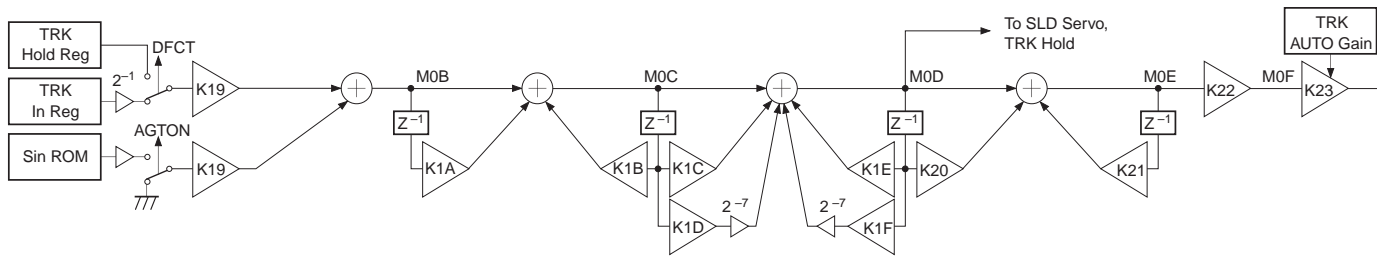
FCS Servo Gain Down fs = 88.2kHz



Note) Set the MSB bit of the K27 and K29 coefficients to "0".

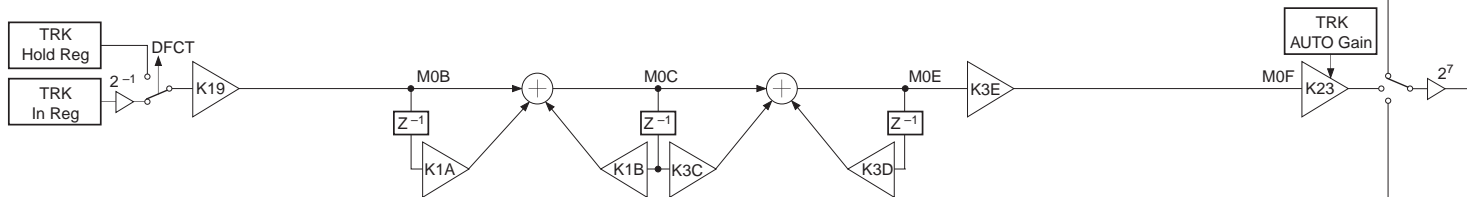


TRK Servo Gain Normal $f_s = 88.2\text{kHz}$

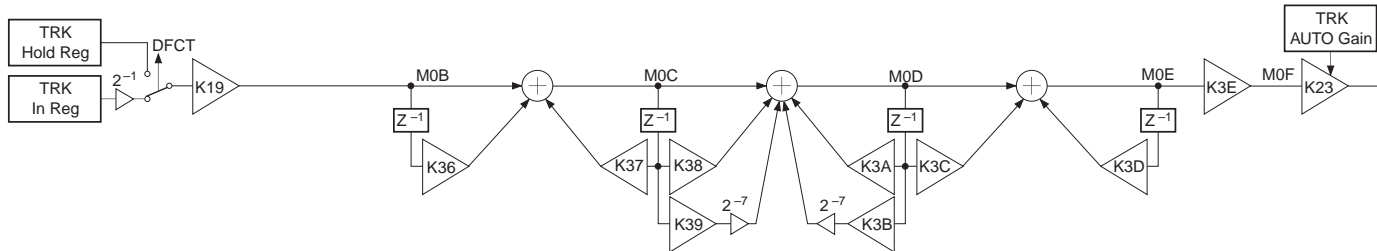


Note) Set the MSB bit of the K1D and K1F coefficients to "0".

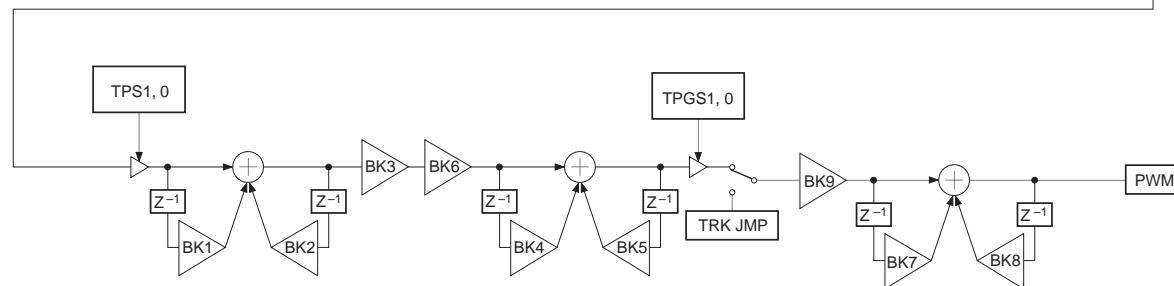
TRK Servo Gain Up1 $f_s = 88.2\text{kHz}$



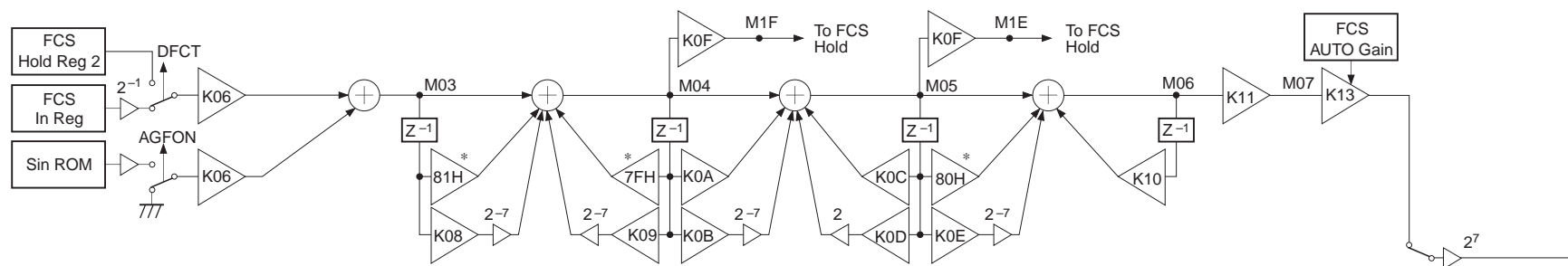
TRK Servo Gain Up2 $f_s = 88.2\text{kHz}$



Note) Set the MSB bit of the K39 and K3B coefficients to "0".

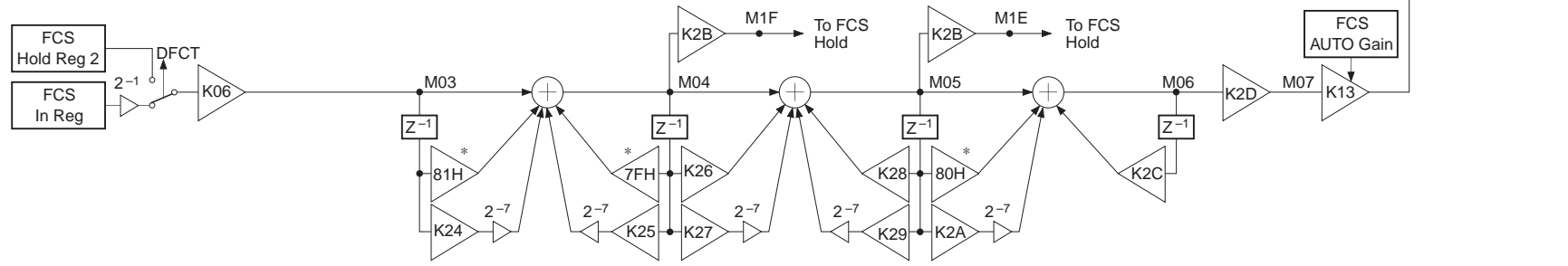


FCS Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EAXX0)



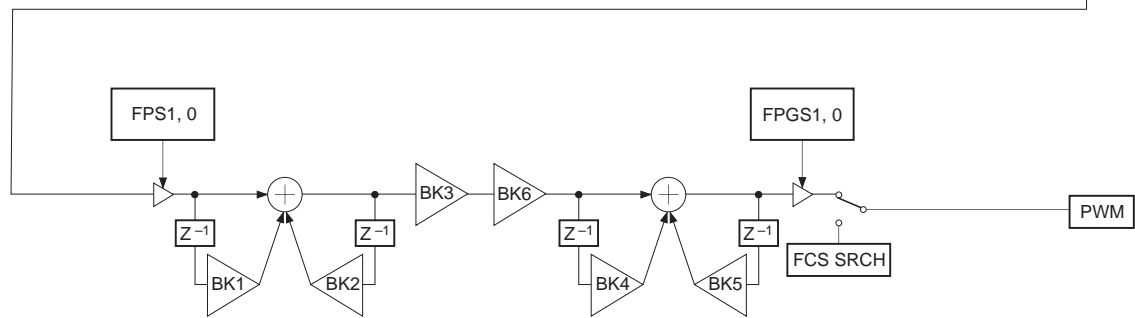
Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K0B, K09 and K0E coefficients during quasi double accuracy to "0".

FCS Servo Gain Down; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3E5XX0)

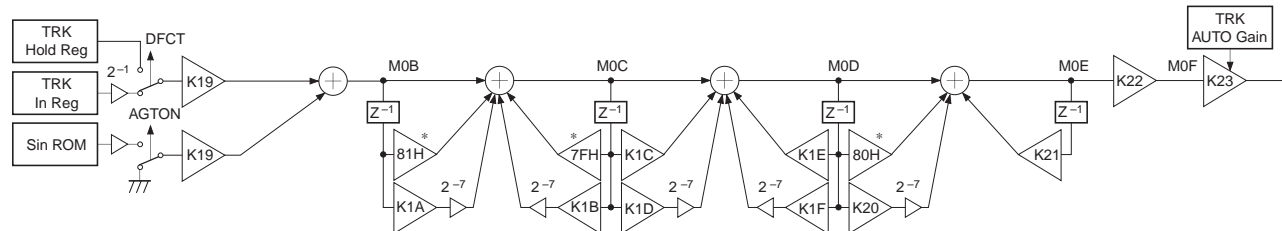


Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to "0".

* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

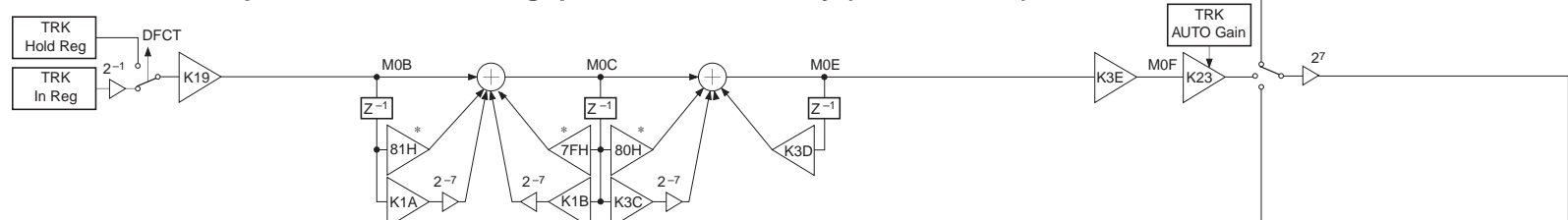


TRK Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EXAX0)



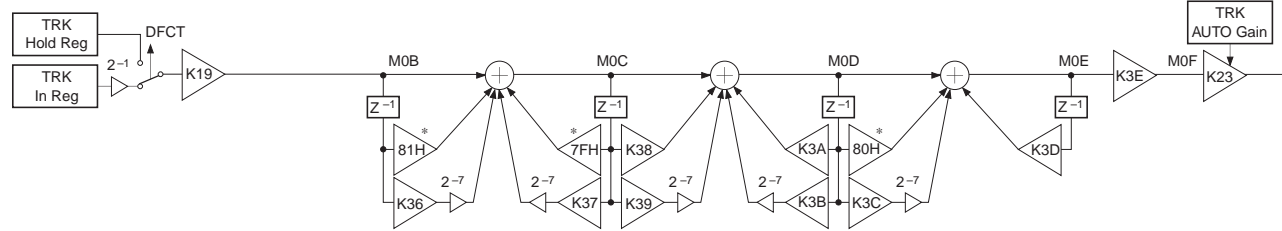
Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to "0".

TRK Servo Gain Up1; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EX5X0)



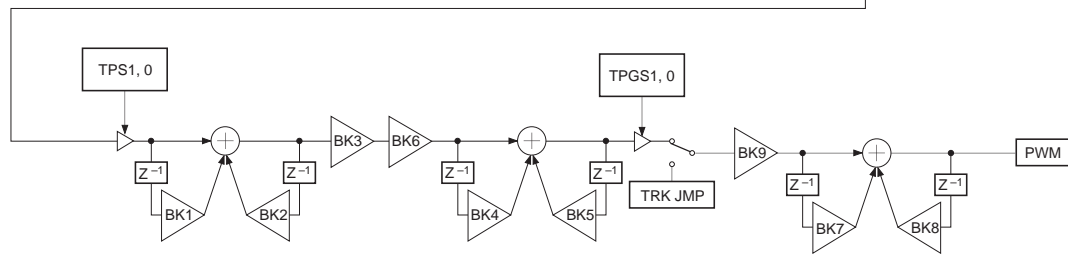
Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to "0".

TRK Servo Gain Up2; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EX5X0)



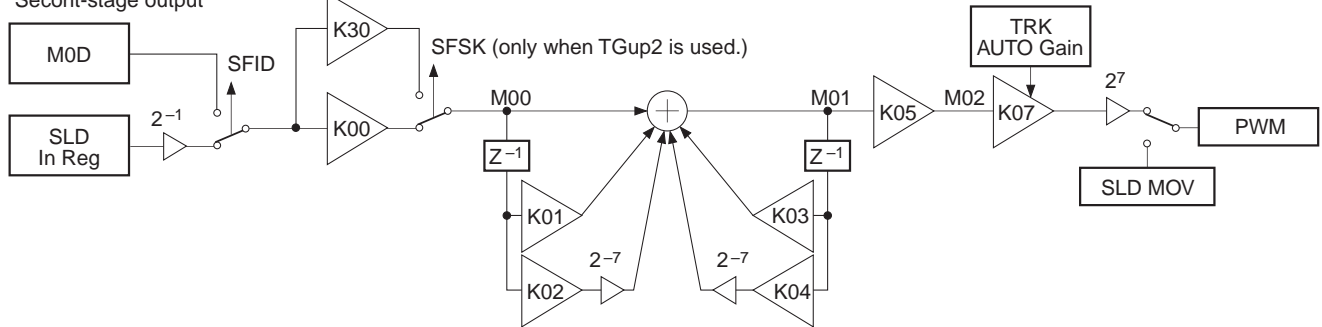
Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to "0".

* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.



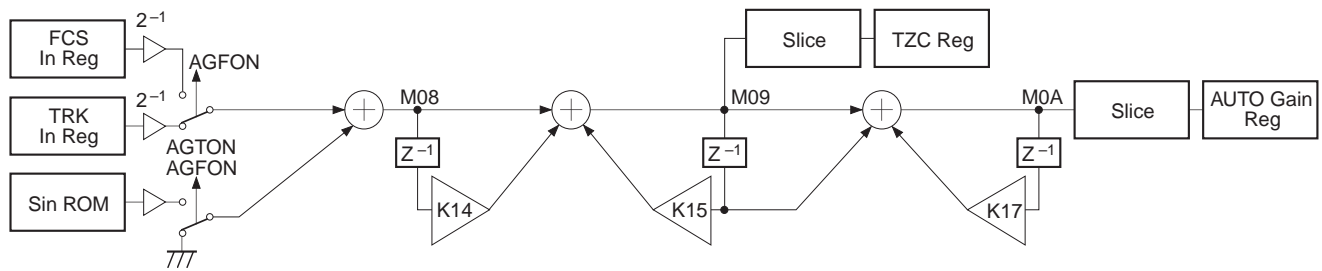
SLD Servo fs = 345Hz

TRK SERVO FILTER
Second-stage output

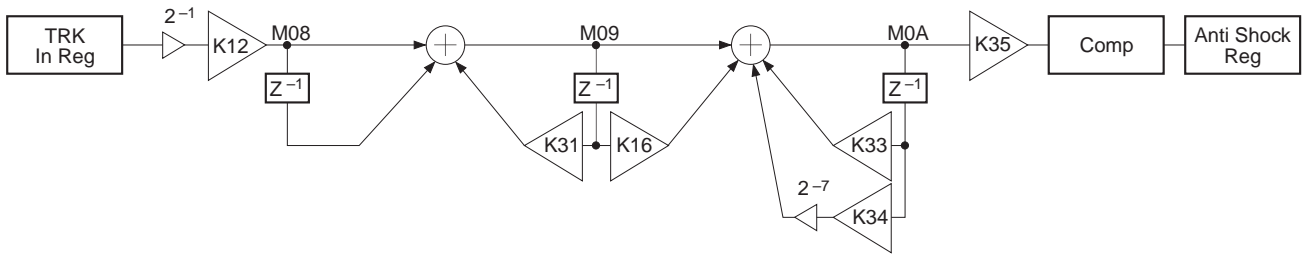


Note) Set the MSB bit of the K02 and K04 coefficients to "0".

HPTZC/Auto Gain fs = 88.2kHz

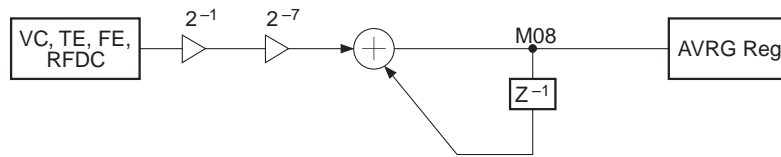


Anti Shock $f_s = 88.2\text{kHz}$

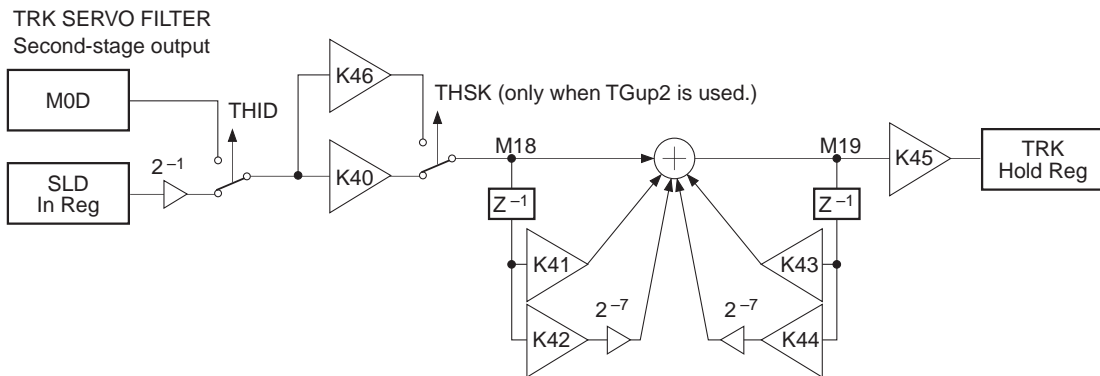


Note) Set the MSB bit of the K34 coefficient to "0".
The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG $f_s = 88.2\text{kHz}$

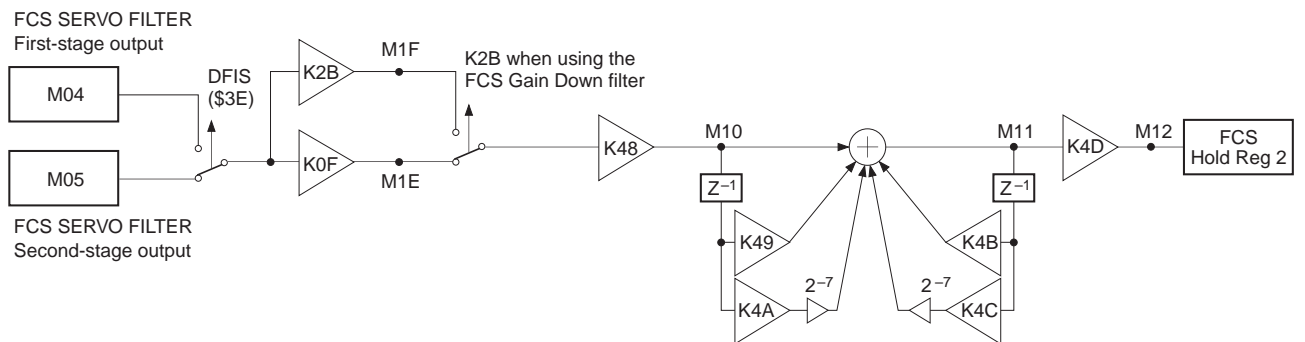


TRK Hold $f_s = 345\text{Hz}$



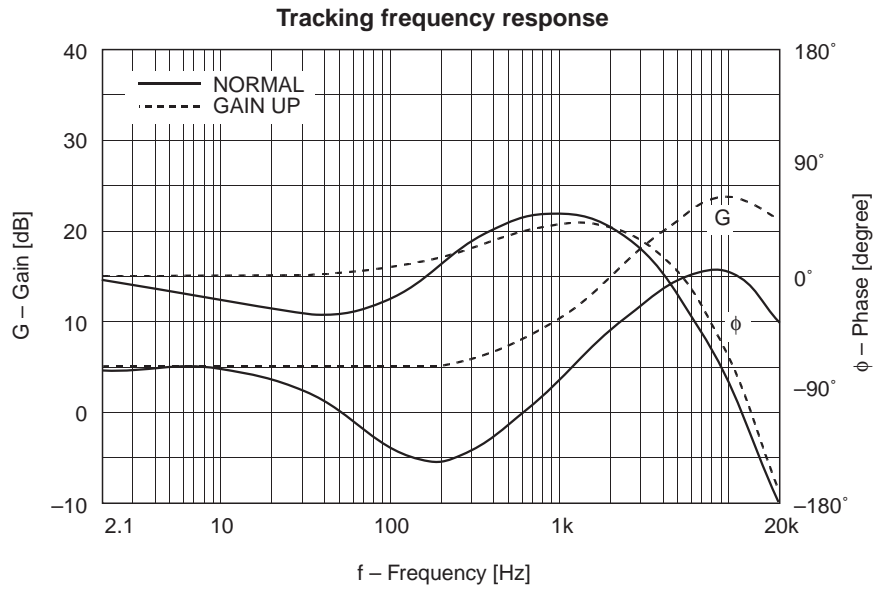
Note) Set the MSB bit of the K42 and K44 coefficients to "0".

FCS Hold $f_s = 345\text{Hz}$

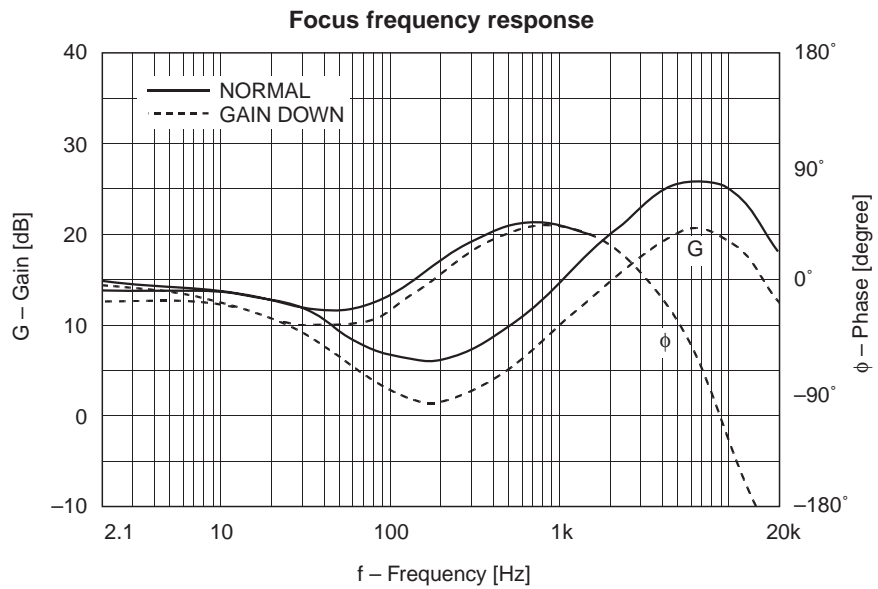


Note) Set the MSB bit of the K4A and K4C coefficients to "0".

§5-21. TRACKING and FOCUS Frequency Response



When using the preset coefficients with the boost function off.



When using the preset coefficients with the boost function off.

