SONY

CXP85840A/85848A/85856A

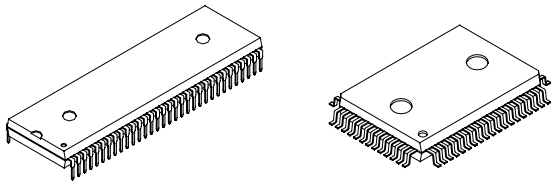
CMOS 8-bit Single Chip Microcomputer

Description

The CXP85840A/85848A/85856A are the CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, closed caption decoder, data slicer, on-screen display function, I²C bus interface, PWM output, remote control reception circuit, HSYNC counter and watchdog timer, besides the basic configurations of 8-bit CPU, ROM, RAM, I/O ports.

The CXP85840A/85848A/85856A also provide a power-on reset function and sleep function that enables to lower the power consumption.

64 pin SDIP (Plastic) 64 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

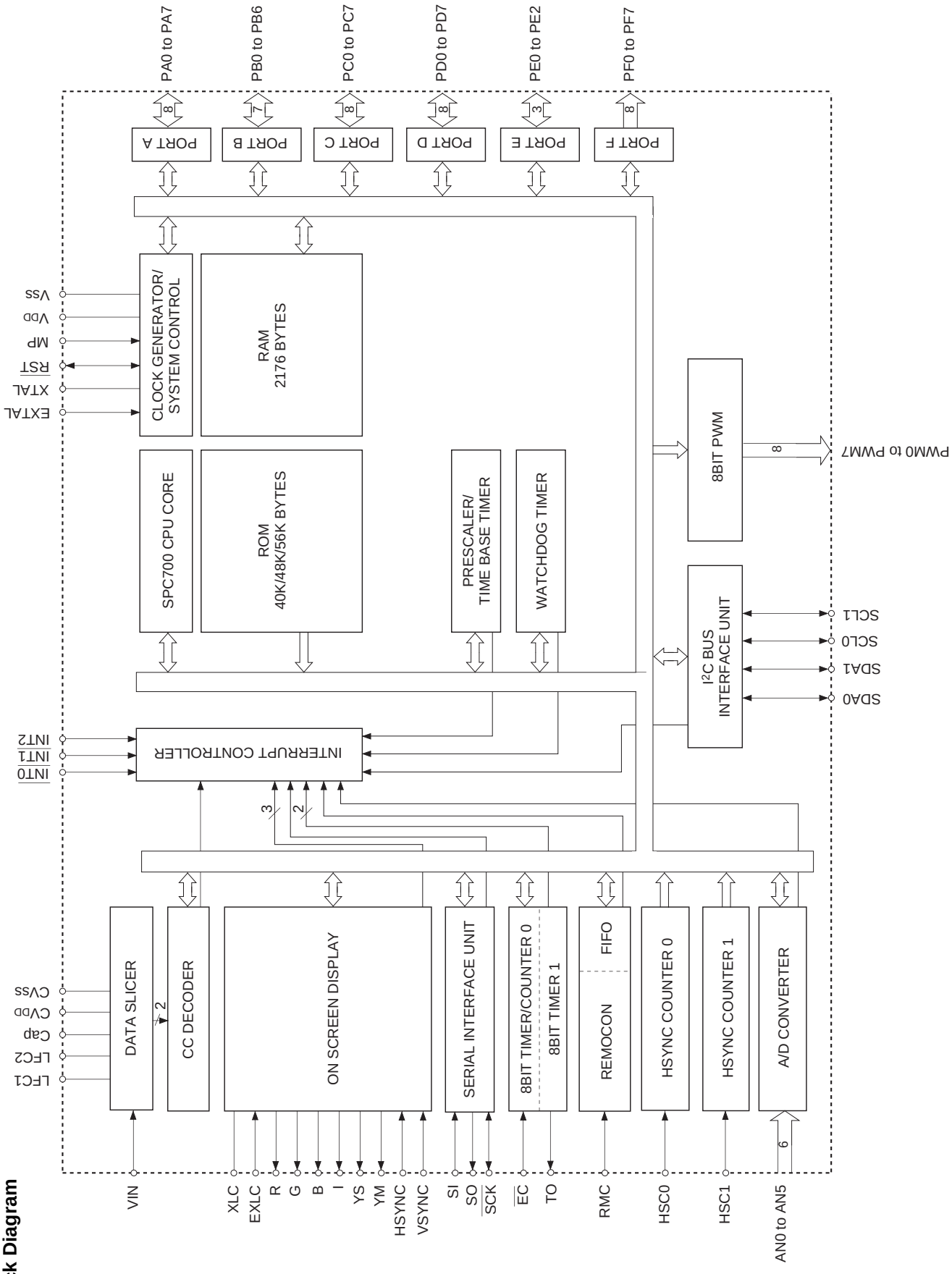
Features

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 333ns at 12MHz operation
- Incorporated ROM 40K bytes (CXP85840A)
  48K bytes (CXP85848A)
  56K bytes (CXP85856A)
- Incorporated RAM 2176 bytes (Excludes closed caption decoder and VRAM for on-screen display)
- Peripheral functions
  - A/D converter: 8-bit 6-channel successive approximation method (Conversion time of 26.7µs at 12MHz)
  - Serial interface: 8-bit clock sync type, 1 channel
  - Timer: 8-bit timer
    8-bit timer/counter
    19-bit time-base timer
  - Closed caption decoder: Data slicer
    Corresponds to FCC (EDS supported), 8 × 13 dots, 192 character types
    15 character colors, 4 lines × 34 characters
    frame background 15 colors/ half blanking
    italic, underline, vertical scrolling
  - On-screen display (OSD) function: 12 × 16 dots, 192 character types, 15 character colors
    2 lines × 24 characters
    frame background 8 colors/ half blanking
    background on full screen 15 colors/ half blanking
    edging and vertical scrolling for every line
    jitter elimination circuit
    sprite OSD, 12 × 16 dots, 1 screen, 8 colors for every dot
  - I²C bus interface
  - PWM output: 8 bits, 8 channels
  - Remote control reception circuit: 8-bit pulse measurement counter, 6-stage FIFO
  - HSYNC counter: 2 channels
  - Watchdog timer
- Interruption: 15 factors, 15 vectors, multi-interruption possible
- Standby mode: Sleep
- Package: 64-pin plastic SDIP/QFP
- Piggyback/evaluator: CXP85890A 64-pin ceramic PSDIP (Supports custom font)

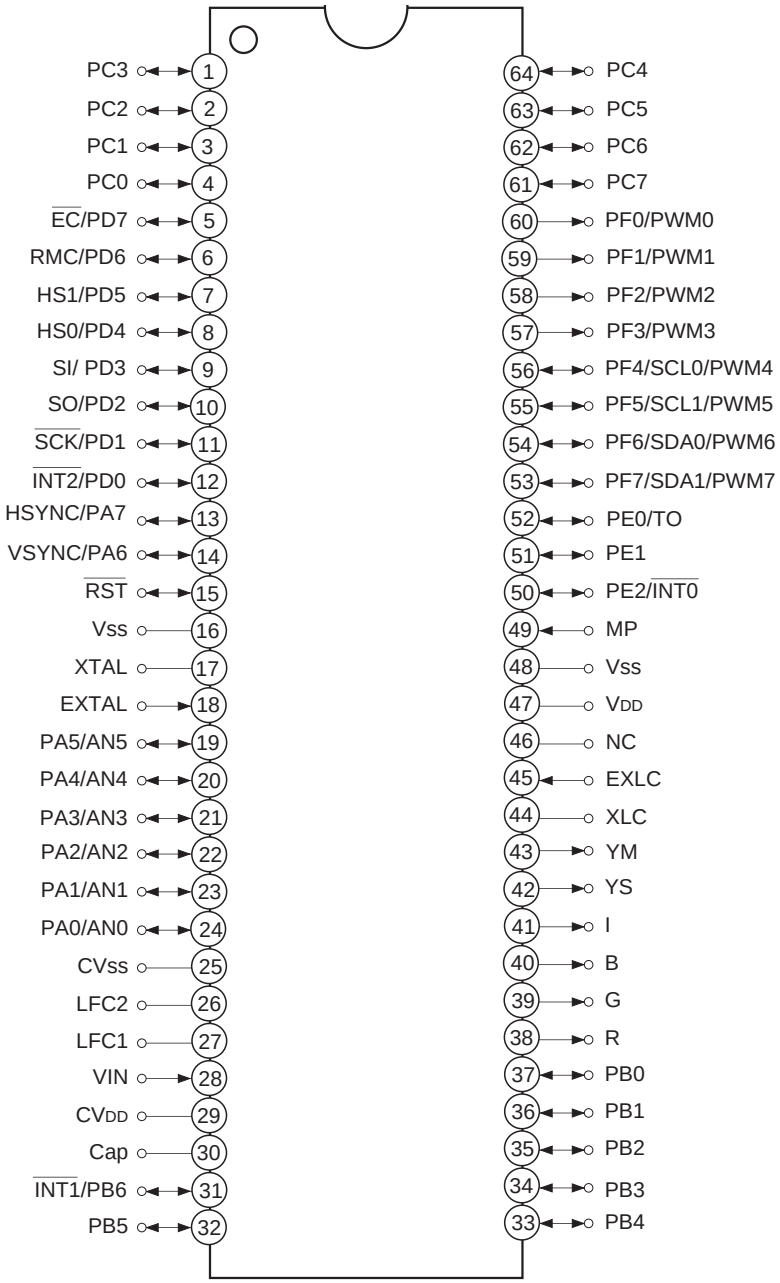
Perchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

E97739A86

Block Diagram



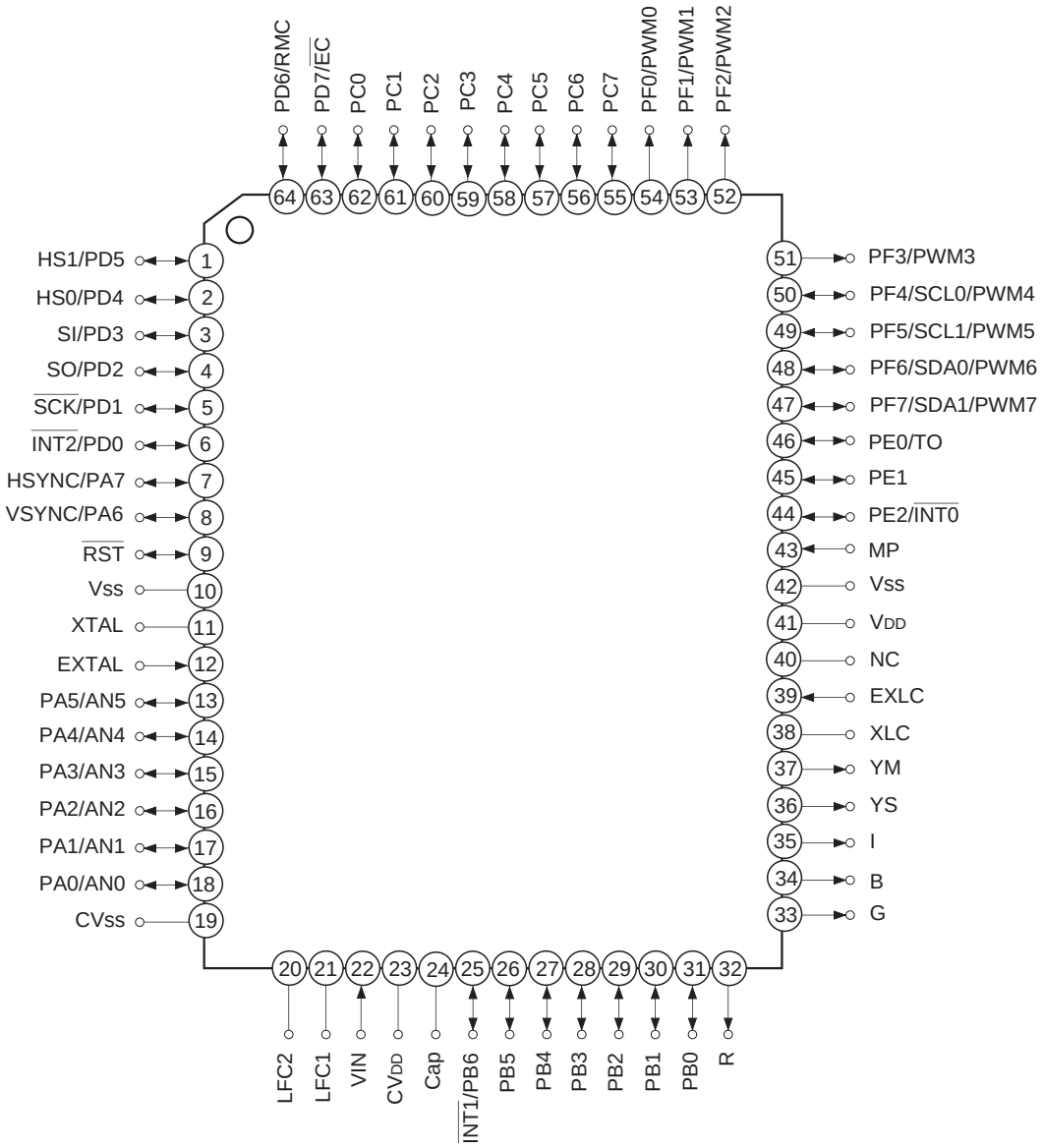
Pin Assignment (Top View) 64-pin SDIP



Note)

1. NC (Pin 46) is always connected to V_{DD}.
2. Vss (Pins 16 and 48) are both connected to GND.
3. MP (Pin 49) is always connected to GND.

Pin Assignment (Top View) 64-pin QFP



Note)

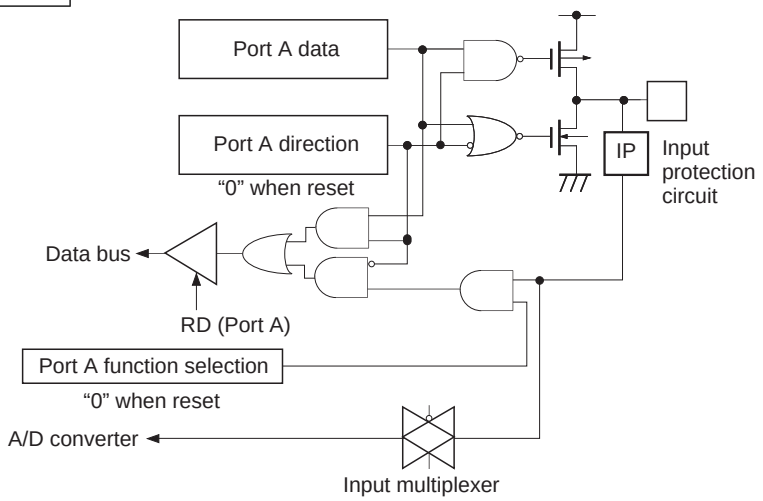
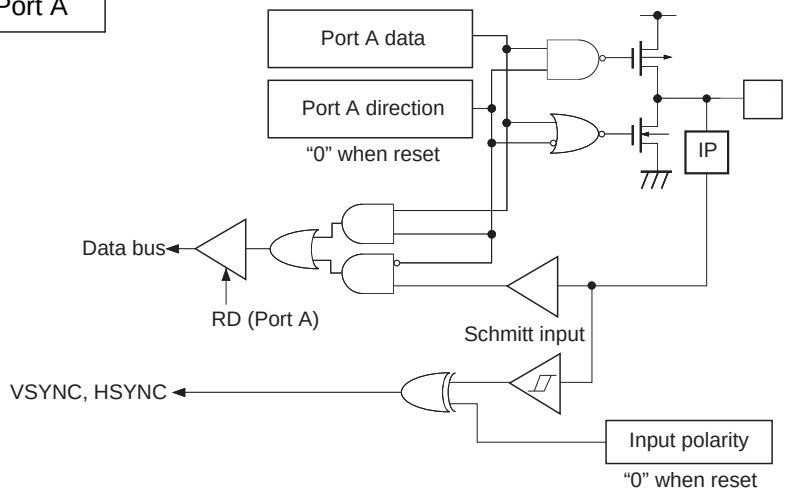
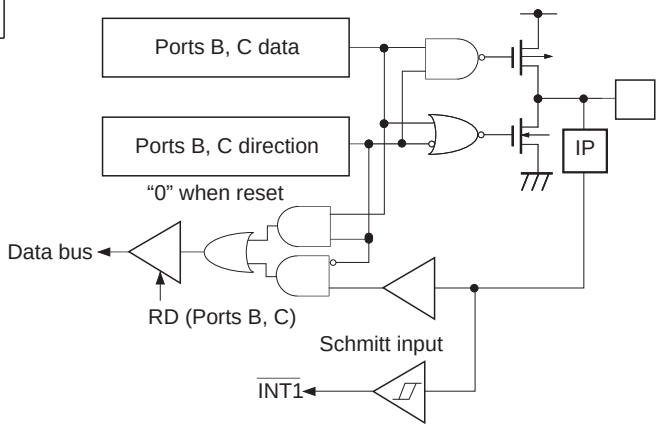
1. NC (Pin 40) is always connected to V_{DD}.
2. Vss (Pins 10 and 42) are both connected to GND.
3. MP (Pin 43) is always connected to GND.

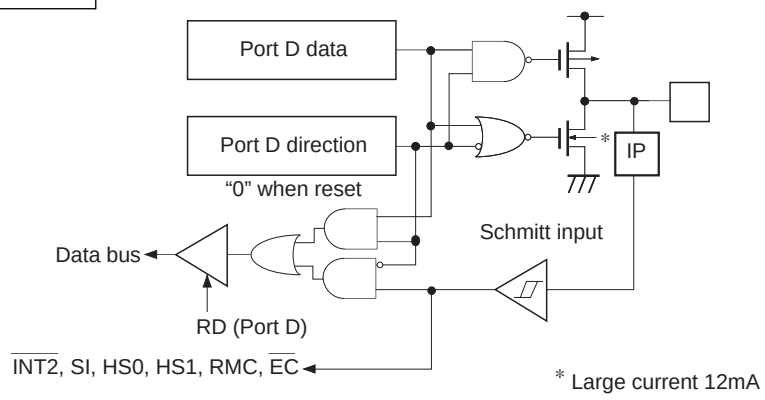
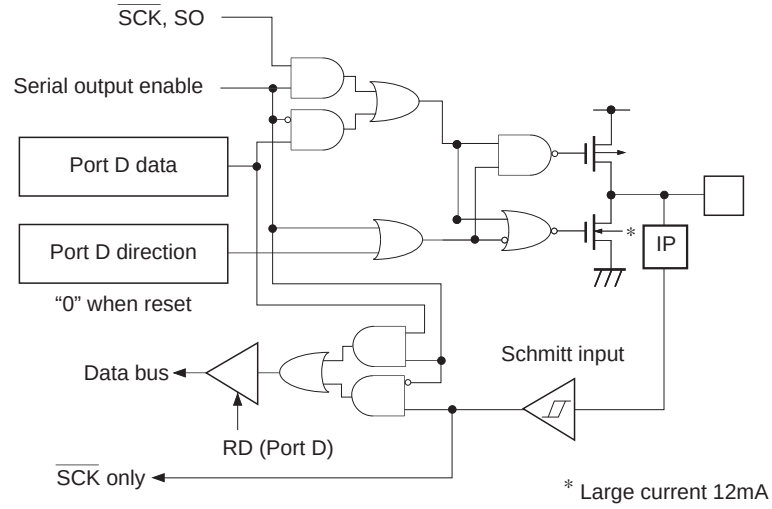
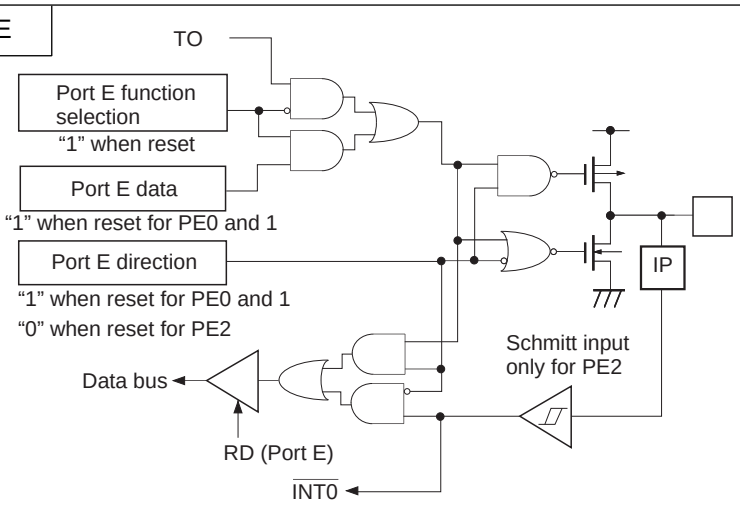
Pin Description

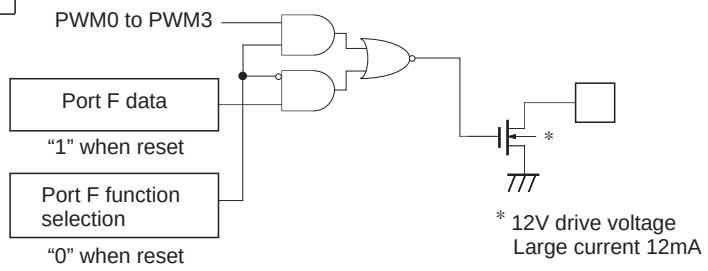
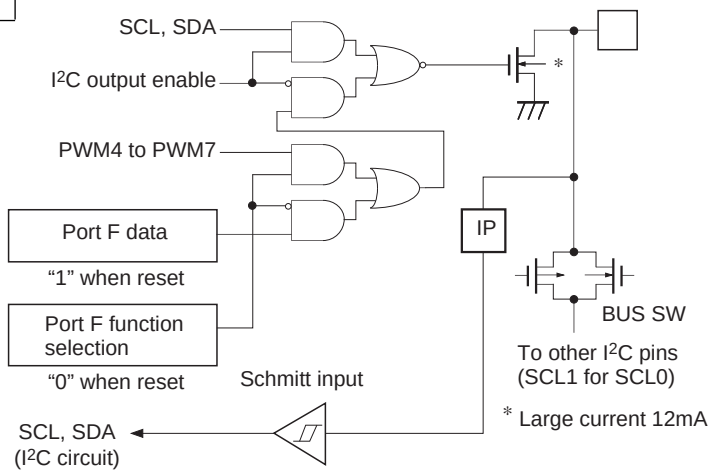
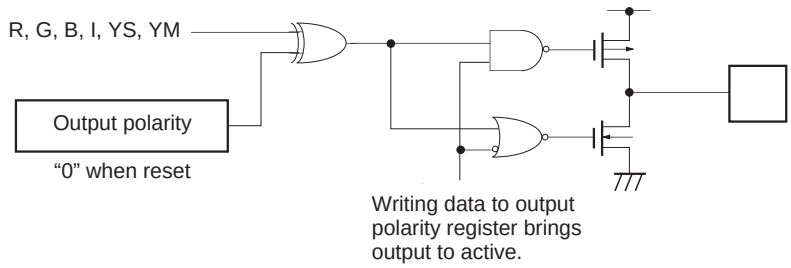
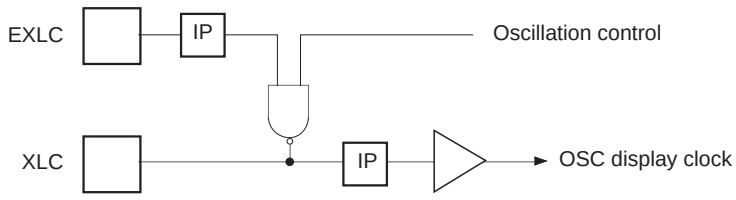
Symbol	I/O	Description	
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.
PB0 to PB5	I/O	(Port B) 7-bit I/O port. I/O can be set in a unit of single bits. (7 pins)	
PB6/$\overline{\text{INT1}}$	I/O/Input		External interruption request input. Active at the falling edge.
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/$\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA synk current. (8 pins)	External interruption request input. Active at the falling edge.
PD1/$\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.
PD6/RMC	I/O/Input		Remote control reception circuit input.
PD7/$\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.
PE0/TO	I/O/Output	(Port E) 3-bit I/O port. I/O can be set in a unit of single bits. (3 pins)	Rectangular wave output for timer/counter
PE1	I/O		
PE2/$\overline{\text{INT0}}$	I/O/Input		External interruption request input. Active at the falling edge.
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-channel open drain output. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (8 pins)
PF4/SCL0/PWM4 PF5/SCL1/PWM5	Output/I/O		I^2C bus interface transfer clock I/O. (2 pins)
PF6/SDA0/PWM6 PF7/SDA1/PWM7	Output/I/O		I^2C bus interface transfer data I/O. (2 pins)
R, G, B, I, YS, YM	Output	6-bit OSD display output. (6 pins)	

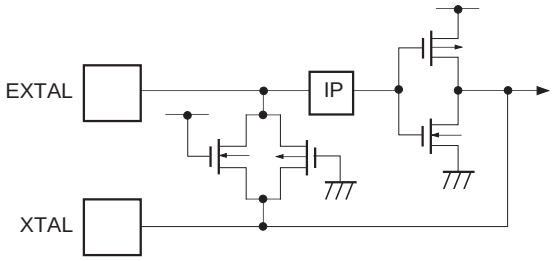
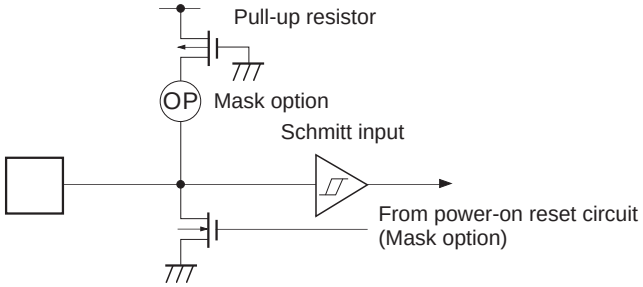
Symbol	I/O	Description
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.
XLC	Output	
VIN	Input	External composite video signal input. Input the 2Vp-p signal via a capacitor.
Cap	—	Connects a data slicer capacitor between Cap and CVss.
LFC1, LFC2	—	Connects a low-pass filter capacitor for PLL circuit between LFC1 and LFC2.
CV_{DD}		Positive power supply for data slicer.
CVss		GND for data slicer.
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL and leave XTAL open.
XTAL	Output	
$\overline{RST}$	I/O	System reset; active at Low level. I/O pin. Outputs a Low level when the power is turned on and the internal power-on reset function operates. (Mask option)
MP	Input	Test mode pin. Always connect to GND.
NC		No connected. Under normal operation, connect to V_{DD}.
V_{DD}		Positive power supply.
Vss		GND. Connect two Vss pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA5/AN5 6 pins	Port A 	Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins	Port A 	Hi-Z
PB0 to PB5 PB6/$\overline{\text{INT1}}$ PC0 to PC7 15 pins	Port B Port C 	Hi-Z

Pin	Circuit format	When reset
PD0/$\overline{INT2}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{EC}$ 6 pins	Port D  	Hi-Z
PD1/$\overline{SCK}$ PD2/SO 2 pins	Port D  	Hi-Z
PE0/TO PE1 PE2/$\overline{INT0}$ 3 pins	Port E  	PE0, PE1: High level PE2: Hi-Z

Pin	Circuit format	When reset
PF0/PWM0 to PF3/PWM3 4 pins	Port F 	Hi-Z
PF4/PWM4/SCL0 PF5/PWM5/SCL1 PF6/PWM6/SDA0 PF7/PWM7/SDA1 4 pins	Port F 	Hi-Z
R G B I YS YM 6 pins		Hi-Z
EXLC XLC 2 pins		Oscillation halted

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. (This device does not enter the stop mode.)	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	PF0 to PF3 pins
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Ports excluding large current outputs (value per pin)
	I_{OLC}	20	mA	Large current output ports (value per pin*2)
Low level total output current	$\sum I_{OL}$	100	mA	Total of all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP-64P-01
		600	mW	GFP-64P-L01

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current output port is Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.5	5.5	V	Guaranteed data hold range for stop mode*1
Data slicer supply voltage	CV_{DD}	4.5	5.5	V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	*3
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4
Operating temperature	Topr	–20	+75	°C	

*1 This device does not enter the stop mode.

*2 PA, PB, PC, PE0 to PE1, SCL0 to 1, SDA0 to 1 pins.

*3 $\overline{INT2}$, $\overline{SCK}$, SO, SI, HS0, HS1, RMC, $\overline{EC}$, $\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$ pins.

*4 Specifies only during external clock input.

*5 CV_{DD} and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC characteristics

(Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE R, G, B, I, YS, YM	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE R, G, B, I, YS, YM, PF0 to PF3, $\overline{RST}$*1	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM, $\overline{RST}$*2	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain I/O leakage current (in N-ch Tr OFF state)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (in output Tr OFF state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current	I_{DD}	V_{DD}*3	1/2 frequency dividing clock operation V_{DD} = 5.5V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		37	50	mA
	I_{DDSL}		Sleep mode V_{DD} = 5.5V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		2.5	5	mA
	I_{DDST}		Stop mode*4 V_{DD} = 5.5V, termination of 12MHz oscillation	—	—	—	µA
	I_{CVDD}	CV_{DD}	V_{DD} = 5.5V	—	5.0	10.0	mA
Input capacitance	C_{IN}	PA to PE, SCL, SDA, EXLC, EXTAL, VIN, $\overline{RST}$	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 Specifies $\overline{RST}$ pin only when the power-on reset circuit is selected with mask option.

*2 For $\overline{RST}$ pin, specifies the input current when pull-up resistor is selected, and specifies the leakage current when non-resistor is selected.

*3 When all output pins are left open. Specifies only when the OSD oscillation is halted.

*4 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2		12.0		MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys}*1 + 50			ns
Event count input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms

*1 Indicates three values according to the contents of the clock control register (CLC: 00FE$_h$) upper 2 bits (CPU clock selection).
t_{sys} (ns) = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Fig. 1. Clock timing

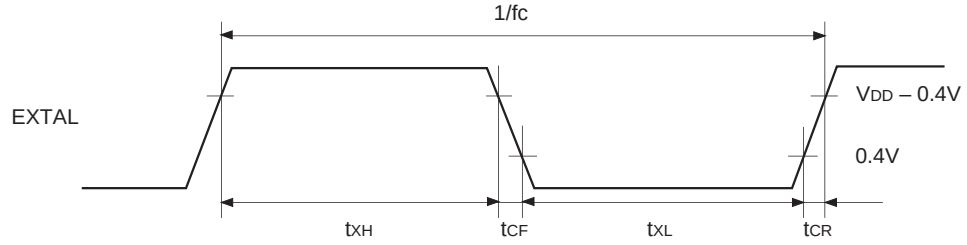


Fig. 2. Clock applied conditions

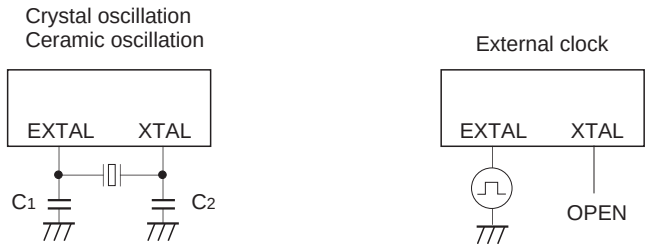
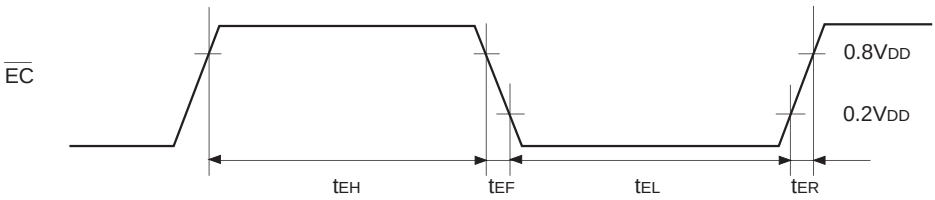


Fig. 3. Event count clock timing

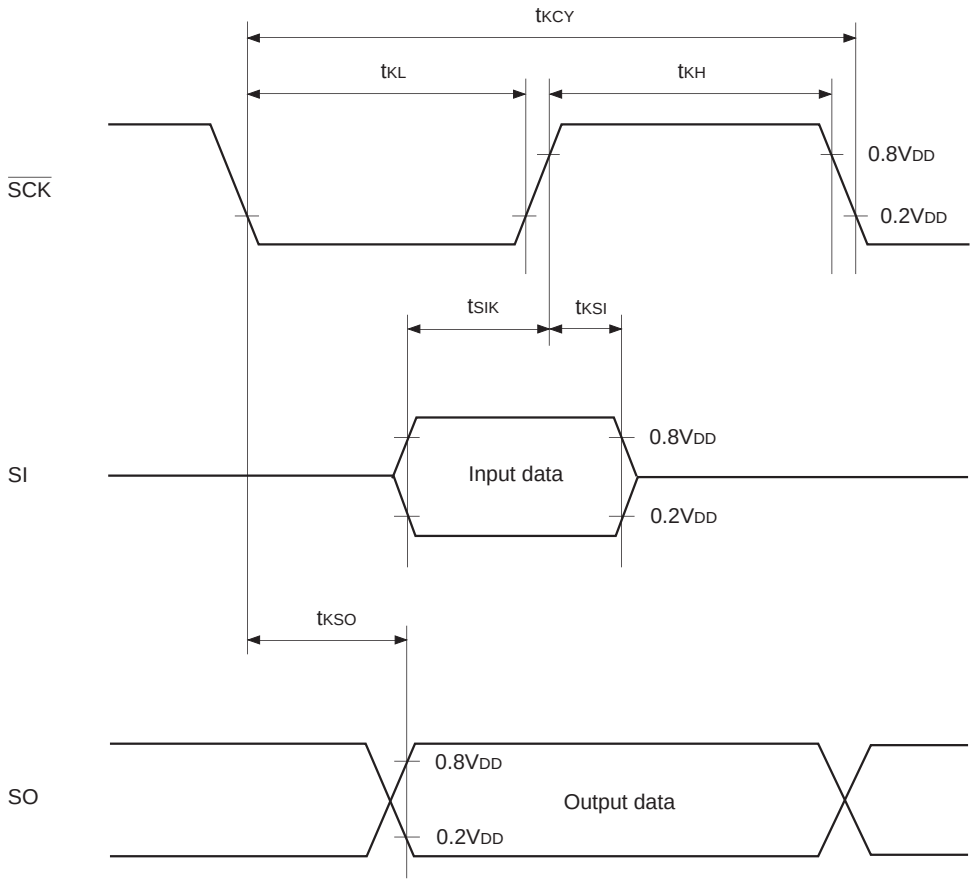


(2) Serial transfer (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50 pF + 1TTL.

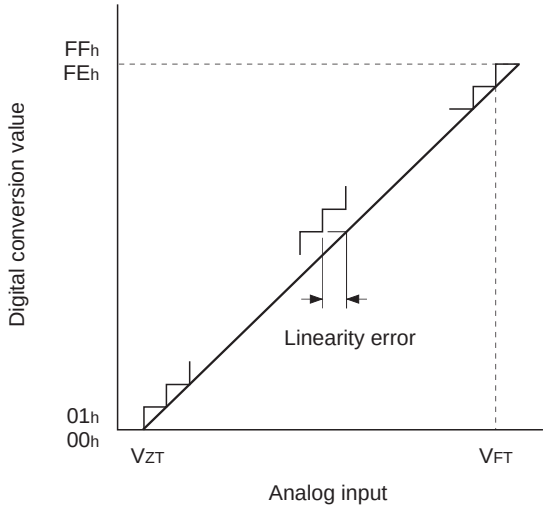
Fig. 4. Serial transfer timing



(3) A/D converter (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN5		0		V_{DD}	V

Fig. 5. Definitions of A/D converter terms



*1 V_{ZT}: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEh).

CKS / PCK1, 0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 6. Interruption input timing

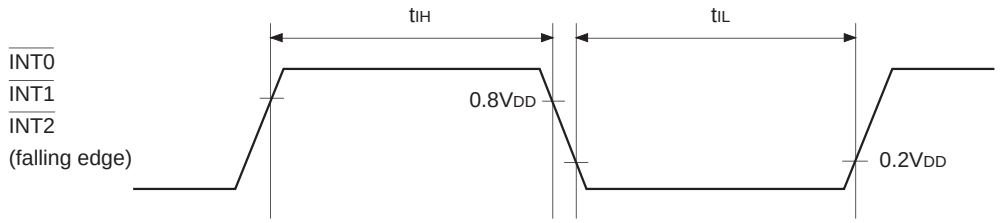
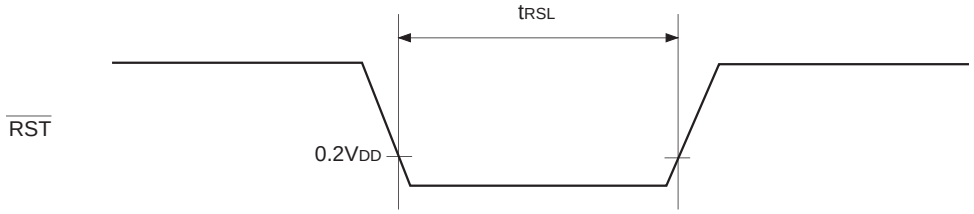


Fig. 7. $\overline{RST}$ input timing

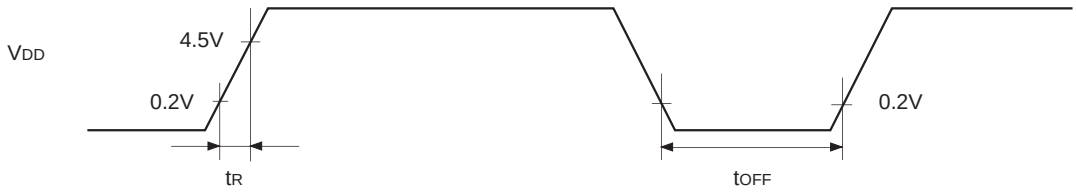


(5) Power-on reset[*1] (Ta = –25 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repeated power-on reset	1		ms

[*1] Specifies only when the power-on reset function is selected.

Fig. 8. Power-on reset



Take care when turning the power on.

(6) I²C bus timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repeated transfers	$t_{SU;\,STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		4.7		µs

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

Fig. 9. I²C bus transfer timing

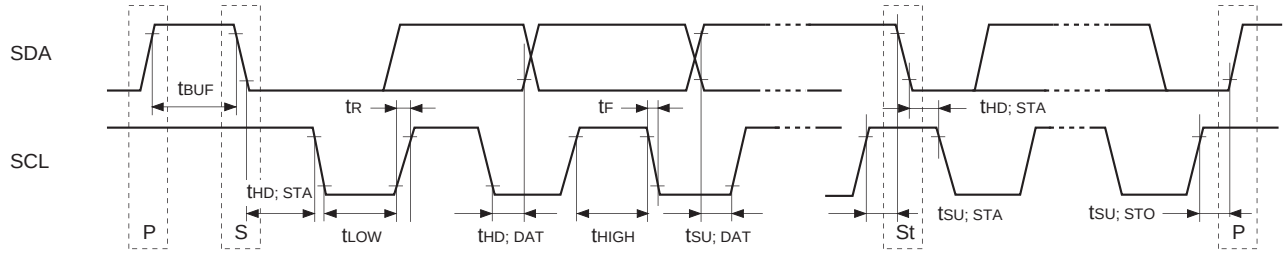
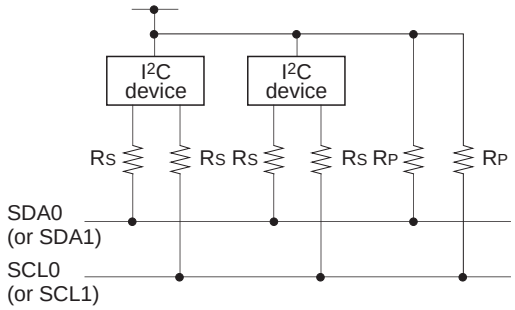


Fig. 10. I²C bus device recommended circuit



- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(7) OSD timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	16.5	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		µs
VSYNC pulse width	t_{VWD}	VSYNC	Fig. 11	1		H*
HSYNC after-write rise and fall times	t_{HCG}	HSYNC	Fig. 11		200	ns
VSYNC before-write rise and fall times	t_{VCG}	VSYNC	Fig. 11		1.0	µs

* H indicates 1HSYNC period.

Fig. 11. OSD timing

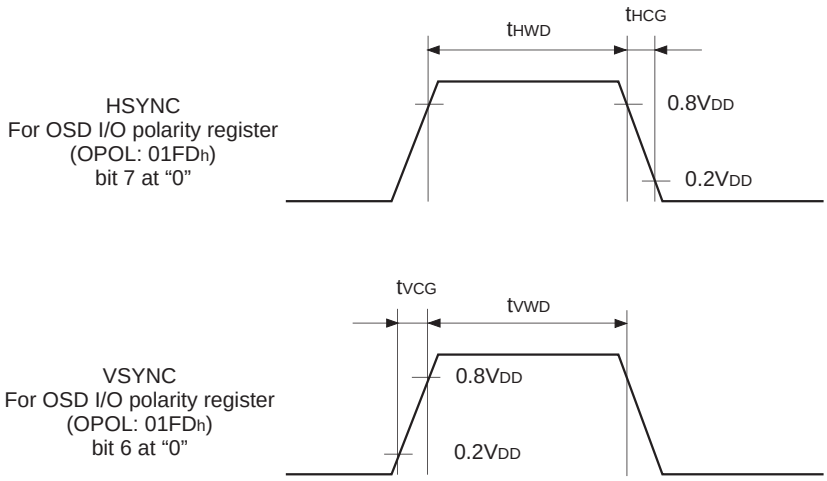
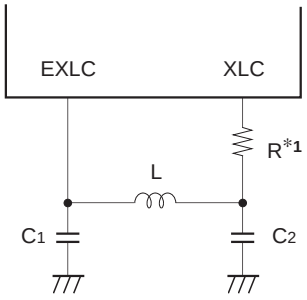


Fig. 12. LC oscillation circuit connection

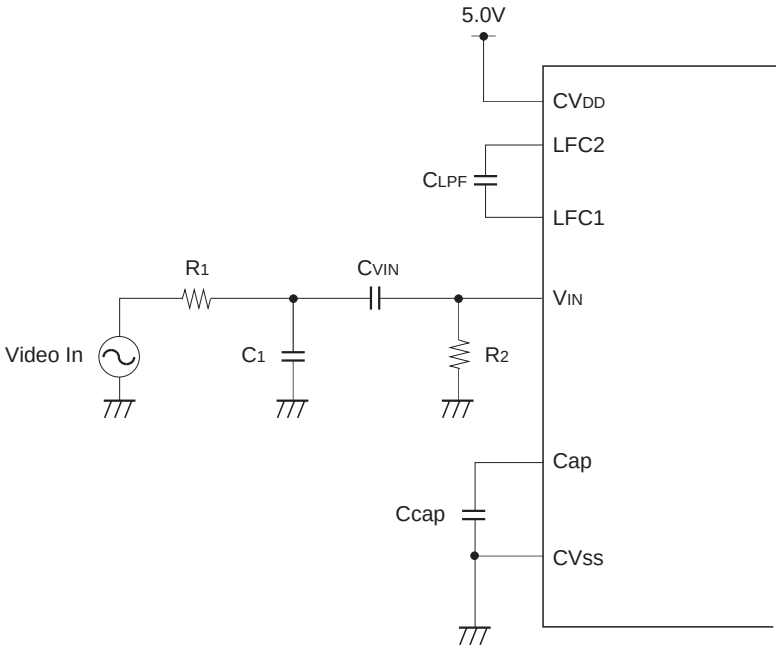


*1 The XLC series resistor can reduce the frequency of occurrence of the undesired radiation.

(8) Data slicer external circuit (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Remarks
VIN pin coupling capacitance	C_{VIN}	VIN		0.1		µF	The B characteristics or more of temperature characteristics is recommended.
Cap pin capacitance	Ccap	Cap		4700		pF	The B characteristics or more of temperature characteristics is recommended.
PLL low-pass filter capacitance	C_{LPF}	LFC1, LFC2		0.47		µF	The B characteristics or more of temperature characteristics is recommended.
Composite video signal input	Video In	VIN		2.0		Vp-p	

Fig. 13. Data slicer external recommended circuit



[Recommended Constant]

R_1 = 220Ω (error: 5%; allowable power dissipation: 1/8W or more)

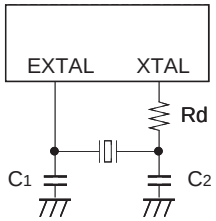
R_2 = 1MΩ (error: 5%; allowable power dissipation: 1/8W or more)

C_1 = 1200pF (ceramic), the B characteristics or more of temperature characteristics is recommended.

Appendix

Fig. 14. SPC 700 Series recommended oscillation circuit

(i)



Manufacture	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	12.0	5	5	0*1	(i)
KINSEKI LTD.	HC-19/U (-S)	12.0	15	15	0*1	(i)

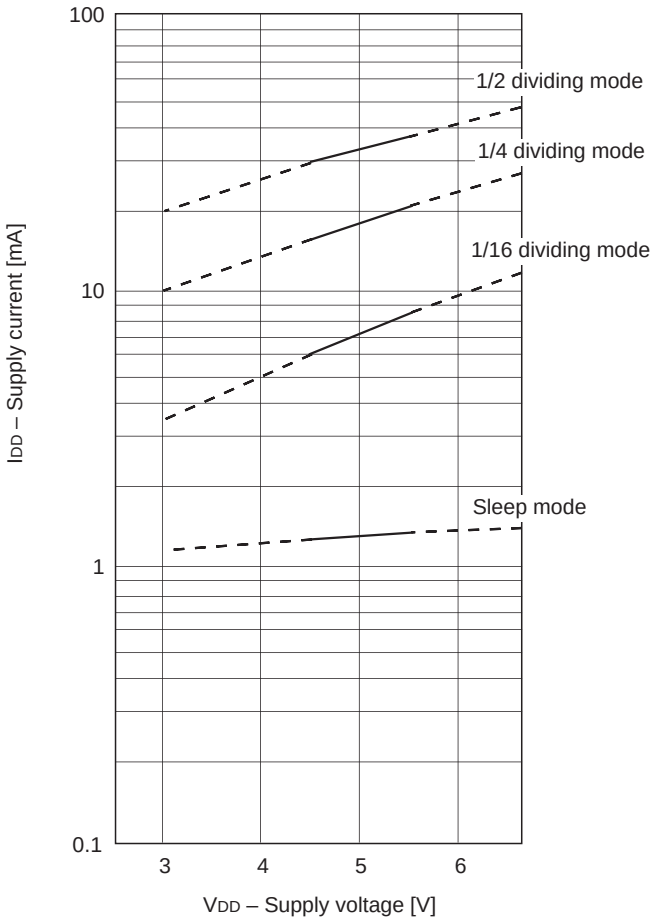
*1 The XTAL series resistor can reduce the effect of the noise caused by the electrostatic discharge.

Mask Option Table

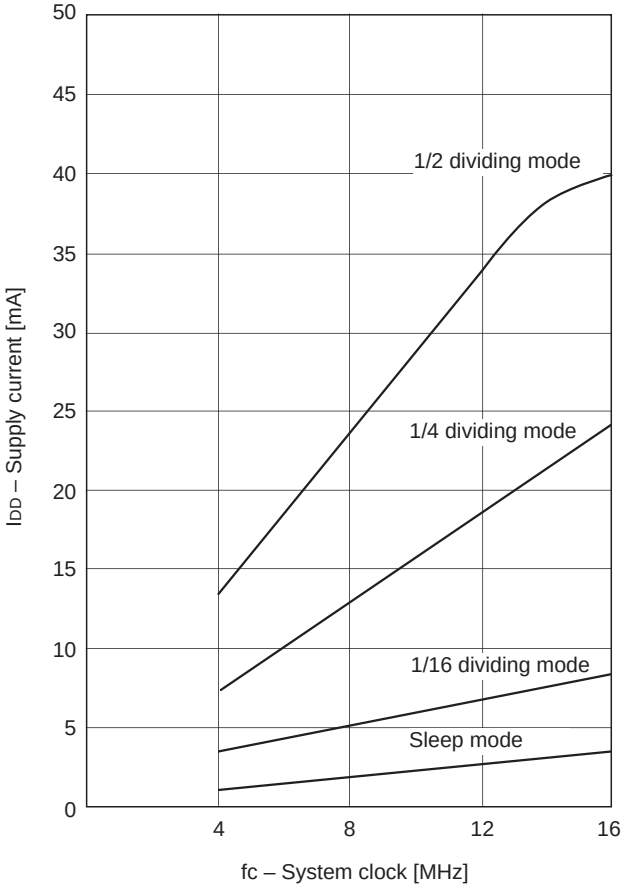
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

Fig. 15. Characteristic curves

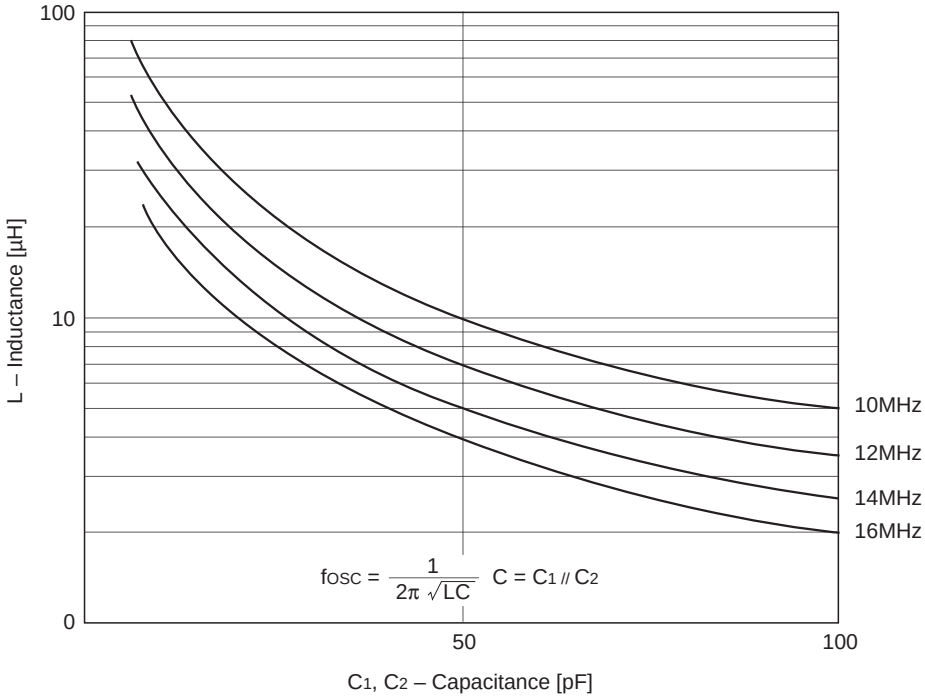
IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)



IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)

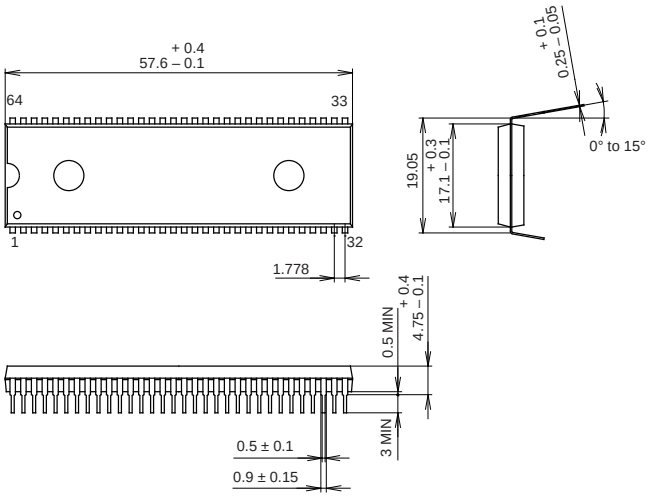


Parameter curve for OSD oscillation L vs. C
(theoretically calculated value)



Package Outline Unit: mm

64PIN SDIP (PLASTIC) 750mil

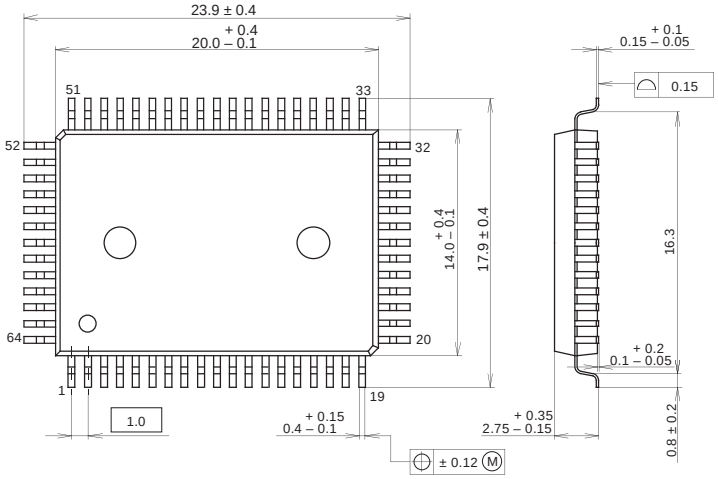


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750-A
JEDEC CODE	————

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP–64P–L01
EIAJ CODE	QFP064–P–1420
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g