IMS1421C

T-46-23-08

CMOS High Performance 4K x 4 Static RAM

Preliminary

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—1.6 Micron Design Rules
- 4K x 4 Bit Organization
- High Speed Chip Select Function
- 40nsec Address Access Times
- 30nsec Chip Select Access Time
- Fully TTL Compatible
- Common Data Input & Outputs
- Three-state Output
- 20-Pin, 300-mil CDIP
- Single +5 volt ± 10% Operation

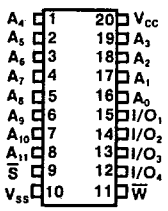
DESCRIPTION

The IMS1421C is a high performance 4K x 4 CMOS static RAM featuring fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1421C provides a Chip Select ($\overline{S}$) function which allows faster system access times to be achieved.

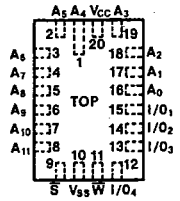
The IMS1421C provides a high reliability CMOS replacement for existing IMS1421 (NMOS) applications.

The IMS1421C is packaged in a 20-pin 300-mil ceramic DIP.

PIN CONFIGURATION

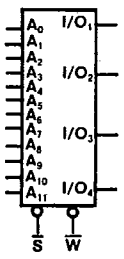


DIP

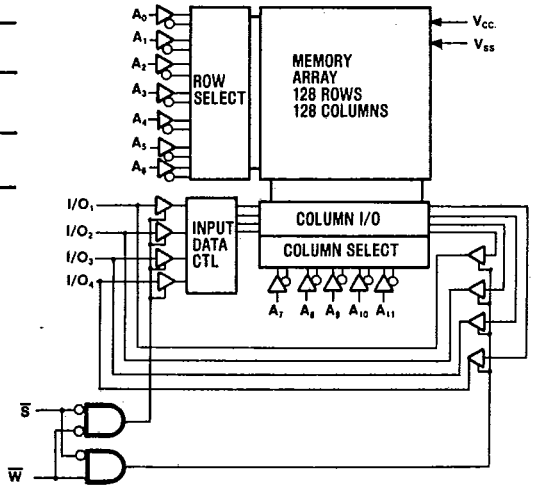


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{S}$	CHIP SELECT		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... −2.0 to 7.0V
Temperature Under Bias ..... −55°C to 125°C
Storage Temperature (Ambient) .... −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		110	mA	$t_C = t_{C(min)}$
I_{IN}	Input Leakage Current (Any Input)		10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		.4	V	$I_{OUT} = 8mA$

AC TEST CONDITIONS[a]

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load ..... See Figure 1

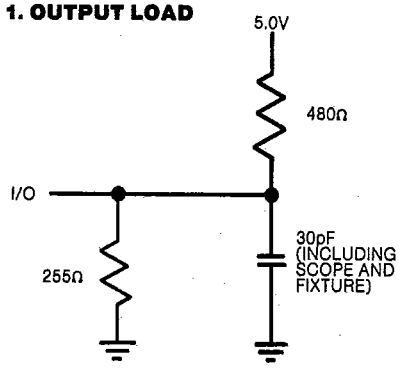
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V
C	$\overline{S}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



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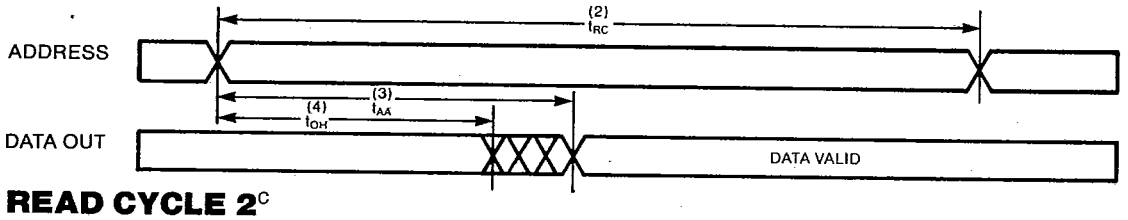
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

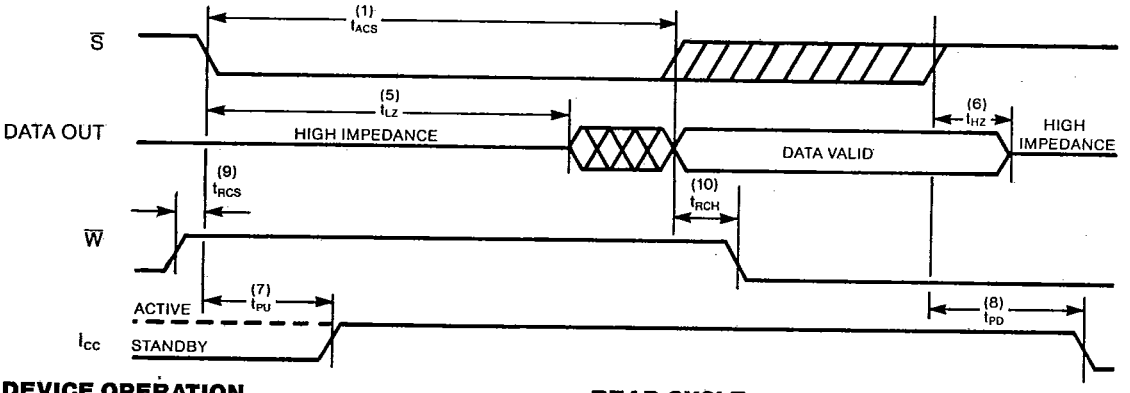
NO.	SYMBOL	PARAMETER	1421-40 MIN	1421-40 MAX	UNITS	NOTES
1	t_{ACS}	Chip Enable/Select Access Time		30	ns	
2	t_{RC}	Read Cycle Time	40		ns	c
3	t_{AA}	Address Access Time		40	ns	d
4	t_{OH}	Output Hold After Address Change	3		ns	
5	t_{LZ}	Chip Select to Output Active	20		ns	
6	t_{HZ}	Chip Select to Output Disable		20	ns	f
7	t_{PU}	Chip Enable to Power Up	NA		ns	
8	t_{PD}	Chip Disable to Power Down		NA	ns	
9	t_{RCS}	Read Command Set-Up Time	−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		ns	
	t_T	Input Rise and Fall Times		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{S}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1421C has two control inputs, Chip Select ($\overline{S}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines. The $\overline{S}$ function controls chip selection but there is no power down function on the IMS1421. The IMS1421 is designed to allow high system performance by removing the Chip Select decoder delay from the critical access delay path.

With $\overline{S}$ high, the device is selected and the outputs are disabled.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{S} \leq V_{IL}$ max. Read access time is measured from either $\overline{S}$ going low or from valid address. If $\overline{S}$ goes low within 10ns of address valid, access time is equal to address access time. If $\overline{S}$ goes low later than 10ns after address valid, then access time is equal to Chip Select access time.

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RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

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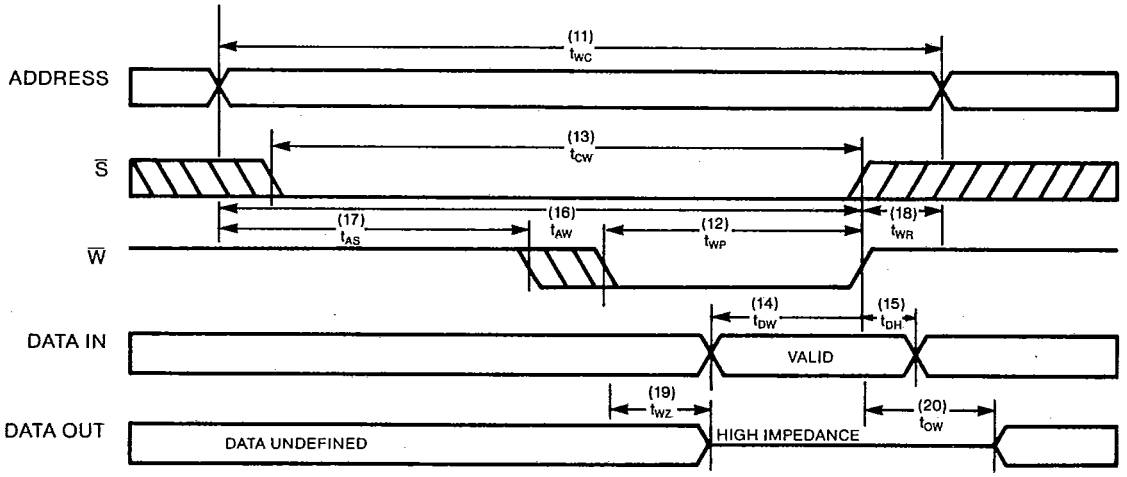
NO.	SYMBOL	PARAMETER	1421-40 MIN	1421-40 MAX	UNITS	NOTES
11	t_{WC}	Write Cycle Time	40		ns	
12	t_{WP}	Write Pulse Width	35		ns	
13	t_{CW}	Chip Select to End of Write	30		ns	
14	t_{DW}	Data Set-up to End of Write	15		ns	
15	t_{DH}	Data Hold After End of Write	3		ns	
16	t_{AW}	Address Set-up to End of Write	40		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		ns	
18	t_{WR}	Address Hold After End of Write	5		ns	
19	t_{WZ}	Write Enable to Output Disable		20	ns	f
20	t_{OW}	Output Active After End of Write	8		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{S}$ goes low with $\overline{W}$ low, Output remains in high impedance state.
Note h: $\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



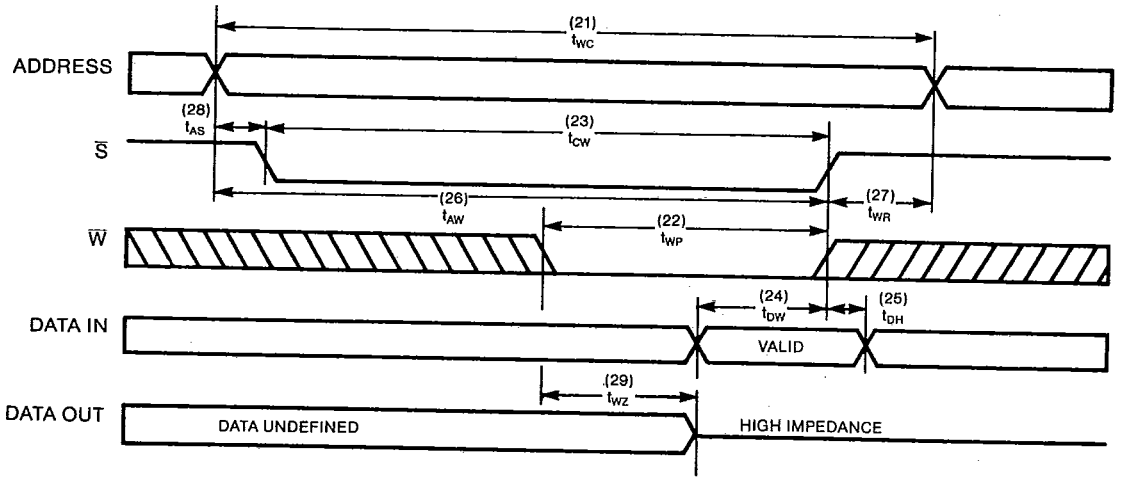
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{S}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1421-40 MIN	1421-40 MAX	UNITS	NOTES
21	t_{WC}	Write Cycle Time	40		ns	
22	t_{WP}	Write Pulse Width	35		ns	
23	t_{CW}	Chip Select to End of Write	30		ns	
24	t_{DW}	Data Set-up to End of Write	15		ns	
25	t_{DH}	Data Hold After End of Write	5		ns	
26	t_{AW}	Address Set-up to End of Write	35		ns	
27	t_{WR}	Address Hold After End of Write	5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	0		ns	
29	t_{WZ}	Write Enable to Output Disable		20	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{S}$ going low and is terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{S}$ (WRITE CYCLE 2) going high. During a write cycle, the outputs are floated and the data on the inputs is written into the addressed memory cells.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{S}$ going low, the address must be stable for the specified WRITE CYCLE 2 set-up time. WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high and $\overline{S}$ low, the outputs become active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by the rising edge of $\overline{S}$. Data set-up and hold times are referenced to the rising edge of $\overline{S}$, and the outputs remain in the high impedance state.

APPLICATION

Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1421C Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1421C. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1421C are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the back-plane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

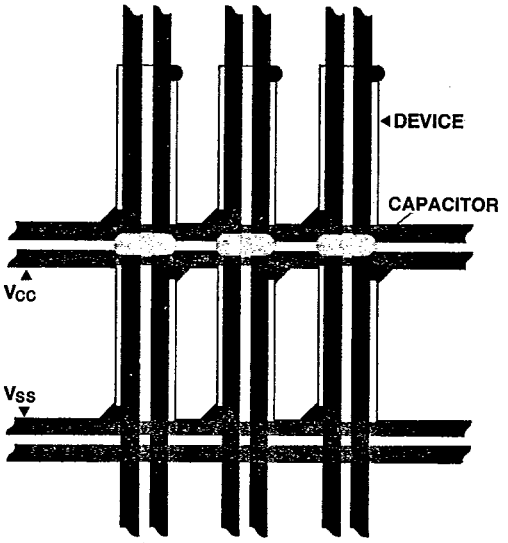
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board providing a quiet environment free of noise spikes and signal reflections.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1421C	40ns	CERAMIC DIP	IMS1421SC-40