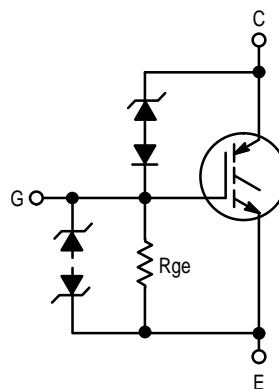


Advanced Information
SMARTDISCRETES™
Internally Clamped, N-Channel
IGBT

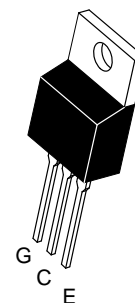
This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability



MGP20N35CL

20 AMPERES
VOLTAGE CLAMPED
N-CHANNEL IGBT
V_{CE(on)} = 1.8 VOLTS
350 VOLTS (CLAMPED)



CASE 221A-09
STYLE 9
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	CLAMPED	V _{dc}
Collector–Gate Voltage	V _{CGR}	CLAMPED	V _{dc}
Gate–Emitter Voltage	V _{GE}	CLAMPED	V _{dc}
Collector Current — Continuous @ T _C = 25°C	I _C	20	A _{dc}
Reversed Collector Current – pulse width < 100 μs	I _{CR}	12	A _{pk}
Total Power Dissipation @ T _C = 25°C (TO-220)	P _D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO-220) — Junction to Ambient	R _{θJC} R _{θJA}	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T _J = 25°C @ Starting T _J = 150°C	E _{AS}	550 150	mJ
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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MGP20N35CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage (I _{Clamp} = 10 mA, T _J = -40 to 150°C)	V _{(BR)CES}	320	350	380	Vdc
Zero Gate Voltage Collector Current (V _{CE} = 250 V, V _{GE} = 0 V, T _J = 125°C) (V _{CE} = 15 V, V _{GE} = 0 V, T _J = 125°C)	I _{CES}	— —	— —	1.0 200	mA μA
Resistance Gate-Emitter (T _J = -40 to 150°C)	R _{GE}	10k	16k	30k	Ω
Gate-Emitter Breakdown Voltage (I _G = 2 mA)	V _{(BR)GES}	11	13	15	± V
Collector-Emitter Reverse Leakage (V _{CE} = -15 V, T _J = -40 to 150°C)	I _{ECS}	—	8	100	mA
Collector-Emitter Reversed Breakdown Voltage (I _E = 75 mA)	V _{(BR)ECS}	26	40	120	V

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1 mA) (V _{CE} = V _{GE} , I _C = 1 mA, T _J = 150°C)	V _{GE(th)}	1.0 0.75	1.7 —	2.4 1.8	V
Collector-Emitter On-Voltage (V _{GE} = 5 V, I _C = 5 A) (V _{GE} = 5 V, I _C = 10 A) (V _{GE} = 5 V, I _C = 10 A, T _J = 150°C)	V _{CE(on)}	— — —	1.1 1.4 1.4	1.4 1.9 1.8	V
Forward Transconductance (V _{CE} > 50 V, I _C = 10 A)	g _{fe}	10	16	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	2800	—	pF
Output Capacitance		C _{oes}	—	200	—	
Transfer Capacitance		C _{res}	—	25	—	

SWITCHING CHARACTERISTICS (1)

Total Gate Charge	(V _{CC} = 280 V, I _C = 20 A, V _{GE} = 5 V)	Q _g	—	45	80	nC
Gate-Emitter Charge		Q _{ge}	—	8.0	—	
Gate-Collector Charge		Q _{gc}	—	20	—	
Turn-Off Delay Time	(V _{CC} = 320 V, I _C = 20 A, L = 200 μH, R _G = 1 KΩ)	t _{d(off)}	—	TBD	TBD	μs
Fall Time		t _f	—	TBD	TBD	
Turn-On Delay Time	(V _{CC} = 14 V, I _C = 20 A, L = 200 μH, R _G = 1 KΩ)	t _{d(on)}	—	TBD	TBD	μs
Rise Time		t _r	—	TBD	TBD	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

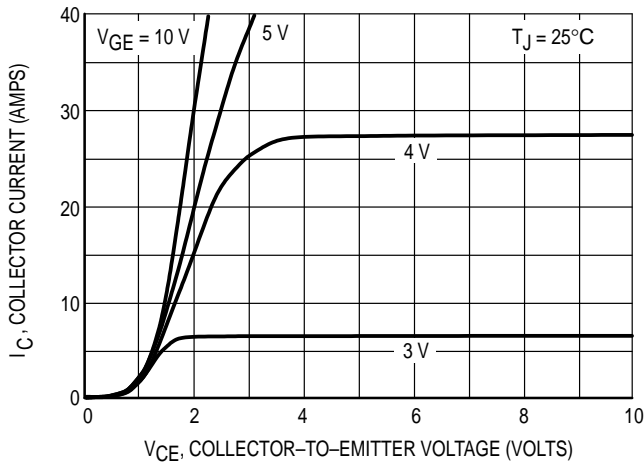


Figure 1. Output Characteristics

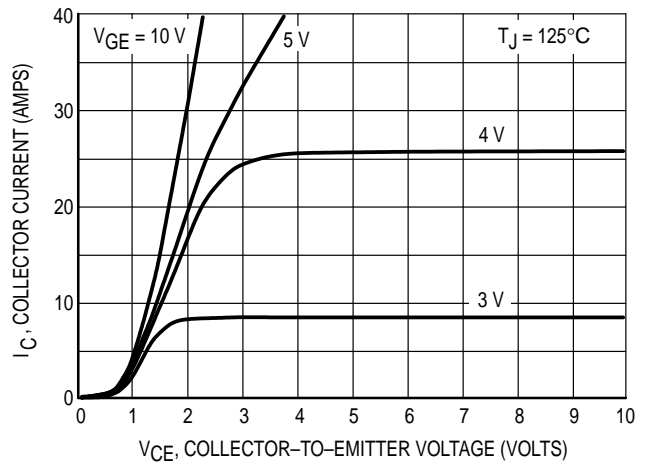


Figure 2. Output Characteristics

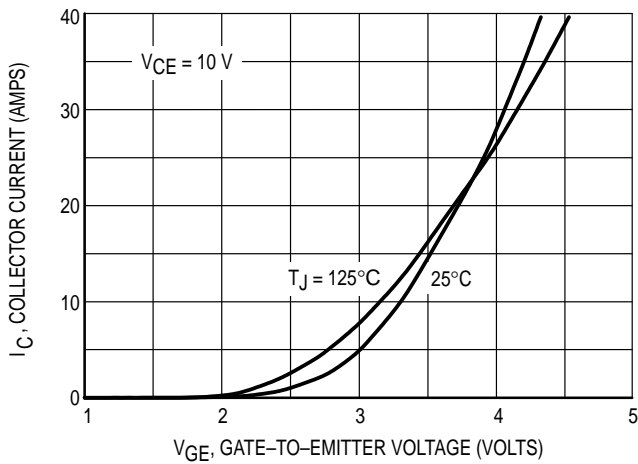


Figure 3. Transfer Characteristics

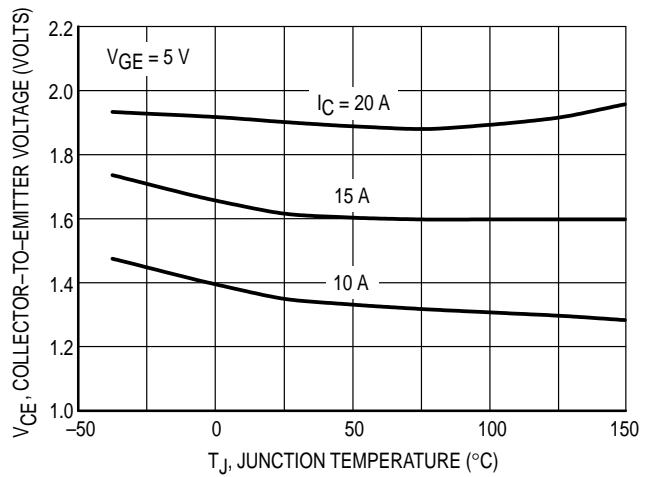


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

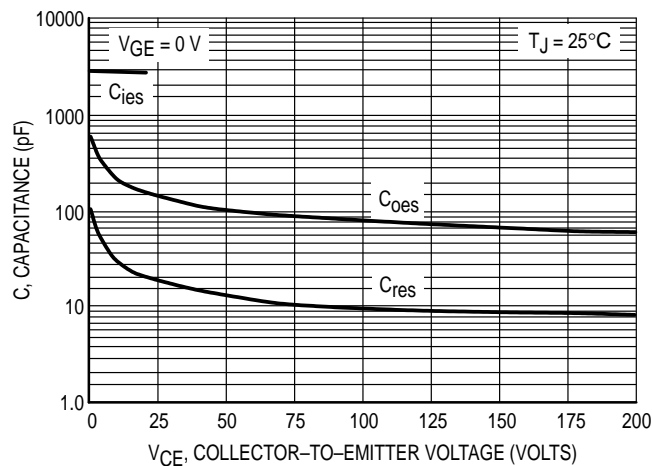


Figure 5. Capacitance Variation

MGP20N35CL

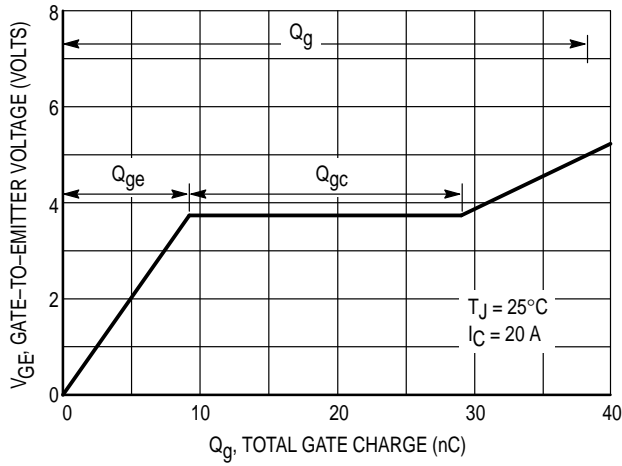


Figure 6. Gate-to-Emitter Voltage versus Total Charge

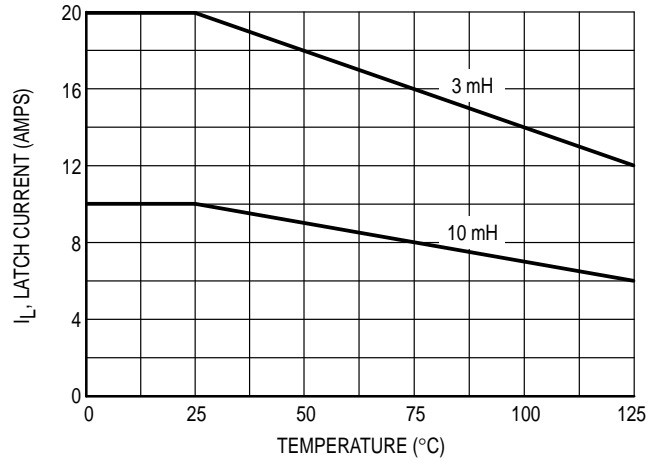


Figure 7. Latch Current versus Temperature

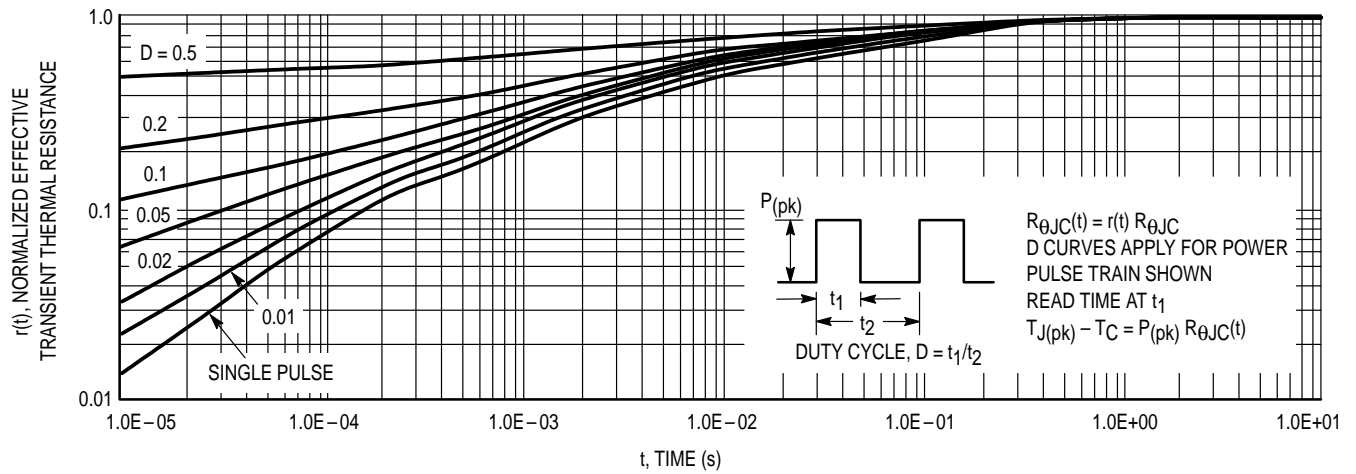
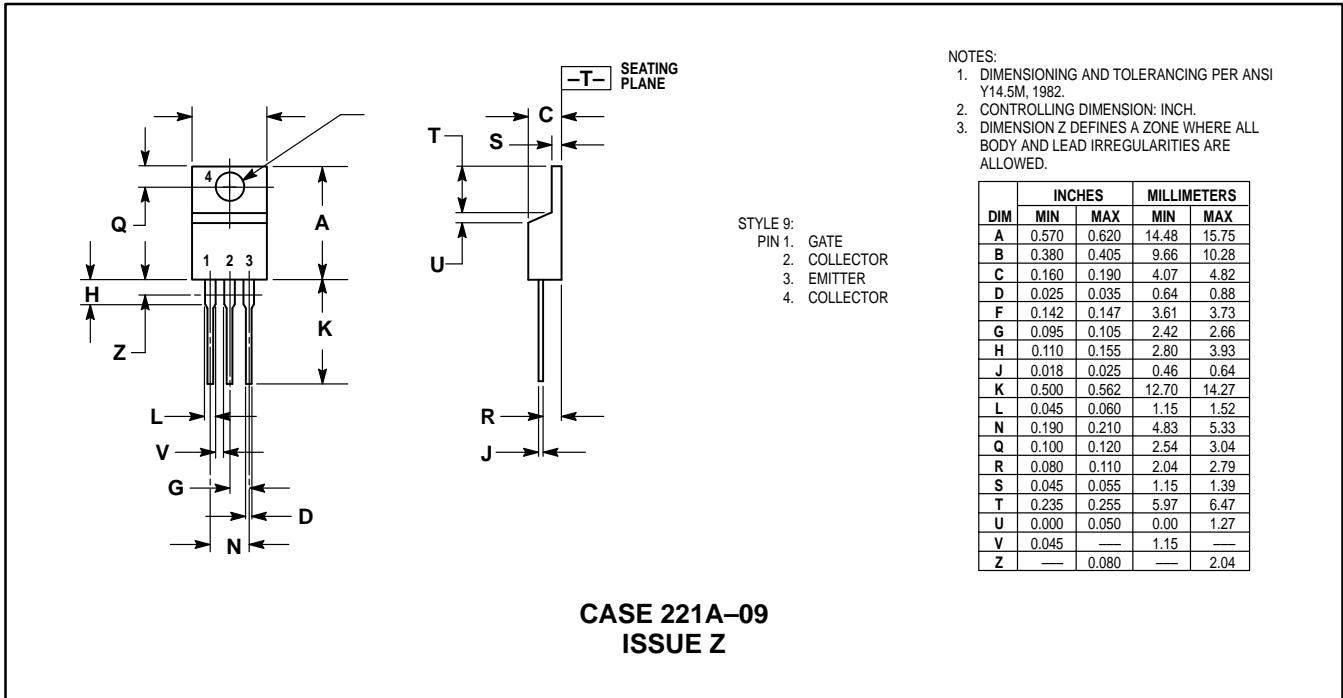


Figure 8. Thermal Response

PACKAGE DIMENSIONS



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