Preliminary

OKI Semiconductor

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MSM9210

32-Bit Duplex/Triplex (1/2 duty / 1/3 duty) VF Controller/Driver with Digital Dimming

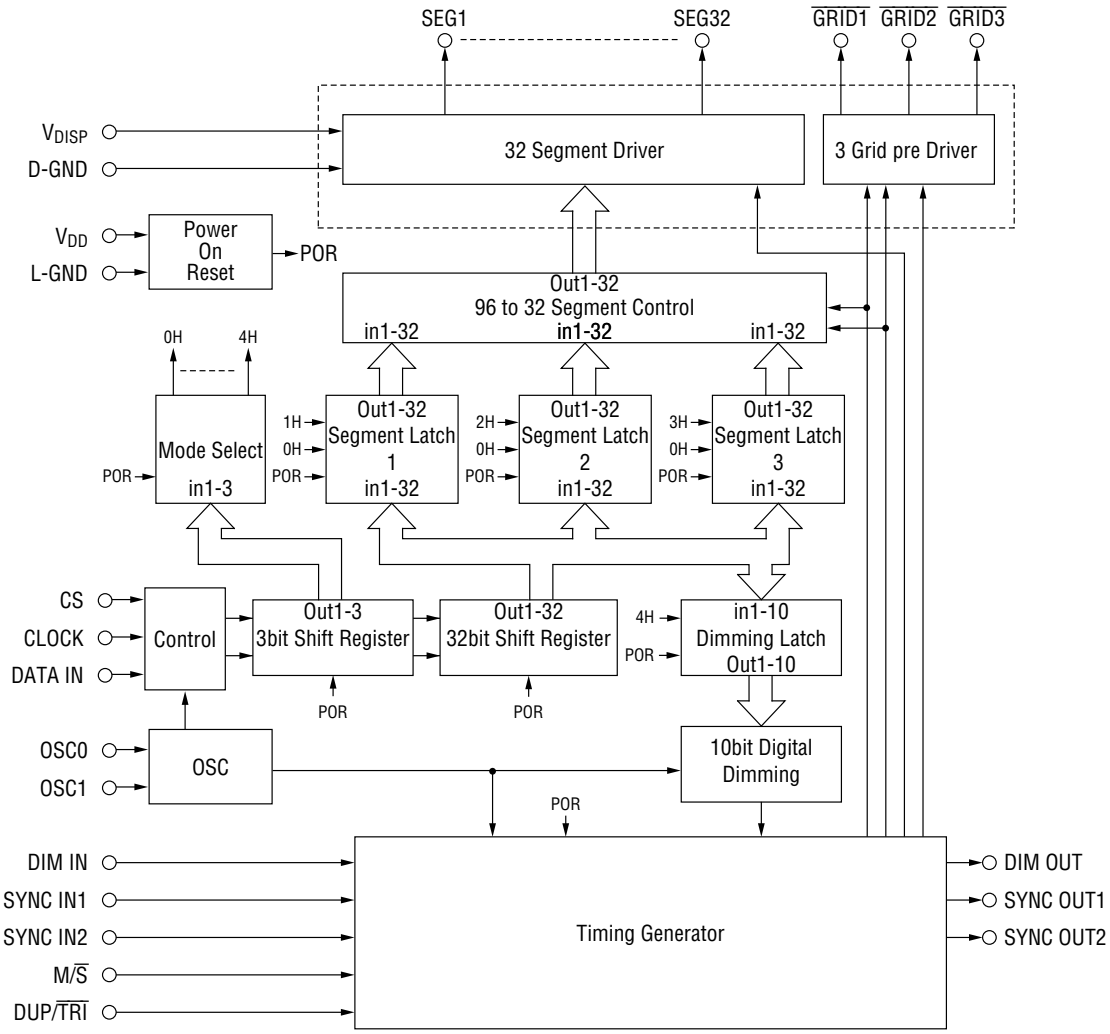
GENERAL DESCRIPTION

The MSM9210 is a full CMOS controller/driver for Duplex or Triplex (1/2 duty or 1/3 duty) vacuum fluorescent display tube. It consists of a 32-segment driver multiplexed to drive up to 96 segments, and 10-bit digital dimming circuit.
MSM9210 features a selection of a master mode and a slave mode, and therefore it can be used to expand segments for the VFD driver with keyscan and A/D converter function.
MSM9210 provides an interface with a microcontroller only by three signal lines: DATA IN, CLOCK and CS.

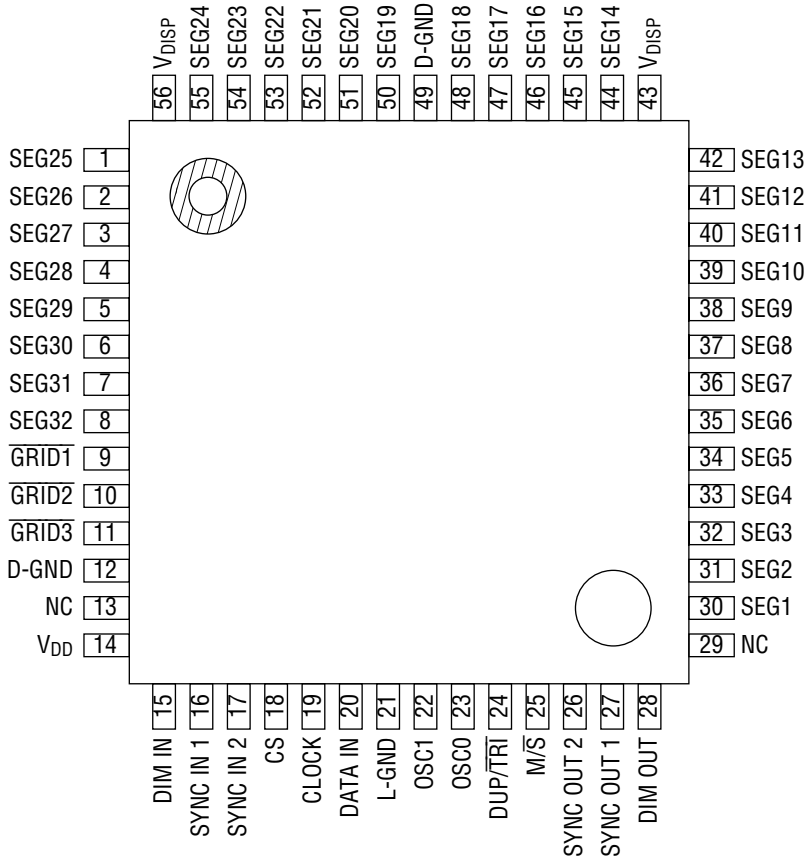
FEATURES

- Logic supply voltage (V_{DD}) : 4.5 to 5.5V
- Driver supply voltage (V_{DISP}) : 8 to 18V
- Duplex/Triplex (1/2 duty / 1/3 duty) selectable
- Master/Slave selectable
- Applicable VF tube : 2 Grids × 32 Anodes VF tube
  : 3 Grids × 32 Anodes VF tube
- 32-segment driver outputs : I_{OH}=–5mA at V_{OH}=V_{DISP}–0.8V (SEG1 to 22)
  : I_{OH}=–10mA at V_{OH}=V_{DISP}–0.8V (SEG23 to 32)
- 3-grid pre-driver outputs : I_{OL}=10mA at V_{OL}=2V
- Built-in digital dimming circuit (10-bit resolution)
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) Product name: MSM9210GS-2K

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



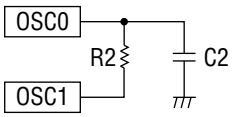
NC: No connection

56-pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Pin	Type	Description
V_{DISP}	43,56	—	Power supply pins for VF driver circuit. 43 pin and 56 pin should be connected externally.
V_{DD}	14	—	Power supply pin for logic drive.
D-GND	12, 49	—	D-GND is ground pin for the VF driver circuit. L-GND is ground pin for the logic circuit. 12pin, 21pin and 49pin should be connected externally.
L-GND	21	—	
SEG1 to 22	30 to 42, 44 to 53	O	Segment (anode) signal output pins for a VF tube. These pins can be directly connected to the VF tube. External circuit is not required. IOH≤5mA
SEG23 to 32	54, 55, 57 to 8	O	Segment (anode) signal output pins for a VF tube.These pins can be directly connected to the VF tube. External circuit is not required. IOH≤10mA
$\overline{GRID1 \text{ to } 3}$	9, 10, 11	O	Inverted Grid signal output pins. For pre-driver, the external circuit is required. IOL≤10mA
CS	18	I	Chip select input pin. Data is not transferred when CS is set to a "L" level.
CLOCK	19	I	Serial clock input pin. Serial data shifts at the rising edge of the CLOCK.
DATA IN	20	I	Serial data input pin. Data is input to the shift register at the rising edge of the serial clock.
DUP/$\overline{TRI}$	24	I	Duplex/Triplex operation select input pin. Duplex (1/2 duty) operation is selected when this pin is set to V_{DD}. Connect this pin to V_{DD} when 1/2 duty VF tube is driven. Triplex (1/3 duty) operation is selected when this pin is set to L-GND.
M/$\overline{S}$	25	I	Master/Slave mode select input pin. Master mode is selected when this pin is set to V_{DD}. Slave mode is selected when this pin is set to L-GND.
DIM IN	15	I	Dimming pulse input. When the slave mode is selected, the pulse width of the all segment output are controlled by a input pulse width of DIM IN. Connect this pin to the master side DIM OUT pin at the slave mode. When the master mode is selected, the input level of this pin is ignored and the pulse width of the all grids and segment outputs are controlled by a built-in 10-bit dimming circuit. Connect this pin to V_{DD} or L-GND at the master mode.
SYNC IN 1, 2	16, 17	I	Synchronous signal input. When the slave mode is selected, connect these pins to the master side SYNC OUT 1, 2 pins. When the master mode is selected, the input level of these pins are ignored. Connect these pins to V_{DD} or L-GND at the master mode.
DIM OUT	28	O	Dimming pulse output. When two this driver ICs are used, connect this pin to the slave side DIM IN pin.

Symbol	Pin	Type	Description
SYNC OUT 1, 2	26, 27	O	Synchronous signal output. When two this driver ICs are used, connect these pins to the slave side SYNC IN 1, 2 pin.
OSC0	23	I	RC oscillator connecting pins. Connect a resistor (R2) between the OSC1 and OSC0 pins and a capacitor (C2) between the OSC0 pin and the ground. Oscillation frequency is 3.3MHz.
OSC1	22	O	



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Ratings	Unit
Driver Supply Voltage	V_{DISP}	—	–0.3 to 20	V
Logic Supply Voltage	V_{DD}	—	–0.3 to 6.5	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta=85°C	360	mW
Storage Temperature	T_{STG}	—	–65 to 150	°C
Output Current	I_{O1}	SEG1 to 22	–10.0 to 2.0	mA
	I_{O2}	SEG23 to 32	–20.0 to 2.0	mA
	I_{O3}	$\overline{GRID1\sim3}$	–2.0 to 20.0	mA
	I_{O4}	DIM OUT, SYNC OUT1, SYNC OUT2	–2.0 to 2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Driver Supply Voltage	V_{DISP}	—		8.0	13.0	18.0	V
Logic Supply Voltage	V_{DD}	—		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}	All inputs except OSC0		0.8V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All inputs except OSC0		—	—	0.2V_{DD}	V
Clock Frequency	f_C	—		—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	R2=4.7kΩ, C2=10pF		2.6	3.3	4.0	MHz
Frame Frequency	f_{FR}	R2=4.7kΩ	1/3 Duty	211	269	325	Hz
		C2=10pF	1/2 Duty	317	403	488	Hz
Operating Temperature	T_{OP}	—		–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

Ta=–40 to 85°C, V_{DISP} =8.0 to 18.0V, V_{DD}=4.5 to 5.5V

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		$0.8V_{DD}$	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	$0.2V_{DD}$	V
High Level Input Current	I_{IH}	*1)	$V_{IH}=V_{DD}$		–1.0	1.0	µA
Low Level Input Current	I_{IL}	*1)	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	SEG1-22	V_{DISP}=9.5V	I_{OH1}=–5mA	V_{DISP}–0.8	—	V
	V_{OH2}	SEG23-32		I_{OH2}=–10mA	V_{DISP}–0.8	—	V
	V_{OH3}	$\overline{\text{GRID1-3}}$		I_{OH3}=–5mA	V_{DISP}–0.8	—	V
	V_{OH4}	*2)	V_{DD}=4.5V	I_{OH4}=–200µA	V_{DD}–0.8	—	V
Low Level Output Voltage	V_{OL1}	SEG1-22	V_{DISP}=9.5V	I_{OL1}=500µA	—	2.0	V
	V_{OL2}	SEG23-32		I_{OL2}=500µA	—	2.0	V
	V_{OL3}	$\overline{\text{GRID1-3}}$		I_{OL3}=10mA	—	2.0	V
	V_{OL4}	*2)	V_{DD}=4.5V	I_{OL4}=200µA	—	0.8	V
Supply Current	I_{DISP}	V_{DISP}	f_{OSC}=3.3MHz, no Load		—	10	mA
	I_{DD}	V_{DD}	f_{OSC}=3.3MHz, no Load		—	8	mA

*1) CS, CLOCK, DATA IN, DIM IN, SYNC IN 1, SYNC IN 2, M/$\overline{\text{S}}$, DUP/$\overline{\text{TRI}}$
*2) DIM OUT, SYNC OUT 1, SYNC OUT 2

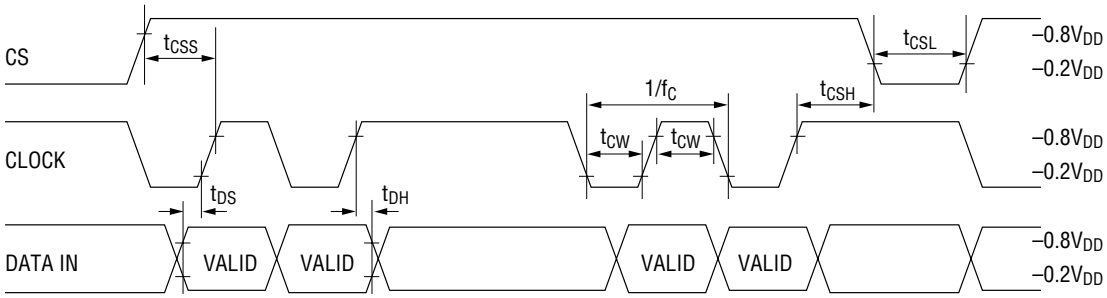
AC Characteristics

Ta=–40 to 85°C, V_{DISP} =8.0 to 18.0V, V_{DD}=4.5 to 5.5V

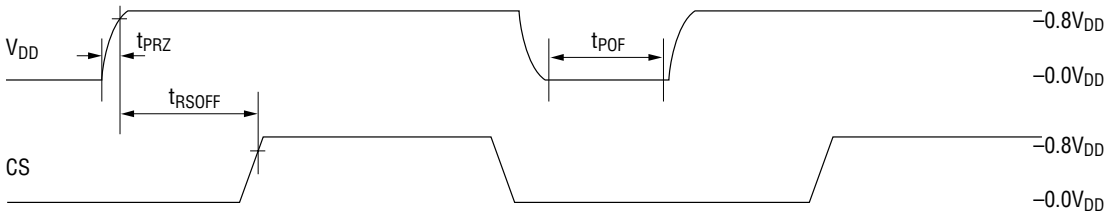
Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	1.0	MHz
Clock Pulse Width	t_{CW}	—		400	—	ns
Data Setup Time	t_{DS}	—		400	—	ns
Data Hold Time	t_{DH}	—		400	—	ns
CS Off Time	t_{CSL}	R2=4.7kΩ, C2=10pF		20	—	µs
CS Setup Time (CS-Clock)	t_{CSS}	—		400	—	ns
CS Hold Time (Clock-CS)	t_{CSH}	—		400	—	ns
Output Slew Rate Time	t_R	C_L=100pF	t_R=20% to 80%	—	4.0	µs
	t_F		t_R=80% to 20%	—	4.0	µs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit		—	100	µs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DD}=0.0V		5.0	—	ms
CS Wait Time	t_{RSOFF}	—		400	—	ns

TIMING DIAGRAM

● Data Input Timing

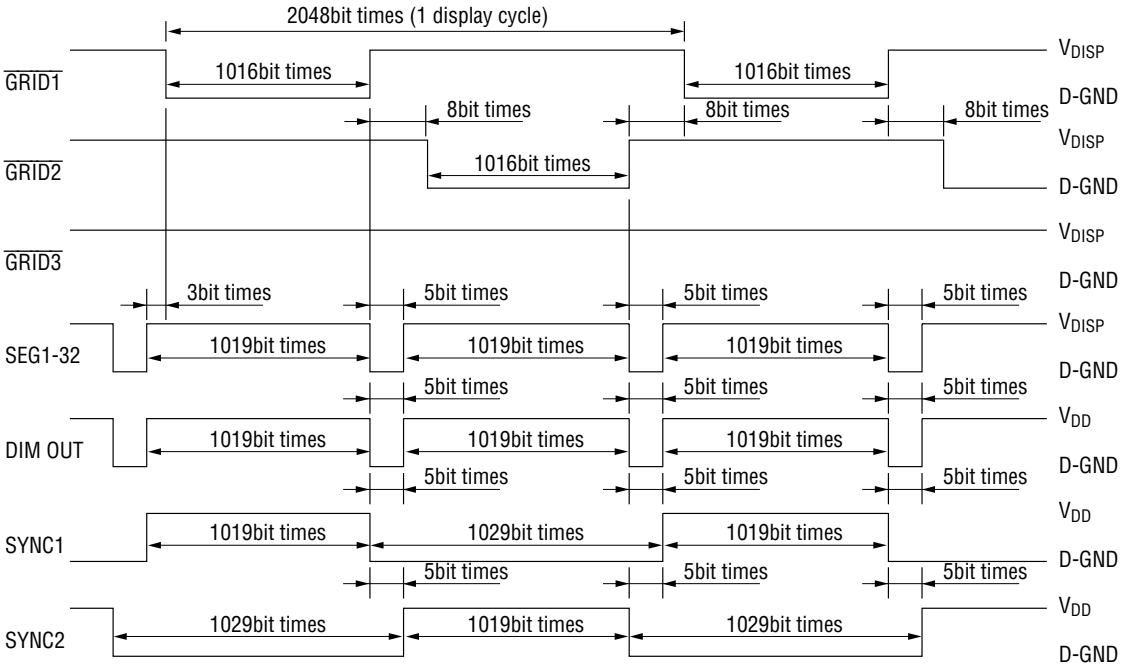


● Reset Timing

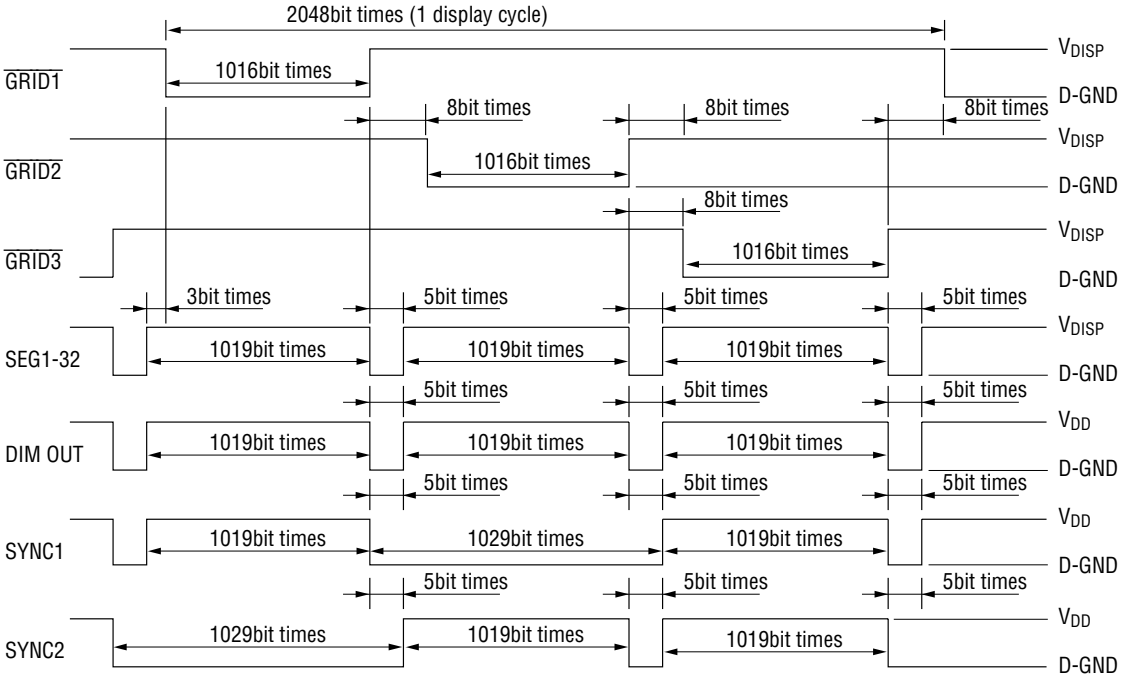


● Driver Output Timing

● **Output Timing (Duplex Operation)** *1bit time=4x f_{OSC}
(The dimming data is 1016/1024 at the master mode)



● **Output Timing (Triplex Operation)** *1bit time=4x f_{OSC}
(The dimming data is 1016/1024 at the master mode)



FUNCTIONAL DESCRIPTION

Power-on Reset

When power is turned on, MSM9210 is initialized by the internal power-on reset circuit, the status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to "0".
- The digital dimming duty cycle is set to "0".
- All segment outputs are set to "L" level.
- All grid outputs are set to "H" level. (at a master mode)
- All grid outputs are set to "L" level. (at a slave mode)

Data input

Data input to the DATA-IN pin is valid only when the CS pin is set at a "H" level.
The input data to DATA-IN pin is shifted into the shift register at the rising edge of the serial clock. The data is automatically loaded to the latches when ths CS pin is set at a "L" level.
MSM9210 uses 10-bit dimming data (D1 to D10) and 32-bit segment data (S1 to S32). To transfer these two data, the mode data (M0 to M2) must be sent after each of these data succeedingly.

Mode Data

Function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data is as follows:

FUNCTION MODE	OPERATING MODE	FUNCTION DATA		
		M0	M1	M2
0	Segment Data for $\overline{\text{GRID1-3}}$ Input	0	0	0
1	Segment Data for $\overline{\text{GRID1}}$ Input	1	0	0
2	Segment Data for $\overline{\text{GRID2}}$ Input	0	1	0
3	Segment Data for $\overline{\text{GRID3}}$ Input	1	1	0
4	Digital Dimming Data Input	0	0	1

Segment Data Input [Function Mode: 0 to 3]

- MSM9210 receive the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latches at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch that is selected by function data, when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 32) becomes "H" level (lightning) when the segment data (S1 to S32) is set to "1".

[Data Format]

Input Data : 35 bits
Segment Data : 32 bits
Mode Data : 3 bits

Bit	1	2	3	4	.....	29	30	31	32	33	34	35
Input Data	S1	S2	S3	S4	.....	S29	S30	S31	S32	M0	M1	M2

Display Data (32bits) | Mode Data (32bits)

[Bit correspondence between segment output and display data]

SEG n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Display data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
SEG n	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Display data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32

Digital Dimming Data Input [Function Mode: 4]

- MSM9210 receives the digital dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit digital dimming data is input from LSB

[Data Format]

Input Data : 13 bits
Digitsl Diming Data : 10 bits
Mode Data : 3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input Data	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2
	LSB ◄					Digital Dimming Data (10bits)				MSB ►	◄	Mode Data (3bits)	►

(LSB)				Dimming Data					(MSB)	Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
				⋮						⋮
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
				⋮						⋮
1	1	1	1	1	1	1	1	1	1	1016/1024

Master Mode

Master Mode is selected when M/$\overline{S}$ pin is set at "H" level. The master mode operation is as follows:

- The input levels of DIM IN, SYNC IN1 and SYNC IN2 are ignored.
- The pulse width of GRID1 to 3 and SEG1 to 32 are controlled by the internal digital dimming circuit.
- The segment Latch1 to 3 corresponding to $\overline{\text{GRID1 to 3}}$ selected by the internal timing generator.
- SYNC OUT1 and 2 output the segment latch select signals.
- DIM OUT outputs the segnent pulse width control signal.

Slave Mode

Slave Mode is selected when M/$\overline{S}$ pin is set at "L" level. The slave mode operation is as follows:

- The internal dimming circuit is ignored.
- The pulse width of SEG1 to 32 are controlled by the pulse width of DIM IN signal.
- The segment Latch1 to 3 corresponding to GRID1 to 3 selected by SYNC IN1 and SYNC IN2 signals.
- The output levels of GRID1 to 3, DIM OUT, SYNC OUT1 and SYNC OUT2 are set at "L" level.

[Correspondence between SYNC IN1, 2 and Segment Latch1 to 3]

SYNC IN 1	SYNC IN 2	Segment Latch	GRID
0	0	No	No
1	0	Latch1	$\overline{\text{GRID1}}$
0	1	Latch2	$\overline{\text{GRID2}}$
1	1	Latch3	$\overline{\text{GRID3}}$

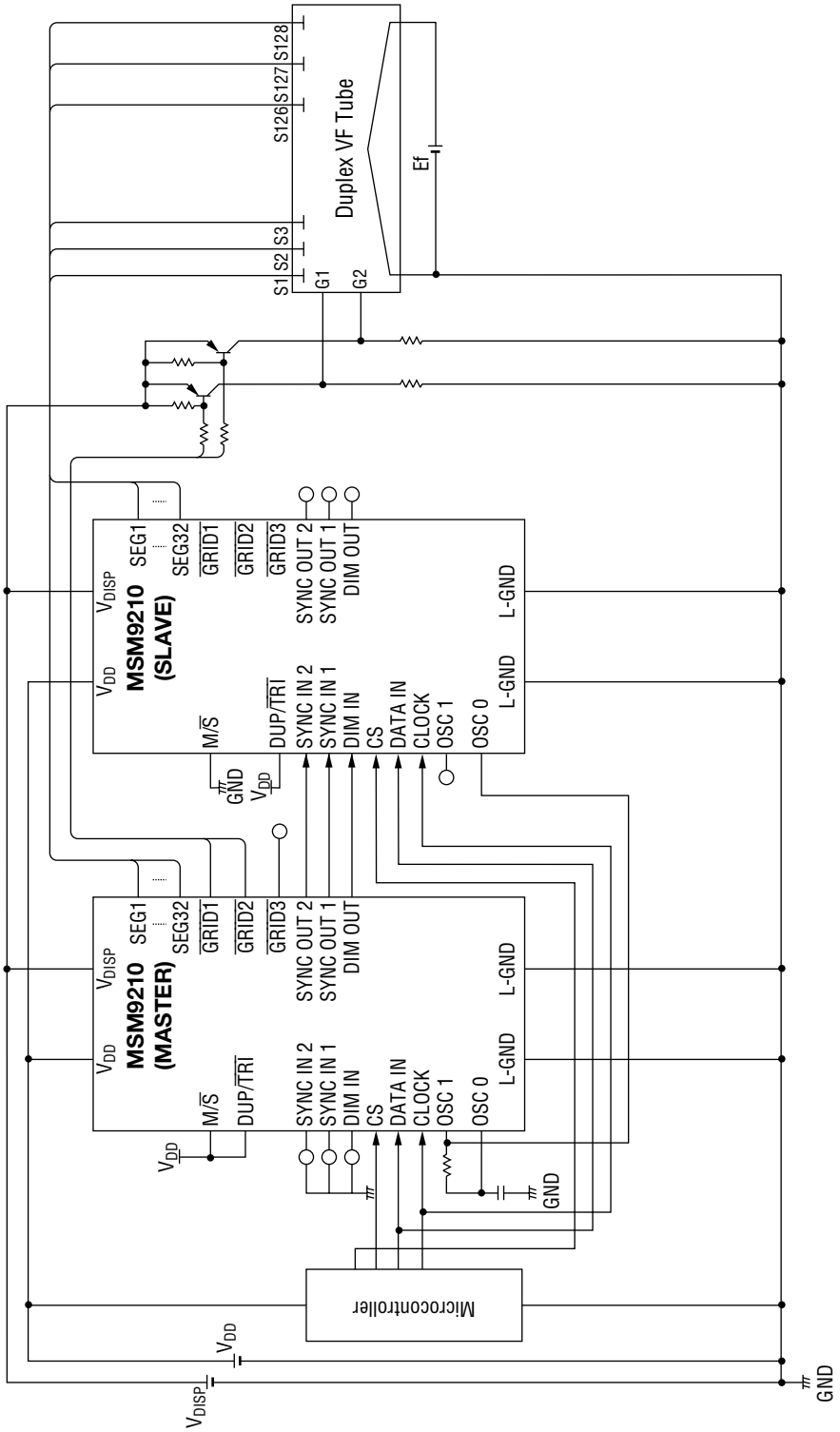
[Correspondence between DIM IN and SEG1 to 32]

DIM IN	SEG1 to 32
0	Low
1	High

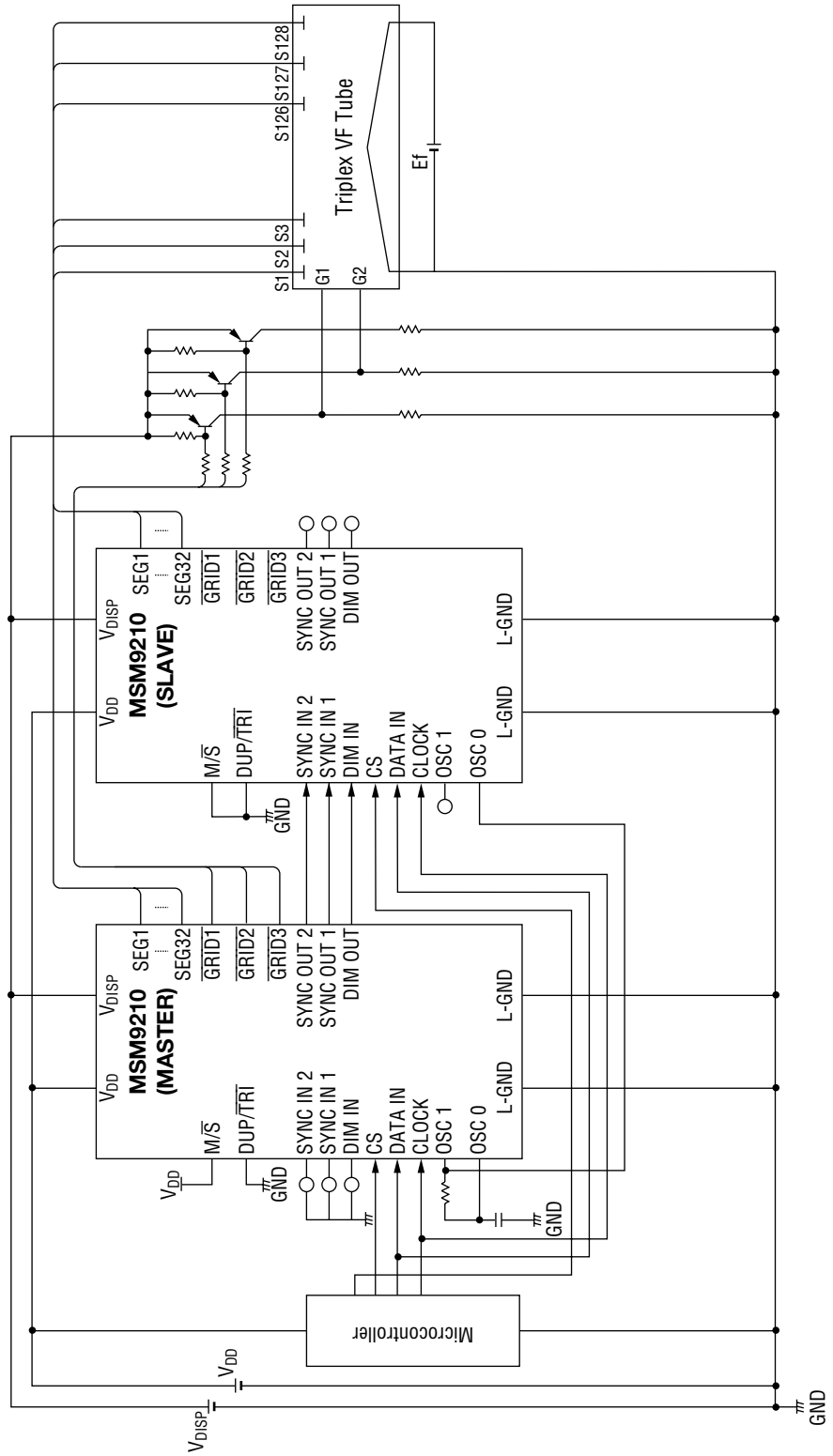
Note: When segment Data (S1 to S32) are "H" level.

APPLICATION CIRCUITS

1. Circuit for the duplex VF tube with 128 segments (2 Grid × 64 Anode)



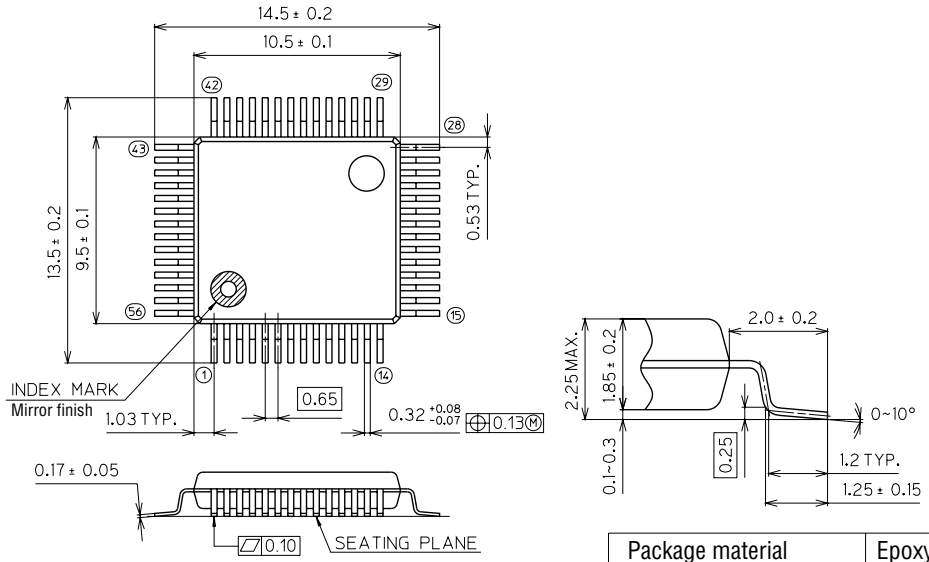
2. Circuit for the triplex VF tube with 192 segments (3 Grid × 64 Anode)



PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).