Winbond
ACPI-STR Controller
W83301R

Date: 2002/07 Revision: 1.0

W83301R
Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		07/2002	1.0	1.0	1st Release

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LIFE SUPPORT APPLICATIONS

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Winbond Electronics Corp.

1. General Description

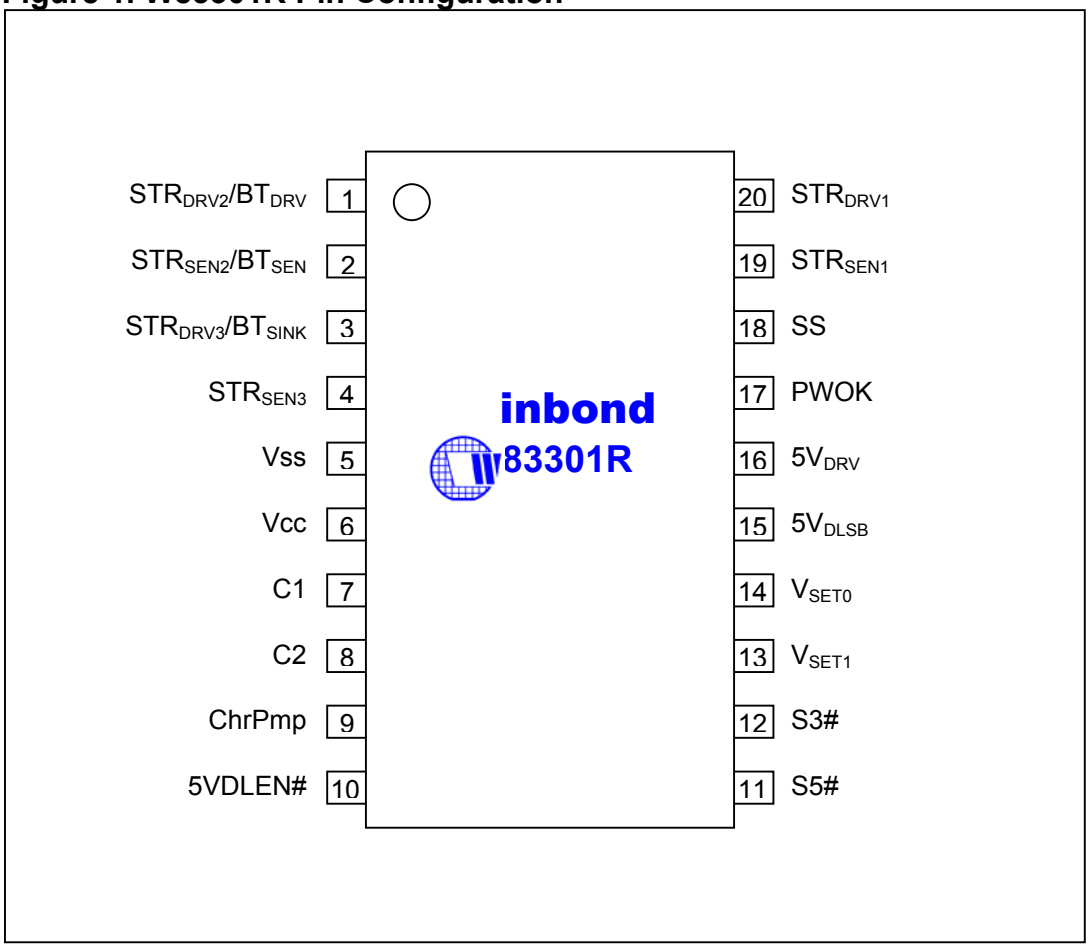
The W83301R is an ACPI-compliant controller for microprocessor and other computer applications. In substance, the part can mainly operate in alternative configurations mode A and B – mode A provides a switch controller to generate a $5V_{DL}$ voltage from ATX power supply, a linear controller – STR1 ($2.5V_{DUAL}$), and a bus termination controller – 1.25 V_{DUAL} for high speed bus such as RDRAM/DDRAM current sinking and sourcing; and mode B provides a switch controller to generate a $5V_{DL}$ voltage from ATX power supply and three linear controllers for specific voltage regulations – that is STR1 ($2.5V_{DUAL}$), STR2 ($3.3V_{DUAL}$) and STR3 (1.8 V_{DUAL}), all of the outputs can simply configured by V_{SET0}, V_{SET1}. Besides, the W83301R also can provide extra voltage up to 0.2V in each regulator output for more performance. In order to reduce the customer's cost, and simplify the circuit design, the W83301R integrates a charge-pump engine into the chip to provide higher driving voltage for single N-channel MOSFETs, that is the W83301R, can drive only N-channel MOSFETs for all applications. In the other hand, the W83301R also offer PWOK and over current detection to protect each output and soft-start protects all linear controllers from rush current attack. The W83301R is available in a 20-pin SOP package.

2. Features

- Provides alternative configurations for flexible applications
  - Mode A
    - Provide a switch controller to generate $5V_{DUAL}$
    - Linear controller STR1–$2.5V_{DUAL}$ (RDRAM/DDRAM application)
    - Bus termination controller –$1.25V_{DUAL}$ for high speed bus termination application to sinking and sourcing redundant current
  - Mode B
    - Provide a switch controller to generate $5V_{DUAL}$
    - Linear controller STR1 – $2.5V_{DUAL}$ (Clock Gen. Application)
    - Linear controller STR2 – 3.3 V_{DUAL} (SDRAM Application)
    - Linear controller STR3 – $1.8V_{DUAL}$ (Chipset Application)
- Provide a switch to enable/disable $5V_{DL}$ output in S5 state via $5V_{DLEN}$ pin for USB application
- Supports SDRAM/RDRAM/DDRAM ACPI-STR Functions
- Drives all N-Channel MOSFETs
- Power-Up Softstart for all controllers
- Up to 0.2V incremental voltage on STR1/STR2 for over-clock application.
- Under-Voltage Fault Monitor
- Soft-Start function
- 20-Pin SOP Package

3.Pin Configuration

Figure 1. W83301R Pin Configuration



4.Pin Description

SYMBOL	PIN	FUNCTION
STR_{DRV2}/BT_{DRV}	1	**Mode A: BT Current Source.** Connect this pin to the gate of a suitable N-channel MOSFET for driving bus termination regulator output.
		Mode B: STR2 Driver. Connect this pin to the gate of a suitable N-channel MOSFET for driving STR2 output.
STR_{SEN2}/BT_{SEN}	2	**Mode A: BT Sense.** Connect this pin to the bus termination regulator output.
		Mode B: STR2 Sense. Connect this pin to the STR2 output.
STR_{DRV3}/BT_{SINK}	3	**Mode A: BT Current Sink.** This pin is used to drive a N-channel MOSFET to sink the redundant current in the high-speed bus.
		Mode B: STR3 Driver. Connect this pin to the gate of a suitable N-channel MOSFET for driving STR3 output.
STR_{SEN3}	4	**Mode A: Function Reserved.** Pull up this pin to +5VSB through a 1.5 Kohm resistor.
		Mode B: STR3 Sense. Connect this pin to the STR3 output.
GND	5	**Power Ground.** Connect this pin to ground.
Vcc	6	**Power Vcc.** Input 5VSB supply.
C1	7	**Charge Pump Cap.** Attach flying capacitor between this pin and C2 to generate internally used high voltage from 5V power supply.
C2	8	**Charge Pump Cap.** Attach flying capacitor between this pin and C1 to generate internally used high voltage from 5V power supply.
ChrPmp	9	**Charge Pump output.** This pin produces voltage doubled 5V supply by charge-pumping. Bypass with a 0.1uF capacitor.
$5V_{DLEN}$#	10	**5VDL Enable.** Control $5V_{DL}$ voltage output. Pull-up internally.
S5#	11	**S5 Status.** Control signal governing the soft off state S5. Pull-up internally.
S3#	12	**S3 Status.** Control signal governing the soft off state S3. Pull-up internally.
V_{SET1}	13	**Voltage Selection 1.** Combine with VSET2 to select operation mode and output voltages of STR regulators.
V_{SET0}	14	**Voltage Selection 0.** Combine with VSET1 to select operation mode and output voltages of STR regulators.
$5V_{DLSB}$	15	**5VSB Output Control.** Connect this pin to the gate of a N-MOSFET to output 5VSB power to $5V_{DL}$.
$5V_{DRV}$	16	**5V Output Control.** Connect this pin to the gate of a N-MOSFET to output 5V power to $5V_{DL}$.
PWOK	17	**Power OK.** Open collector input/output. Used to indicate the ready of 5Vin supply. If any STR supply (only STR1 in mode A) occurs over current and induce under-voltage, PWOK will be pull down.
SS	18	**Soft-Start.** Attach a capacitor (0.033u) to this pin to determine the softstart rate. A ramp generated by charging this capacitor with internal soft-start current (18uA) is used to clamp the voltage rising slew rate of STR regulators and $5V_{DL}$. Soft starting avoids too much rush current during voltage setup.
STR_{SEN1}	19	**STR1 Sense.** Connect this pin to the STR1 output.
STR_{DRV1}	20	**STR1 Driver.** Connect this pin to the gate of a suitable N-channel MOSFET for driving STR1 output.

5. Application Circuit

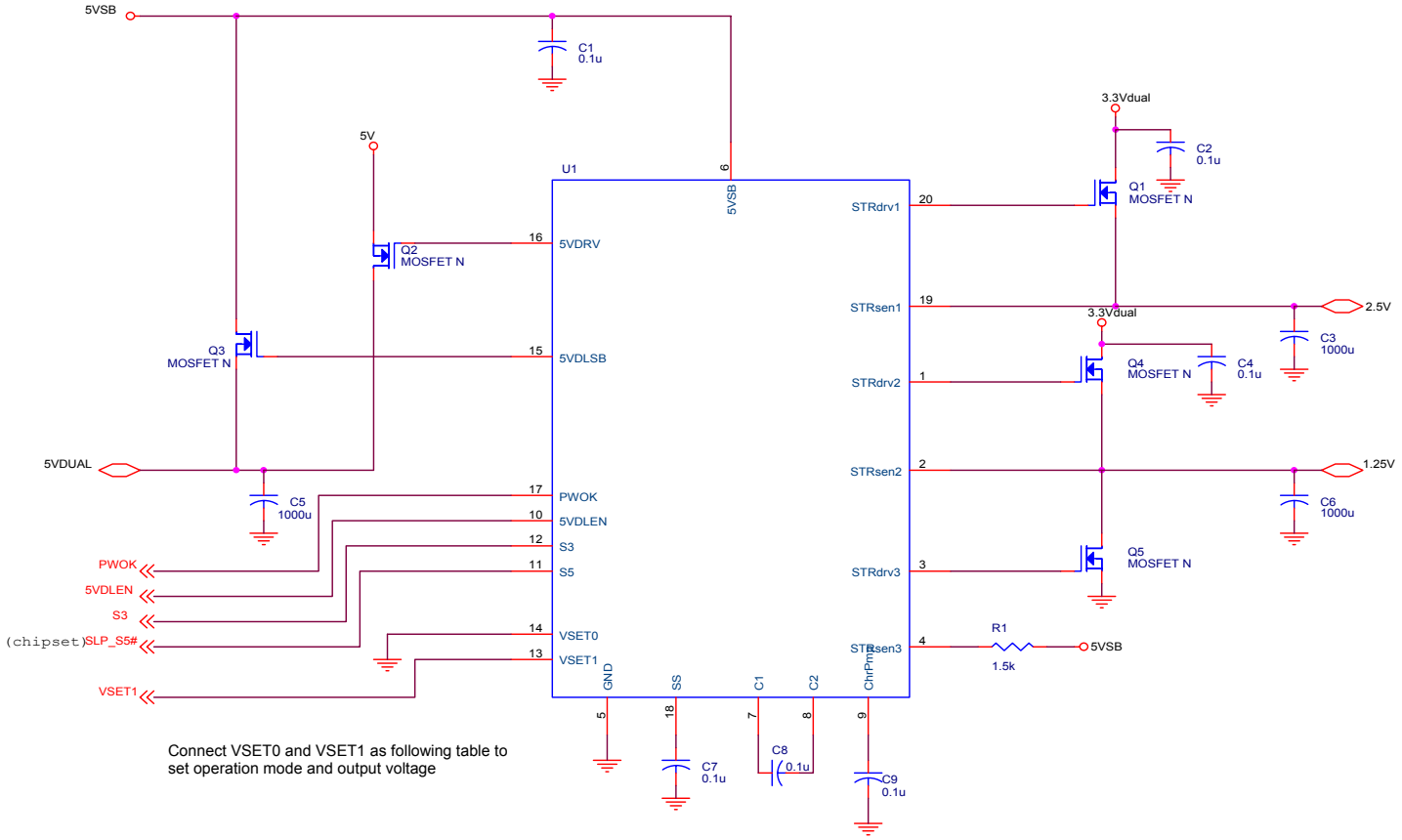
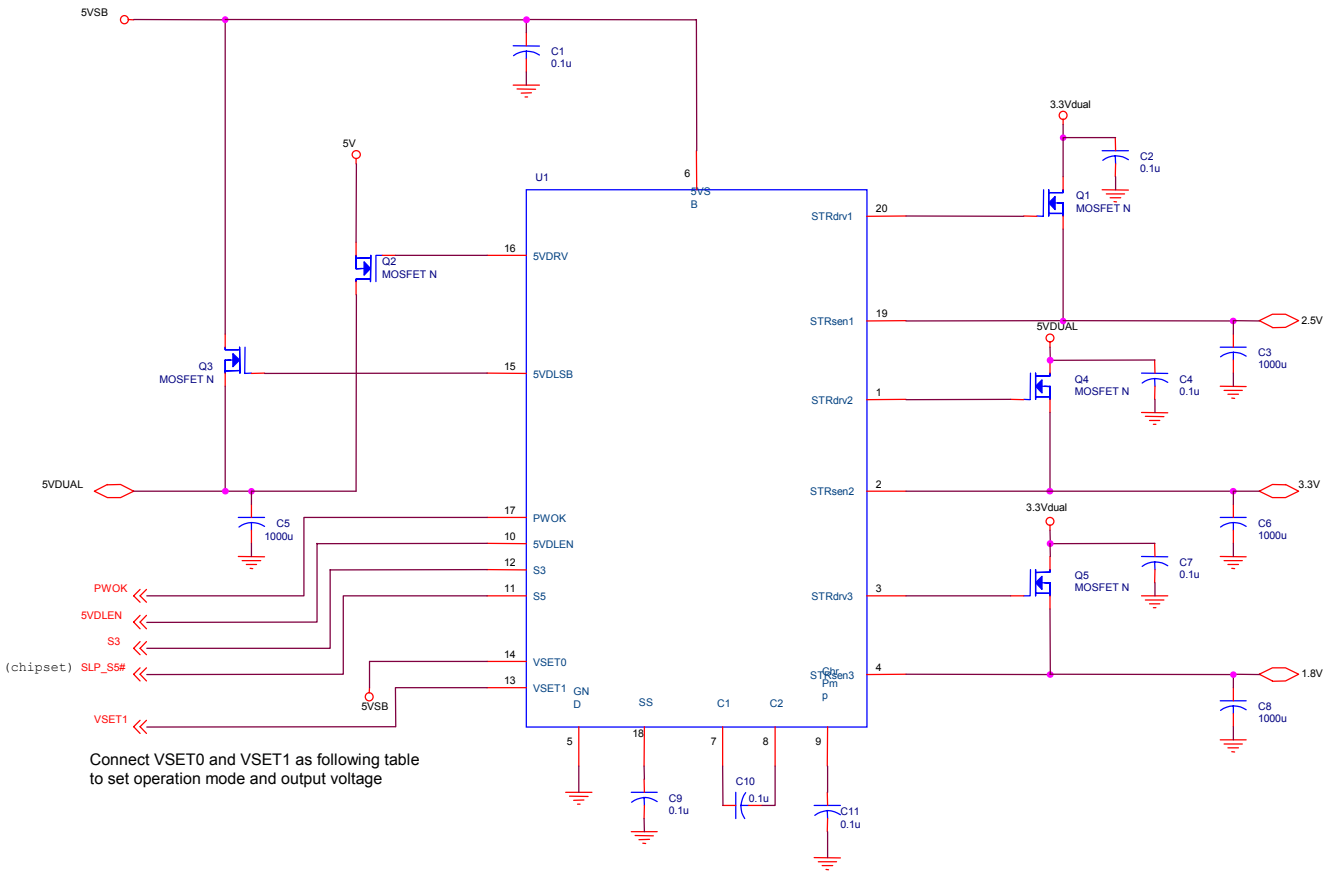


Figure 2. Mode A (DDR Mode) Application Circuit

Mode	VSET0	VSET1	STR1	Bus Termination Controller
DDR	0V	0V	$2.5V_{DUAL}$	$1.25V_{DUAL}$
	0V	NC	$2.6V_{DUAL}$	$1.30V_{DUAL}$
	0V	5V	$2.7V_{DUAL}$	$1.35V_{DUAL}$

5. Application Circuit

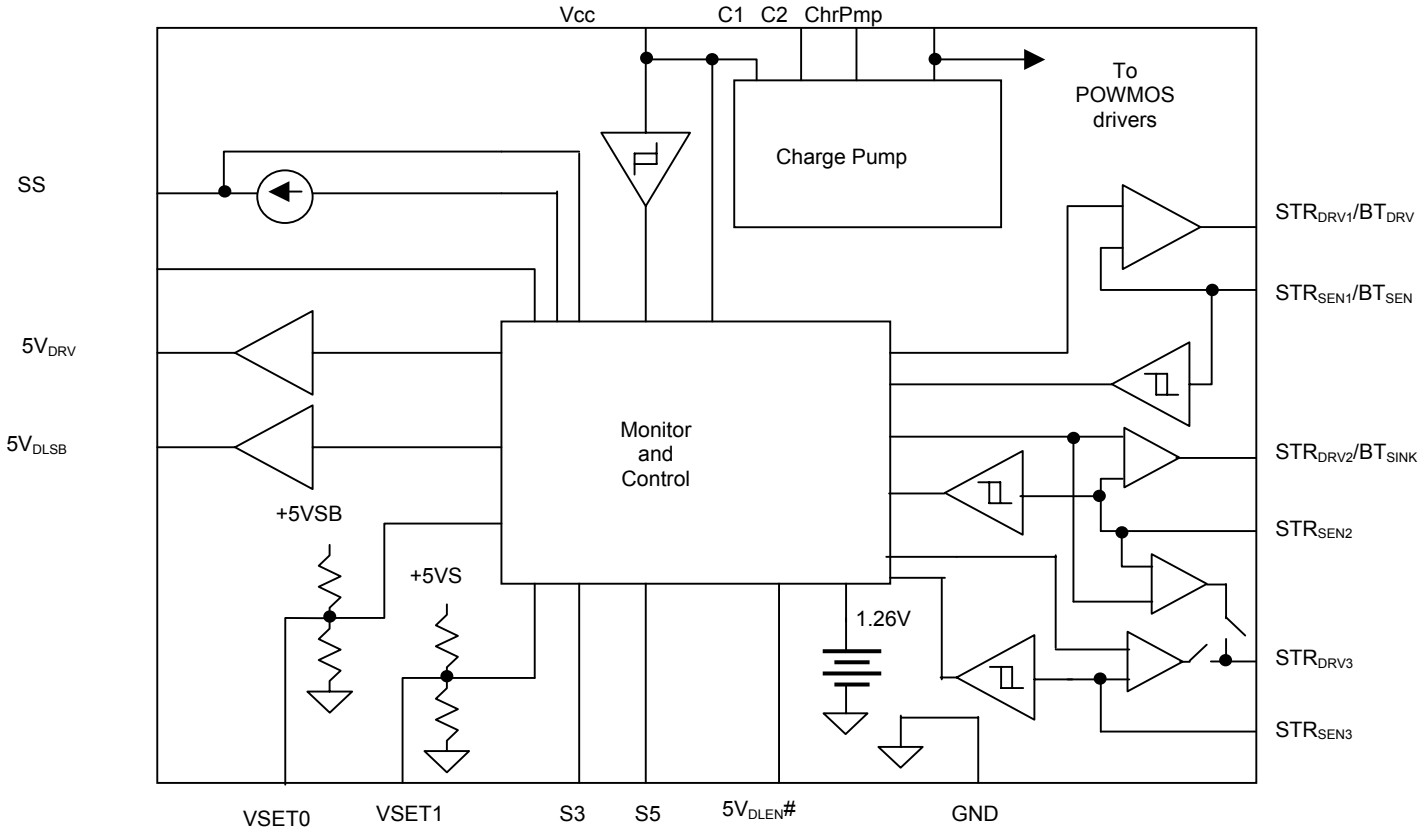
Figure 3. Mode B (SDRAM Mode) Application Circuit



Mode	VSET0	VSET1	STR1	STR2	STR3
SDRAM	5V	5V	$2.5V_{DUAL}$	$3.3V_{DUAL}$	$1.8V_{DUAL}$
	5V	NC	$2.6V_{DUAL}$	$3.4V_{DUAL}$	$1.8V_{DUAL}$
	5V	0V	$2.7V_{DUAL}$	$3.5V_{DUAL}$	$1.8V_{DUAL}$

6.Block Diagram

Figure 4. W83301R Internal Block Diagram



7. Functional Description

7.1 Mode Selection

The W83301R supports two modes for customer's multi-applications, as shown as Table1, the mode A and mode B can selected via VSET0 pin. If this pin connects to 5V, the chip will operate under mode A, otherwise the chip will operate under mode B when VSET0 connects to ground.

Both mode A and B supports a linear switch to generate an ACPI-compliant $5V_{DL}$ voltage from ATX power supply $5V/5V_{SB}$ according to S5# and S3# signals. And user also can turn off the whole $5V_{DL}$ output in S5 state via $5V_{DLEN}$# pin if needed.

Under the mode A operation, the chip provide a linear controller STR1 that drives a N-channel MOSFET Q3 (refer to figure) to generate a regulated voltage $2.5V_{DUAL}$ from an external power source $3.3V_{DUAL}$, the 2.5 V_{DUAL} is provide for RDRAM/DDRAM ACPI suspend to RAM application. And In order to simply the circuit design and reduce customer's cost, the W83301R also integrate a bus termination controller BT driving two external N-channel MOSFETs (Q4, Q5) to generate a specific ACPI-compliant voltage according to a half of STR1 output for sourcing and sinking bus redundant current.

Under the mode B operation, the chip provide three linear controllers, that is STR1- $2.5V_{DUAL}$, STR2- 3.3 V_{DUAL}, and STR3- $1.8V_{DUAL}$, all of the three outputs drive a N-channel MOSFET (Q3, Q4, and Q5) to generate an ACPI-compliant voltage by different applications. Such as STR1- $2.5V_{DUAL}$ for clock generator application, STR2- 3.3 V_{DUAL} for SDRAM application, and STR3- $1.8V_{DUAL}$ chipset application.

Besides, as shown in Table 1 the W83301R also provide a tri-state pin VSET1 to bias an extra voltage up to 0.2V in each output for more performance but under mode A operation, the BT output voltage will generated according to a half of STR1 output set by VSET1.

Table 1. W83301R Control Table

Mode	VSET0	VSET1	STR1	Bus Termination Controller		Remark
A	0V	0V	$2.5V_{DUAL}$	$1.25V_{DUAL}$		-STR1 output for RDRAM/DDRAM voltage -Bus Termination Controller for memory bus redundant current sinking and sourcing.
	0V	NC	$2.6V_{DUAL}$	$1.30V_{DUAL}$		
	0V	5V	$2.7V_{DUAL}$	$1.35V_{DUAL}$		
Mode	VSET0	VSET1	STR1	STR2	STR3	Remark
B	5V	5V	$2.5V_{DUAL}$	$3.3V_{DUAL}$	$1.8V_{DUAL}$	-STR1 output for Clock Gen. voltage -STR2 output for SDRAM voltage -STR3 output for Chipset voltage
	5V	NC	$2.6V_{DUAL}$	$3.4V_{DUAL}$	$1.8V_{DUAL}$	
	5V	0V	$2.7V_{DUAL}$	$3.5V_{DUAL}$	$1.8V_{DUAL}$	

7.2 ACPI State Control

In order to meet the ACPI specification, the W83301R implement a state machine as shown as Figure 5 to generate ACPI-compliant power state transition.

There are only five states in the state machine cause the W83301R only focus on the memory ACPI control, and the five states are G3 (Mechanical-Off State), S0 (Full-Power State), S3 (Sleeping State-Suspend to RAM), $S5_{On}$ (Soft-Off State), $S5_{Off}$ and all of these states changed to the other according to the condition of S3#, S5# and $5V_{DLEN}$#. On the other hand, cause of the W83301R allows customer to disable/enable the $5V_{DUAL}$ output in S5 state via $5V_{DLEN}$# pin, there are two states, $S5_{On}$ and $S5_{Off}$, corresponding to S5 state. A soft ramp-up mechanism is needed to protect the $5V_{DL}$ output from the rush current attack during the $S5_{Off}$ to $S5_{On}$ state transition. Same as the $5V_{DL}$ output, the W83301R also provides soft ramp-up mechanism during $S5_{On}$ to S0 state transition in each STR output.

In the state machine, when the power on, and the 5V input from power supply arrive 4.5V, the chip will enter $S5_{Off}$ first from G3, and ramp-up into $S5_{On}$ state by two conditions, the one is when $5V_{DLEN}$#=0 under standby power supply to resume the $5V_{DL}$ output, the other one is S3#=1 and S5#=1 the system will enter S1 state.

During $S5_{On}$ state, the chip will return back to $S5_{Off}$ when the customer wants disabling the $5V_{SB}$ output ($5V_{DLEN}$#=1) to save some power. And the chip will drive all outputs into S0 state will S3#=1 and S5#=1.

When the system under the S0 state, the system should enter the S3-sleeping (S3#=0, S5#=1) or S5-soft off (S5#=0) state when the system idle for a long time or user power-off.

When the system suspend to RAM, the system will be wakeup and enter S0-full power state by (S3#=1, S5#=1,PWOK=1), or get into S5-sleeping soft off state by (S5#=0)

Table 2. W83301R Outputs Table

State	$5V_{DL}$	STR1	STR2	STR3	LUV Activity *
G3	Off	Off	Off	Off	No
S5 ($5V_{DL}$ Off)	Off	Off	Off	Off	No
S5 ($5V_{DL}$ On)	On (Driven by $5V_{DLSB}$)	Off	Off	Off	No
S0	On (Driven by $5V_{DRV}$)	On	On	On	Yes
S3	On (Driven by $5V_{DLSB}$)	On	On	On	Yes

*When the STR2 & STR3 configured as bus termination controller, only STR1 has linear under voltage function.

7.3 Charge Pump

In order to simply the design circuit and provide a good-price solution for customer, the W83301R integrate with a switched-capacitor voltage doubler charge pump to provide a higher driving voltage (Up to 10 volt) and can drive a single N-channel MOSFETs in each output.

7.4 Power OK

The W83301R use a bi-direction Power OK signal to ensure the system can work normally. When the system jump from state S3 to state S0, the W83301R will monitor the input signal from PWOK pin to ensure that external system power is OK and then switch each outputs into S0 stage; In the other hand, the W83301R will pull down the Power OK signal to inform the system that a over current and induce under-voltage occurred.

7.5 Soft-Start

During ‘S5off’ to ‘S5on’ and ‘S5on’ to ‘S0’ state transitions, the 5Vdual and STR voltages need to ramp up from 0 to their set values respectively. The charging current flowing to output capacitors must be limited to avoid supply drop-off.

In W83301R, an internal 18 uA current source (Iss) charges an external capacitor (Css) to generate a linear ramp-up voltage on SS pin (Vss). The Vss slews from 0 to about 9V during the above-mentioned state transitions, and the Vss slew rate is used to clamp the ramp-up rate of 5Vdual and STR output voltages. This output clamping allows power-ups free of supply drop-off events.

Since the outputs are ramped up in a constant slew-rate, the current dedicated to charge any output capacitor can be calculated with the following formula:

I_{COUT} = Iss x (Cout / Css)

Some technique is included in W83301R to further reduce the total charging current: In Mode B configuration, the start-up of ramp-up time STR3 (1.8V) will be advanced from that of STR1 to reduce the overlap time of charging. And in Mode A configuration, the bus-terminator is input clamped, and its output voltage slew-rate, so as its charging current, will be limited to half of that of STR1.

Note that, too slow ramp-up rate is not recommended. If so, the state transition mentioned above will be prolonged to much. Before Vss ramps up to its upper limit (about 9V), the state transition will not be completed and will not go into next state.

8. Electrical Characteristics

8.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vss, V_{cc}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
ChrPmp		- 0.5 V to + 12.0 V
Hi-V Pins	Pin# 1,2,3,4,8,15,16,18,19,20	GND-0.3 V to $V_{Chr-Pmp}$ + 0.3V
Lo-V Pins	Pin# 7,10,11,12,13,14,17	GND-0.3 V to Vcc + 0.3V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

8.2 AC CHARACTERISTICS

Vcc=5V ± 5 %, T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Vcc SUPPLY CURRENT						
Norminal Supply Current	**I_{5VSB}**		6		mA	
POWER-ON RESET						
Rising V_{5VSB} Threshold				4.3	V	V_{Chr_Pmp} > 8.5V
5VSB Hysteresis			1		V	
Rising V_{Chr_Pmp} Threshold				8.5	V	V_{5VSB} > 4.3V
V_{Chr_Pmp} Hysteresis			1		V	
SOFT-START						
Soft-Start Current	**Iss**		18		uA	
V_{SS} upper limit			9		V	

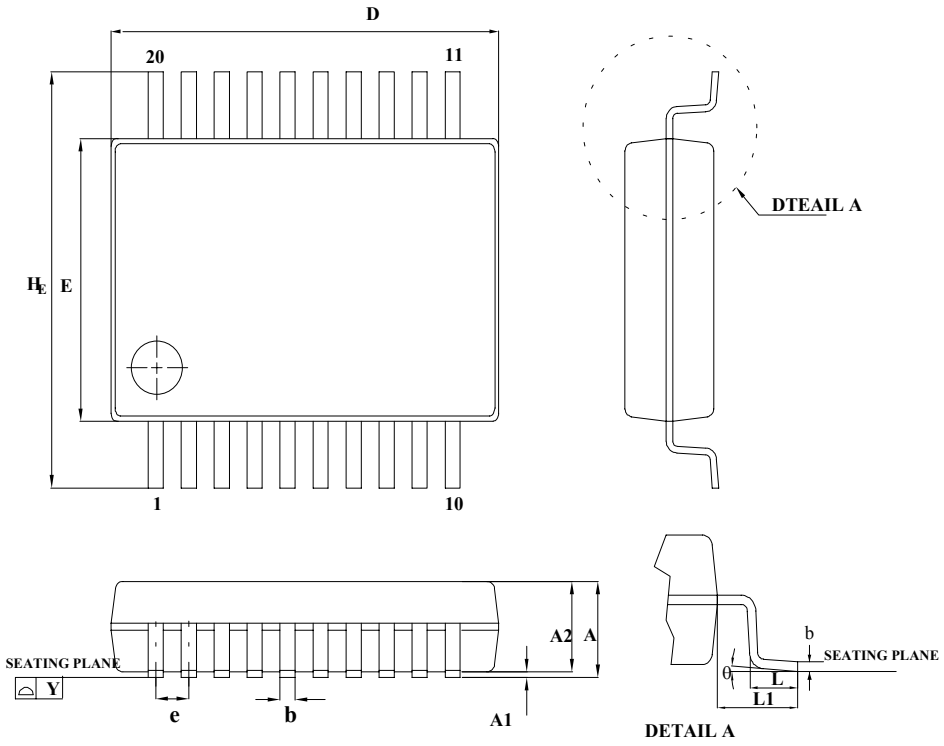
8.2 AC CHARACTERISTICS (Continued)

Vcc=5V ± 5 %, T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
STR1 IINEAR REGULATOR						
Nominal Output Voltage			2.5		V	VSET0=0V, VSET1=0V or VSET0=5V,VSET1=5V
Nominal Output Voltage			2.6		V	VSET0=0V, VSET1=NC or VSET0=5V,VSET1=NC
Nominal Output Voltage			2.8		V	VSET0=0V, VSET1=5V or VSET0=5V,VSET1=0V
Regulation				5	%	
STR_{SEN1} Under-Voltage Falling Threshold			80		%	
MAX STR_{DRV1} Output Voltage		6			V	$I(STR_{DRV1}) < 0.1mA$
STR2 LINEAR REGULATOR						
Nominal Output Voltage			3.3		V	VSET0=5V,VSET1=5V
Nominal Output Voltage			3.4		V	VSET0=5V,VSET1=NC
Nominal Output Voltage			3.5		V	VSET0=5V,VSET1=0V
Regulation				5	%	
STR_{SEN1} Under-Voltage Falling Threshold			80		%	
MAX STR_{DRV1} Output Voltage		6			V	$I(STR_{DRV1}) < 0.1mA$
STR3 LINEAR REGULATOR						
Nominal Output Voltage			1.8		V	VSET0=5V
Regulation				5	%	
STR_{SEN1} Under-Voltage Falling Threshold			83		%	
MAX STR_{DRV1} Output Voltage		6			V	$I(STR_{DRV1}) < 0.1mA$
BUS TERMINATOR						
Nominal Output Voltage / $V_{STRSEN1}$			50		%	VSET0=0V
Regulation				5	%	
5VDUAL SWITCH CONTROLLER						
$5V_{DRV}$ Output High Voltage		9				Cload=3000p
$5V_{DRV}$ Sourcing Current			7		mA	Cload=3000p
$5V_{DRV}$ Sinking Current			400		uA	Cload=3000p
$5V_{DLSB}$ Output High Voltage		9				Cload=3000p
$5V_{DLSB}$ Sourcing Current			7		mA	Cload=3000p
$5V_{DLSB}$ Sinking Current			230		uA	Cload=3000p
S3#,S5#,5VDLEN#, PWOK,CHARGE PUMP						
Input Logic High	2.2				V	

Input Logic Low				0.8	V	
PWOK Output Inpedence		150			ohm	LUV active
Charge Pump Frequency			200		KHz	

9. Package Specification

20L SSOP-209 mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

10. Ordering Information

Part Number	Package Type	Production Flow
W83301R	20-PIN SSOP	Commercial, 0°C to +70°C

11. How to Read the Top Marking

Left Line: Winbond Logo
1st line: Part No W83301R-G
2nd line: Tracking code XXXXXXXXX
3rd line: **Package date code XXX** + assembly house ID X + B: the IC version
1: wafers manufactured in Winbond FAB I
1039050-21NA: wafer production series number

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