STRUCTURE Silicon monolithic integrated circuit

PRODUCT NAME BU98032CH-3BW

FUNCTION 65,536 Colors 132RGB x 132 STN LCD control driver

FEATURE
- Supports 65,536 colors by PWM (Pulse Width Modulation) R:32, G:64, B:32 gray scale
- Supports variety interface (3/4-SPI,8bit parallel interface)

○ Absolute maximum ratings (VSS = 0V)

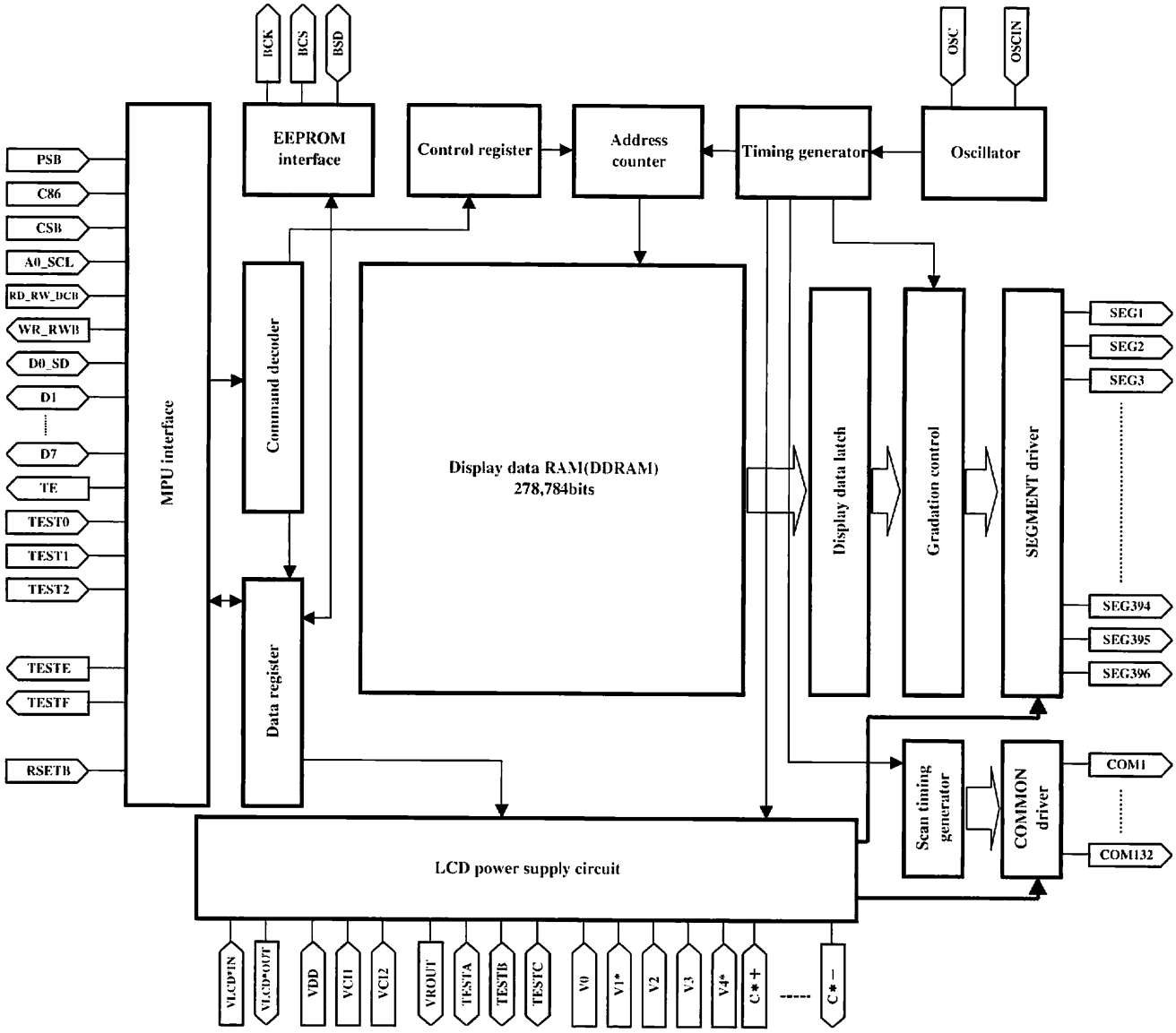
Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage 1	VDD	-0.5 ~ +4.0	V	Logic power supply
Power supply voltage 2	VCI1, 2	-0.5 ~ +4.0	V	Booster power supply
Power supply voltage 3	VLCD1IN_L, R	-0.5 ~ +22.0	V	LCD driver power supply
Input voltage range	VIN	-0.5 ~ VDD+0.5	V	
Operational temperature range	Topr	-40 ~ +85	℃	
Storage temperature range	Tstg	-55 ~ +125	℃	

○ Recommend operating conditions (Ta = 25℃, VSS = 0V)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power supply voltage 1	VDD	1.6	-	VCI1,2	V	Logic power supply
Power supply voltage 2	VCI1, 2	2.6	-	3.3	V	Booster power supply
Power supply voltage 3	VLCD1IN_L, R	6.0	-	20.0	V	LCD driver power supply

※ About shape / delivery forms of this product, please refer to "Specification of Chip Shipment"
※ About explanation about panel module design that used this product, please refer to "Panel Layout Design Guide"
※ About detailed function explanation of this product, please refer to "Function Description Guide"
※ About explanation about picture quality adjustment of this product, please refer to "Adjustment manual for the picture quality of LCD Display"

○ Block diagram



○ Electrical characteristics

DC characteristics

(Ta=-40～85℃, VDD=1.6V～3.3V, VCI=2.6V～3.3V, VSS = 0V, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
"H" level input voltage		VIH	0.7VDD	-	-	V	
"L" level input voltage		VIL	-	-	0.3VDD	V	
"H" level input leakage current		IIH	-	-	1	uA	
"L" level input leakage current		IIL	-1	-	-	uA	
"H" level output voltage		VOH	0.8VDD	-	-	V	IOH=-1mA
"L" level output voltage		VOL	-	-	0.2VDD	V	IOL=1mA
LCD driver ON resistance (COM)		RON1	-	1.0	4.0	kΩ	Iload=±10uA (COM1-COM132)
LCD driver ON resistance (SEG)		RON2	-	3.0	6.0	kΩ	Iload=±10uA (SEG1-SEG396)
LCD driver voltage		ΔV0	-350	-	+350	mV	V0=14V,-0.15%/℃
Standby current1	VDD	IDD1	-	-	20	uA	Sleep mode , Ta=85℃
	VCI	ICI1	-	-	5	uA	VDD=2.0V, VCI1,2=3.3V
Standby current2	VDD	IDD2	-	-	40	uA	Sleep mode , Ta=85℃
	VCI	ICI2	-	-	5	uA	VDD=3.3V, VCI=3.3V
Operating current	VDD	IDD3	-	-	400	uA	Normal operation , "All 0 display" MPU I/F non-Access VDD=1.8V, VCI1,2=2.75V VLCD1IN_L,R=VCI7xbooster fFR=80Hz, N-line=14 GCP0:The following reference
	VCI	ICI3	-	380	450	uA	
	VDD	IDD4	-	-	450	uA	Normal operation , "1 By 1display" MPU I/F non Access VDD=1.8V, VCI1,2=2.75V VLCD1IN_L,R=VCI7xbooster fFR=80Hz, N-line=14 GCP0:The following reference
	VCI	ICI4	-	580	650	uA	

Oscillation Characteristics

(Ta=-40～85℃, VDD=1.6V～3.3V, VCI=2.6V～3.3V, VSS = 0V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency (70Hz)	fFR	65.1	70	74.9	Hz	When select fFR=70Hz setting

RESET Characteristics

(Ta=-40～85℃, VDD=1.6V～3.3V, VCI=2.6V～3.3V, VSS = 0V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Reset enable width	tRWe	10	-	-	us	
Reset disable width	t RWn	-	-	2.2	us	
Reset command time	tRC	-	-	1.5	ms	
Noise width "H"	t PNS	-	-	20	ns	

MPU interface Characteristics (3-SPI / 4-SPI)

(Ta=-40～85℃, VDD=1.6V～3.3V, VCI=2.6V～3.3V, VSS = 0V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCYC	80	-	-	ns	
SCL "H" level pulse width	tSHW	35	-	-	ns	
SCL "L" level pulse width	tSLW	35	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	20	-	-	ns	
CSB setup time	tCSS	30	-	-	ns	
CSB hold time (Write)	tCSH	40	-	-	ns	
CSB "H" level pulse width	tCHW	30	-	-	ns	
CSB hold time (Read)	tSCC	15	-	-	ns	
SD output delay time	tACC	-	-	35	ns	CL=30pF, VDD=1.6V～2.0V
SD output hold time	tOH	-	-	40	ns	CL=30pF, VDD=1.6V～2.0V
D/CB setup time	tSAS	20	-	-	ns	
D/CB hold time	tSAH	20	-	-	ns	

MPU interface Characteristics (Parallel interface)

(Ta=-40～85℃, VDD=1.6V～3.3V, VCI=2.6V～3.3V, VSS = 0V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
Address setup time	tAS	20	-	-	ns	
Address hold time	tAH	20	-	-	ns	
Chip Select setup time	tCS	40	-	-	ns	
Chip Select hold time	tCW	20	-	-	ns	
Chip Select "H" width	tCSWH	50	-	-	ns	
Enable pulse width "H"	tWH	50	-	-	ns	
Enable pulse width "L"	tWL	40	-	-	ns	
Enable cycle time	tCYC	100	-	-	ns	
Data setup time	tDS	20	-	-	ns	
Data hold time	tDH	20	-	-	ns	
Data output delay time	tACC	-	-	35	ns	CL=30pF, VDD=1.6V～2.0V
Data output hold time	tOH	-	-	70	ns	CL=30pF, VDD=1.6V～2.0V

○ Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operatingconditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

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