

2048-pixel CCD Linear Image Sensor (B/W)

Description

The ILX511 is a rectangular reduction type CCD linear image sensor designed for bar code POS hand scanner and optical measuring equipment use. A built-in timing generator and clock-drivers ensure single 5 V power supply for easy use.

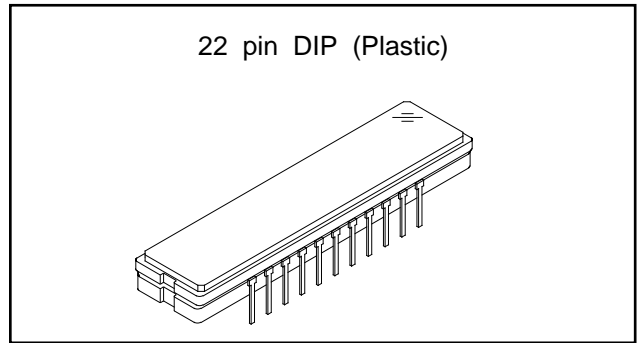
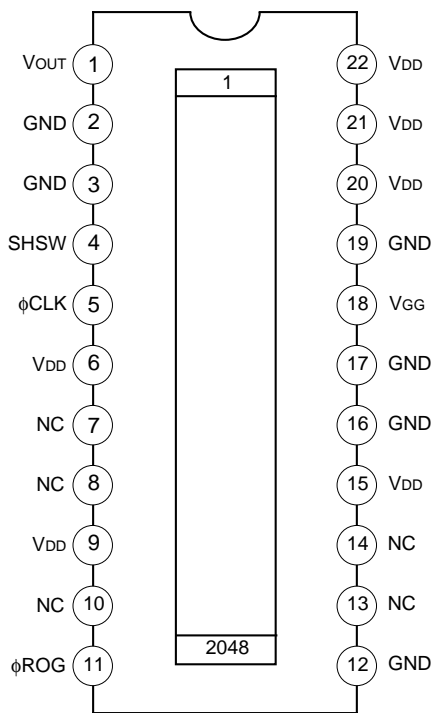
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14 μm × 200 μm (14 μm pitch)
- Single 5 V power supply
- Ultra-high sensitivity
- Built-in timing generator and clock-drivers
- Built-in sample-and-hold circuit
- Maximum clock frequency: 2MHz

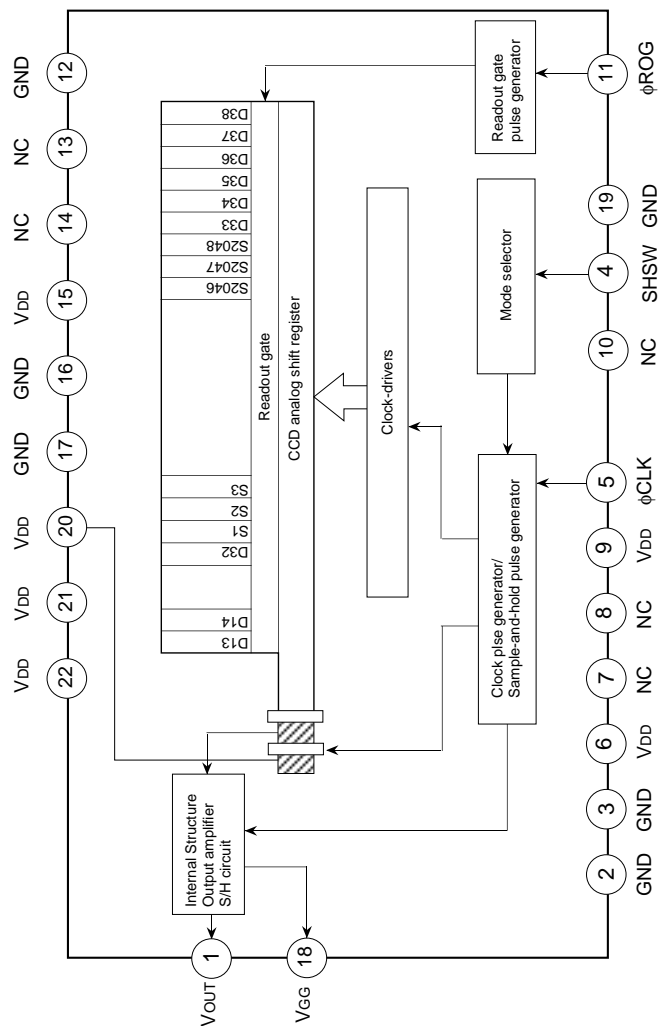
Absolute Maximum Ratings

- Supply voltage V<sub>DD</sub> 6 V
- Operating temperature -10 to +60 °C
- Storage temperature -30 to +80 °C

Pin Configuration (Top View)



Block Diagram



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**Pin Description**

| Pin No. | Symbol     | Description                      |
|---------|------------|----------------------------------|
| 1       | VOUT       | Signal output                    |
| 2       | GND        | GND                              |
| 3       | GND        | GND                              |
| 4       | SHSW       | Switch (with S/H or without S/H) |
| 5       | $\phi$ CLK | Clock pulse input                |
| 6       | VDD        | 5V power supply                  |
| 7       | NC         | NC                               |
| 8       | NC         | NC                               |
| 9       | VDD        | 5V power supply                  |
| 10      | NC         | NC                               |
| 11      | $\phi$ ROG | Readout gate pulse input         |
| 12      | GND        | GND                              |
| 13      | NC         | NC                               |
| 14      | NC         | NC                               |
| 15      | VDD        | 5V power supply                  |
| 16      | GND        | GND                              |
| 17      | GND        | GND                              |
| 18      | VGG        | Output circuit gate bias         |
| 19      | GND        | GND                              |
| 20      | VDD        | 5V power supply                  |
| 21      | VDD        | 5V power supply                  |
| 22      | VDD        | 5V power supply                  |

**Mode Description**

| Mode in Use | Pin 4 (SHSW) |
|-------------|--------------|
| With S/H    | GND          |
| Without S/H | VDD          |

**Recommended Voltage**

| Item | Min. | Typ. | Max. | Unit |
|------|------|------|------|------|
| VDD  | 4.5  | 5.0  | 5.5  | V    |

**Input Clock Voltage Condition (Note)**

| Item            | Min. | Typ. | Max. | Unit |
|-----------------|------|------|------|------|
| V <sub>IH</sub> | 4.5  | 5.0  | 5.5  | V    |
| V <sub>IL</sub> | 0    | —    | 0.5  | V    |

Note) This is applied to the all pulses applied externally. ( $\phi$  CLK,  $\phi$  ROG)

| Item                             | Symbol       | Min. | Typ. | Max. | Unit |
|----------------------------------|--------------|------|------|------|------|
| Input capacity of $\phi$ CLK pin | C $\phi$ CLK | —    | 10   | —    | pF   |
|                                  |              |      |      |      |      |

**Electro-optical Characteristics**

(Ta = 25 °C, VDD = 5 V, Clock frequency: 1 MHz, Light source = 3200 K, IR cut filter: CM-500S (t = 1.0 mm), Without S/H mode)

| Item                      | Symbol | Min. | Typ.  | Max. | Unit       | Remarks |
|---------------------------|--------|------|-------|------|------------|---------|
| Sensitivity 1             | R1     | 150  | 200   | 250  | V/(lx • s) | Note 1  |
| Sensitivity 2             | R2     | —    | 1800  | —    | V/(lx • s) | Note 2  |
| Sensitivity nonuniformity | PRNU   | —    | 5.0   | 10.0 | %          | Note 3  |
| Saturation output voltage | VSAT   | 0.6  | 0.8   | —    | V          | —       |
| Dark voltage average      | VDRK   | —    | 3.0   | 6.0  | mV         | Note 4  |
| Dark signal nonuniformity | DSNU   | —    | 6.0   | 12.0 | mV         | Note 4  |
| Image lag                 | IL     | —    | 1     | —    | %          | Note 5  |
| Dynamic range             | DR     | —    | 267   | —    | —          | Note 6  |
| Saturation exposure       | SE     | —    | 0.004 | —    | lx • s     | Note 7  |
| 5 V current consumption   | I VDD  | —    | 5.0   | 10.0 | mA         | —       |
| Total transfer efficiency | TTE    | 92.0 | 98.0  | —    | %          | —       |
| Output impedance          | Zo     | —    | 250   | —    | Ω          | —       |
| Offset level              | Vos    | —    | 2.8   | —    | V          | Note 8  |

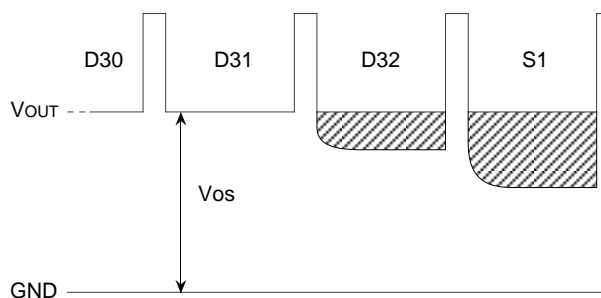
Note)

1. For the sensitivity test light is applied with a uniform intensity of illumination.
2. Light source: LED λ = 660nm
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

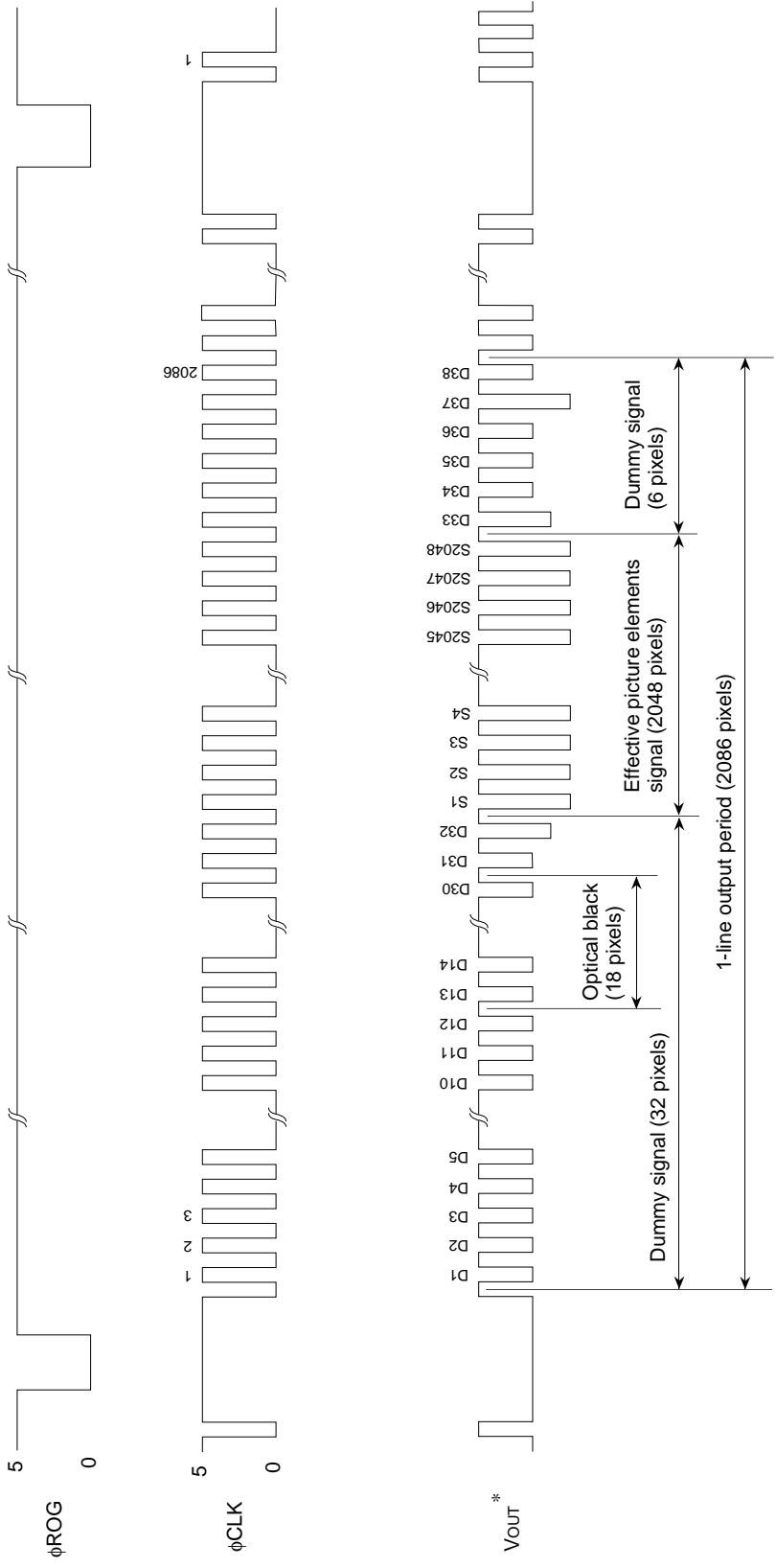
$$PRNU = \frac{(V_{MAX}-V_{MIN})/2}{V_{AVE}} \times 100 (\%)$$

The maximum output of all the valid pixels is set to VMAX, the minimum output to VMIN and the average output to VAVE.

4. Integration time is 10ms.
5. Typical value is used for clock pulse and readout pulse. VOUT = 500 mV.
6. DR = VSAT/VDRK. When optical integration time is shorter, the dynamic range sets wider because dark voltage is in proportion to optical integration time.
7. SE = VSAT/R1
8. Vos is defined as indicated below.



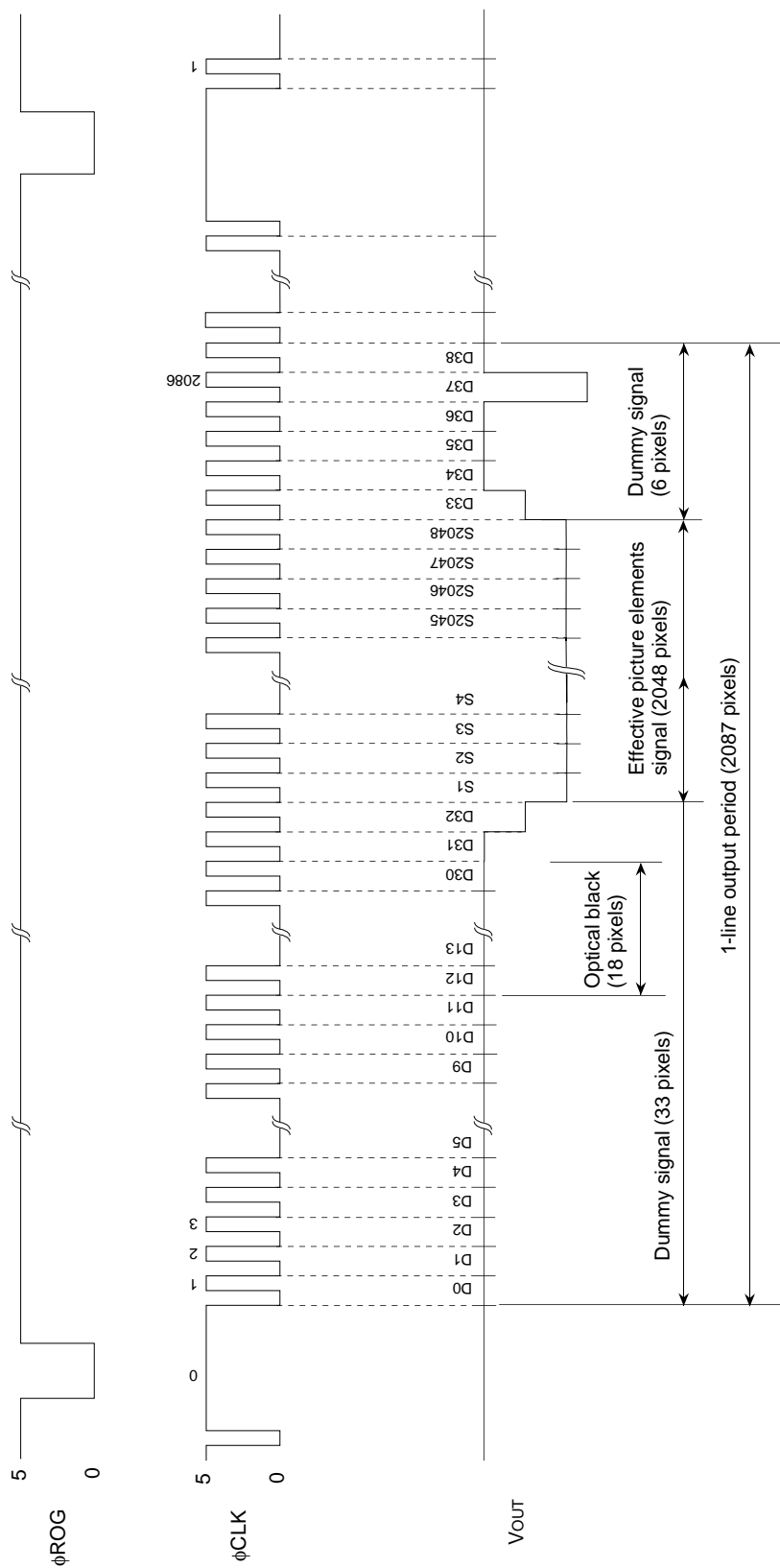
**Clock Timing Diagram (Without S/H mode)**



\* Without S/H mode (4pin  $\neq$   $V_{DD}$ )

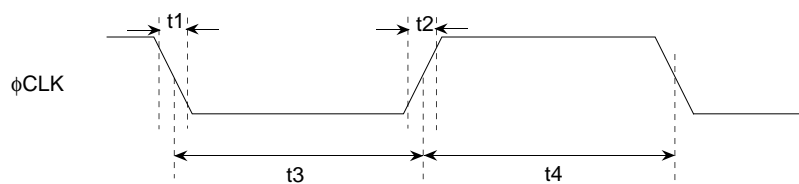
2088 or more clock pulses are required.

**Clock Timing Diagram (With S/H mode)**



2088 or more clock pulses are required.

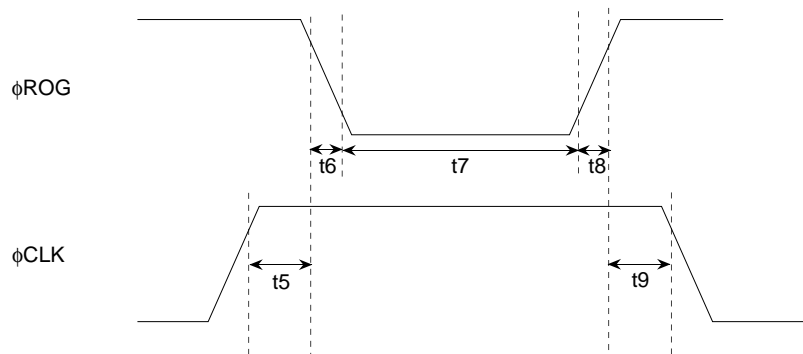
$\phi$  CLK Timing (For all modes)



| Item                            | Symbol     | Min. | Typ. | Max. | Unit |
|---------------------------------|------------|------|------|------|------|
| $\phi$ CLK pulse rise/fall time | $t_1, t_2$ | 0    | 10   | 100  | ns   |
| $\phi$ CLK pulse duty (Note 1)  | —          | 40   | 50   | 60   | %    |

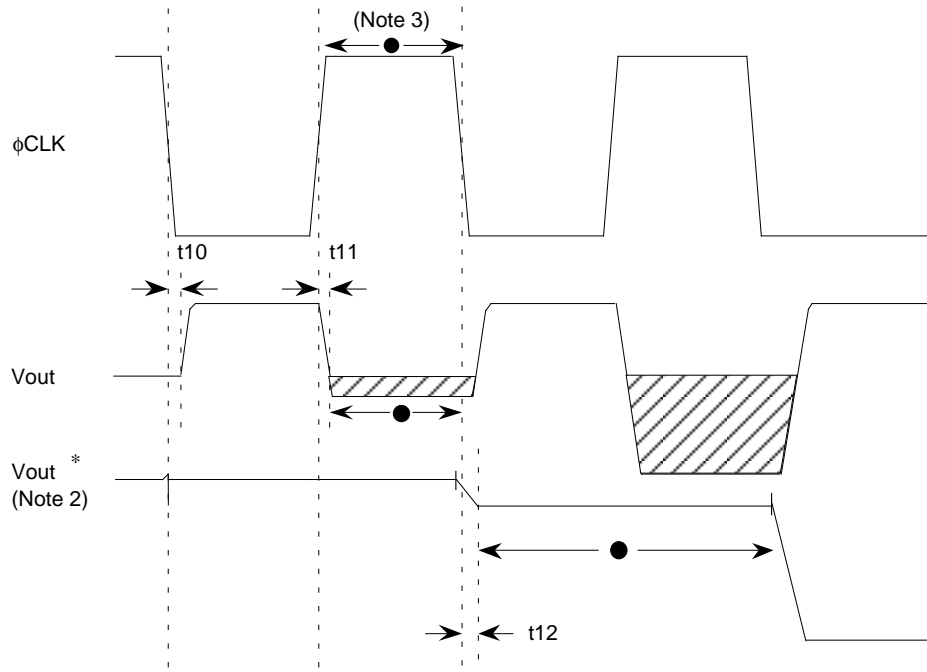
Note 1)  $100 \times t_4 / (t_3 + t_4)$

$\phi$  ROG,  $\phi$  CLK Timing



| Item                                  | Symbol     | Min. | Typ. | Max. | Unit |
|---------------------------------------|------------|------|------|------|------|
| $\phi$ ROG, $\phi$ CLK pulse timing 1 | $t_5$      | 0    | 3000 | —    | ns   |
| $\phi$ ROG, $\phi$ CLK pulse timing 2 | $t_9$      | 1000 | 3000 | —    |      |
| $\phi$ ROG pulse rise/fall time       | $t_6, t_8$ | 0    | 10   | —    |      |
| $\phi$ ROG pulse period               | $t_7$      | 3000 | 5000 | —    |      |

$\phi$  CLK, VOUT Timing (Note 1)

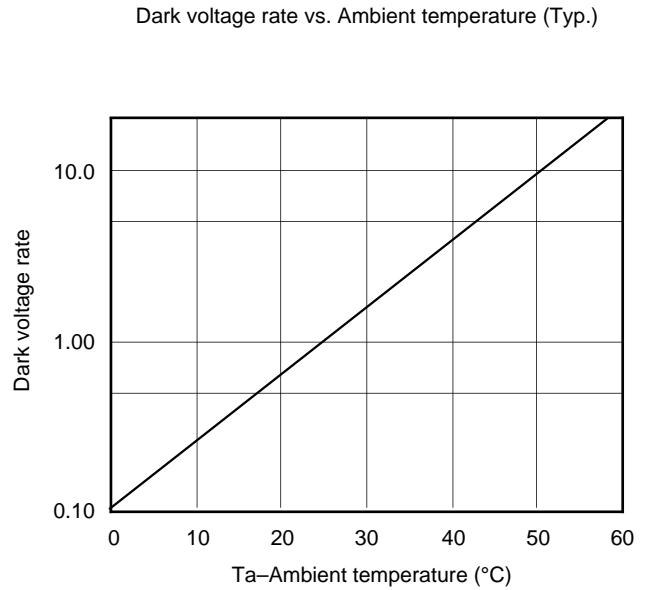
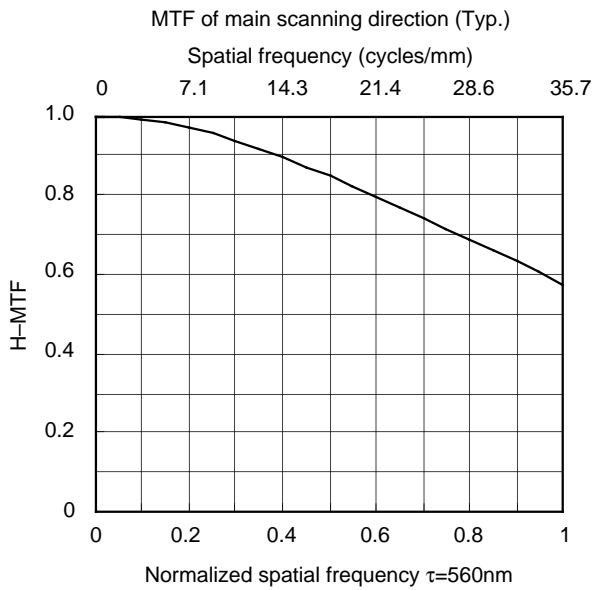
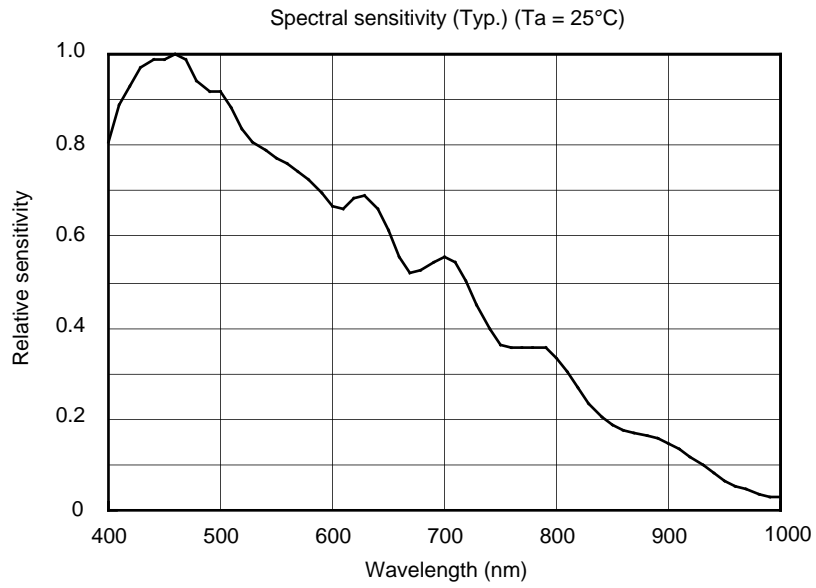


| Item                        | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------|--------|------|------|------|------|
| $\phi$ CLK-VOUT 1           | t10    | 40   | 115  | 280  | ns   |
| $\phi$ CLK-VOUT 2           | t11    | 55   | 120  | 205  |      |
| $\phi$ CLK-VOUT* (with S/H) | t12    | 10   | 165  | 240  |      |

Note 1)  $f_{clk} = 1\text{MHz}$ ,  $\phi$  CLK pulse duty = 50 %,  $\phi$  CLK pulse rise/fall time = 10 ns

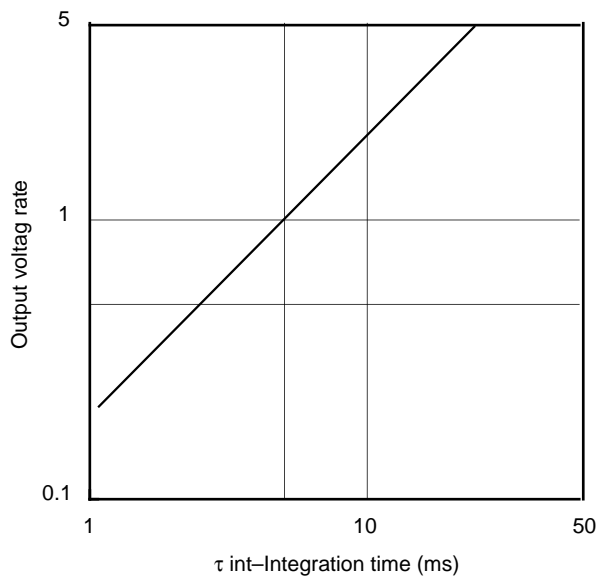
Note 2) Output waveform when internal S/H is in use.

Note 3) ● indicates the correspondence of clock pulse and data period.

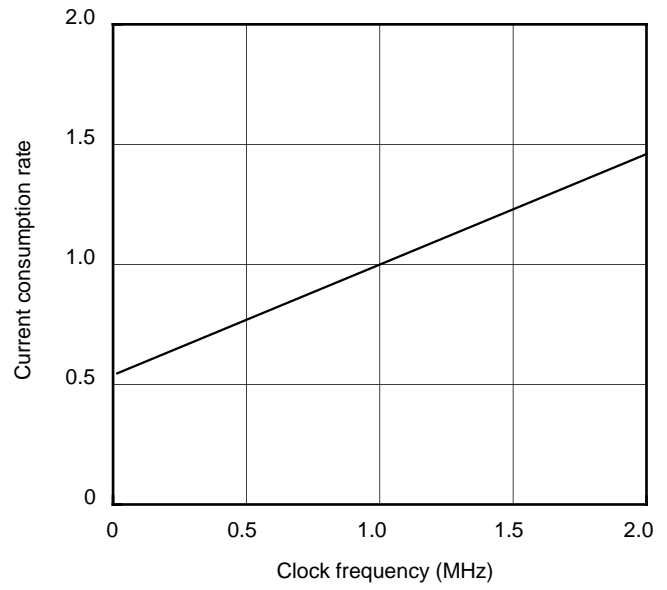




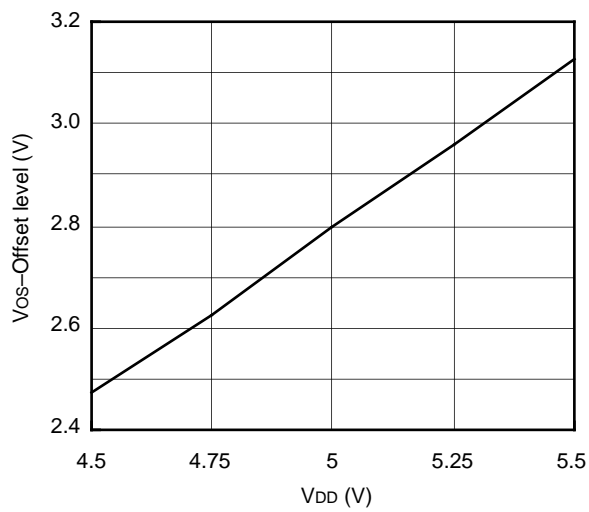
Output voltage rate vs. Integration time (Typ.)



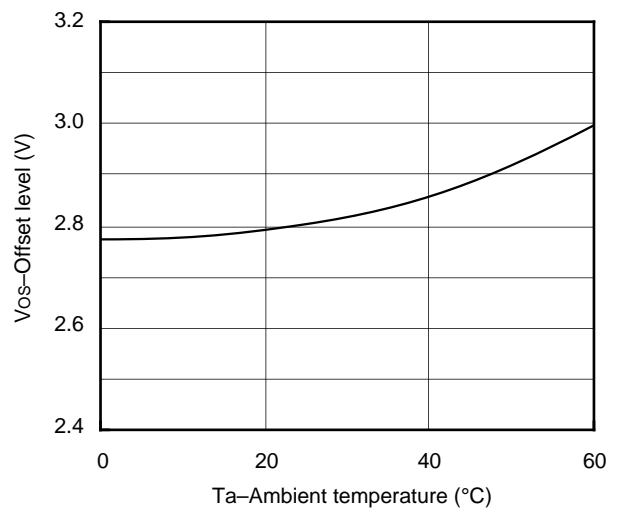
Current consumption rate vs. Clock frequency (Typ.)



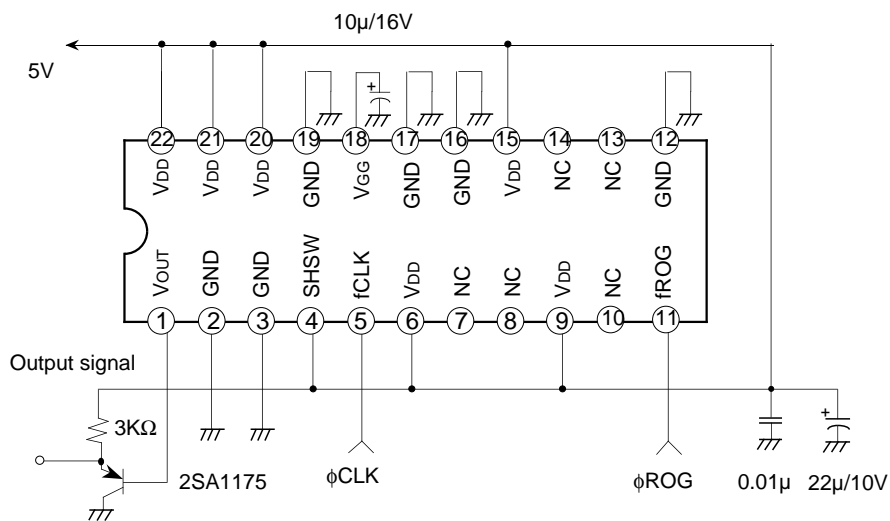
Offset level vs. VDD (Typ.)



Offset level vs. Ambient temperature (Typ.)



Application Circuit (Without S/H mode (Note))



Note) This circuit diagram is the case when internal S/H is not used.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## Notes on Handling

### 1) Static charge prevention

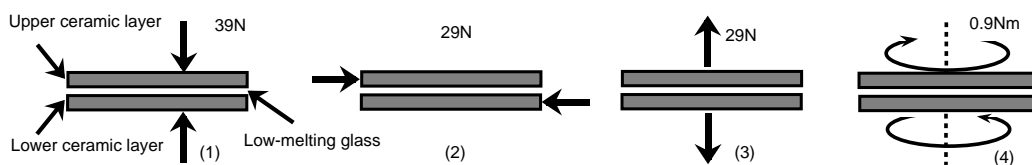
CCD image sensors are easily damaged by static discharge. Before handling, be sure to take the following protective measures.

- Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
- When handling directly use an earth band.
- Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- Ionized air is recommended for discharge when handling CCD image sensors.
- For the shipment of mounted substrates use cartons treated for the prevention of static charges.

### 2) Notes on handling CCD Cer-DIP package

The following points should be observed when handling and installing this package.

- (1) Compressive strength: 39N/surface  
(Do not apply any load more than 0.7 mm inside the outer perimeter of the glass portion.)
- (2) Shearing strength: 29N/surface
- (3) Tensile strength: 29N/surface
- (4) Torsional strength: 0.9Nm



- In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
- Be aware that any of the following can cause the glass to crack because the upper and lower ceramic layers are shielded by low-melting glass.
  - Applying repetitive bending stress to the external leads.
  - Applying heat to the external leads for an extended period of time with a soldering iron.
  - Rapid cooling or heating.
  - Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
  - Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

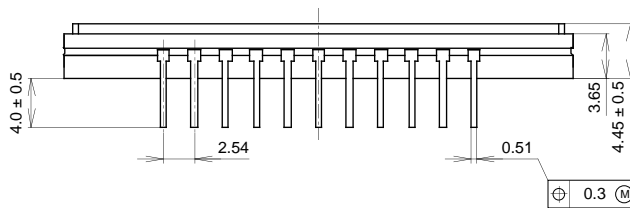
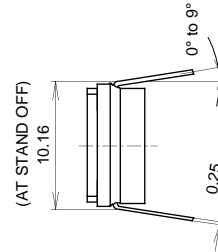
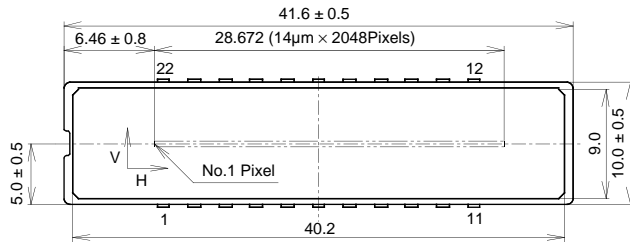
### 3) Soldering

- Make sure the package temperature does not exceed 80 °C.
- Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- To dismount image sensors, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

- 4) Dust and dirt protection
  - a) Operate in clean environments.
  - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)
  - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
  - d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- 5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.
- 7) Make sure the input pulse should not be -1 V or below.
- 8) Normal output signal is not obtained immediately after device switch on. Use the output signal added 22500 pulses or above to  $\phi$  CLK clock pulse.

Package Outline Unit : mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is  $2.45 \pm 0.3$ mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

|                  |             |
|------------------|-------------|
| PACKAGE MATERIAL | Cer-DIP     |
| LEAD TREATMENT   | TIN PLATING |
| LEAD MATERIAL    | 42 ALLOY    |
| PACKAGE WEIGHT   | 5.2g        |