Fact Sheet

MPC8560

POWERQUICC™ INTEGRATED COMMUNICATIONS PROCESSOR

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OVERVIEW

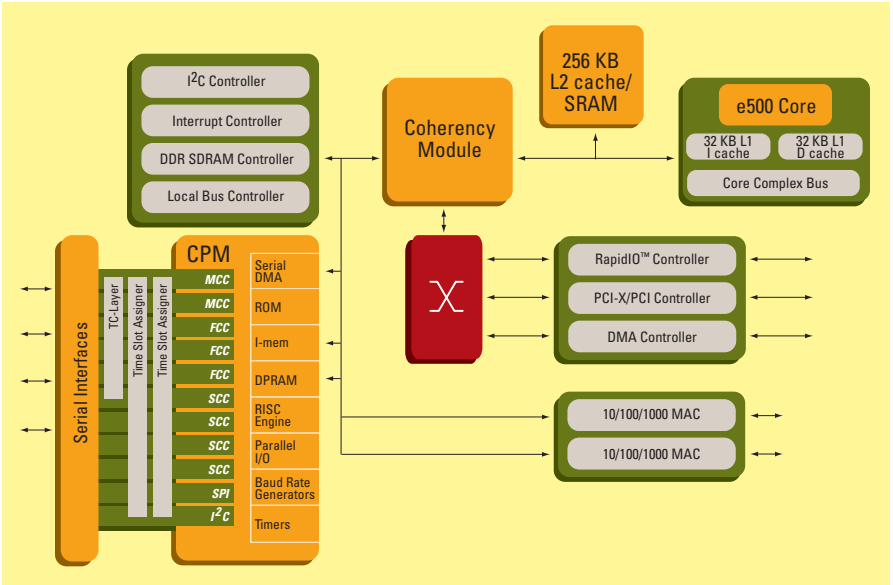
The PowerQUICC III™ is a verstile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. Motorola's PowerQUICC III processor family is the next generation of Motorola's leading PowerQUICC line of integrated communications processors. The PowerQUICC III provides higher performance in all areas of device operation, including greater flexibility, extended capabilities, and higher integration.

PRODUCT HIGHLIGHTS

Motorola's leading PowerQUICC III architecture integrates two processing blocks. One block is a high-performance embedded e500 core. With 256 KB of Level 2 cache, the e500 core implements the enhanced PowerPC Book E instruction-set architecture and provides unprecedented levels of hardware and software debugging support. The second block is the Communications Processor Module (CPM). The CPM of the PowerQUICC III can support three fast serial communications controllers (FCCs), two multichannel controllers (MCCs), four serial communications controllers (SCCs), one serial peripheral interface (SPI), and one I^2C interface. The PowerQUICC III also offers two integrated 10/100/1000 Ethernet controllers, a DDR SDRAM memory controller, a 64-bit PCI-X/PCI controller, and a RapidIO™ interconnect. This high level of integration helps simplify board design and offers significant bandwidth and performance for high-end control-plane and data-plane applications.

TYPICAL APPLICATIONS

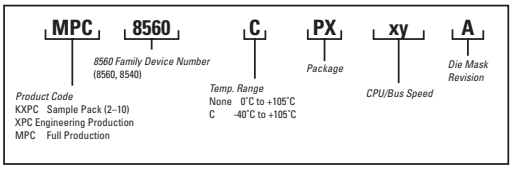
- Remote access concentrators/servers
- Regional office routers
- Wireless infrastructure equipment
- Telecommunications switching and transmission equipment
- Ethernet switches
- T1/E1 and T3/E3 Line Cards
- OC-3 Line Card
- LAN- to WAN-router
- DSLAMs
- Multi-service access platforms
- Optical Networking
- IP Networking
- SONET transmission controller
- Media Gateways
- IP Virtual Private Networks (VPN)



TECHNICAL SPECIFICATIONS

- Embedded e500 Book E compatible core available from 600 MHz up to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 1850 MIPS at 800 MHz (est. Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
  - SIMD extension with single precision floating point
- High-performance RISC CPM available at up to 333 MHz
  - CPM software compatibility with previous families
  - Greater than 1 Gbps aggregate CPM bandwidth
  - 32 KB of dual-port RAM
  - 128 KB of ROM + 32 KB of RAM for protocol microcode storage
  - Two UTOPIA Level II master/slave ports with multi-PHY support (one can be 16-bit)
  - Three MII interfaces
  - Eight TDM interfaces (T1/E1), two TDM ports that can be interfaced with T3/E3
  - Four SCCs supporting HDLC and SDLC, HDLC bus, UART, Transparent, BISYNC
  - Three FCCs supporting:
    - Up to 155 Mbps ATM SAR-AAL0, AAL1, AAL2, AAL3/4, AAL5
    - 10/100 Mbps Ethernet (up to three) IEEE 802.3X
    - 45 Mbps HDLC/transparent (up to three)
  - Two MCCs each supporting 128 full-duplex, 64 kbps, HDLC lines for a total of 256 channels
  - ATM transmission convergence layer capabilities (8 channels)
  - Integrated inverse multiplexing for ATM (IMA) functionality
- Two TSECs supporting 10/100/1000 Mbps Ethernet (IEEE 802.3, 802.3u, 802.3x, 802.3z, and 802.3ac compliant) with two GMII/TBI/RGMII interfaces
- 166 MHz, 64-bit, 2.5V I/O, DDR SDRAM memory controller with full ECC support
- 500 MHz, 8-bit, LVDS I/O, RapidIO controller
- 133 MHz, 64-bit, 3.3V I/O, PCI-X 1.0a/PCI 2.2 bus controller
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Interrupt controller
- IEEE 1149.1 JTAG test access port
- 1.2V core power supply with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

PowerQUICC III™	MPC8560	MPC8540
Core	e500	e500
I-Cache/D-Cache (KB)	32/32	32/32
Integrated L2 Cache (KB)	256	256
Fast Communications Controllers	3	-
Serial Communications Controllers	4	-
Ethernet (10/100 only)	up to 3	1
Ethernet (10/100/1000)	2	2
Utopia Level II Ports	2	-
Multi-Channel HDLC	up to 256	-
PCI-X/PCI Interface	Yes	Yes
RapidIO Interface	Yes	Yes
IMA Functionality	Yes	-
TC-Layer Capabilities	Yes	-



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