# Winbond LPC I/O
# W83627THF

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## W83627THF Data Sheet Revision History

| | PAGES | DATES | VERSION | WEB VERSION | MAIN CONTENTS |
|---|---|---|---|---|---|
| 1 | N.A. | 01/16/2003 | 0.50 | | First published preliminary version. |
| 2 | P.104<br>P.117~120 | 03/25/2003 | 0.60 | | SUSLED data correction.<br>Add Item 7.8.9 |
| 3 | P.116~122 | 04/10/2003 | 0.70 | | Update Appendix A to demo circuit |

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## 1. GENERAL DESCRIPTION

W83627THF is a Winbond LPC I/O product. It integrates the following major peripheral functions in a chip: the disk driver adapter (FDC), serial port (UART), parallel port (SPP/EPP/ECP), keyboard controller (KBC), SIR, game port, MIDI port, hardware monitor, ACPI, On Now Wake-Up features.

The disk drive adapter functions of W83627THF include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83627THF greatly reduces the number of components required for interfacing with floppy disk drives. The W83627THF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s.

The W83627THF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupts system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps, which support higher speed modems. In addition, the W83627THF provides IR functions: IrDA 1.0 (SIR for 1.152K bps)

The W83627THF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83627THF provides functions that complies with ACPI (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through PME# or PSOUT#

function pins. For OnNow keyboard Wake-Up, OnNow mouse Wake-Up. The W83627THF also has auto power management to reduce the power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware are available with optional AMIKEY™-2, Phoenix MultiKey/42™, or customer code.

The W83627THF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

The W83627THF is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover, W83627THF is made to meet the specification of PC2001's requirement in the power management: ACPI 1.0/1.0b/2.0 and DPM (Device Power Management).

The W83627THF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices. They are very important for an entertainment or consumer computer.

The W83627THF supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83627THF support the Smart Fan control system, including the “Thermal Cruise™” and “Speed Cruise™” functions. Smart Fan can make system more stable and user friendly.

The special characteristic of Super I/O product line is to avoid power rails short. This is especially true to a multi-power system where power partition is much more complex than a single-power one. Special care might be applied during layout stage or the IC will fail even though its intended function is OK.

## 2. FEATURES

### General

Meet LPC Spec. 1.1

Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)

Compliant with Microsoft PC98/PC2001 Hardware Design Guide

Support DPM (Device Power Management), ACPI

Programmable configuration settings

Single 24 or 48 MHz clock input

### FDC

Compatible with IBM PC AT disk drive systems

Variable write pre-compensation with track selectable capability

Support vertical recording format

DMA enable logic

16-byte data FIFOs

Support floppy disk drives and tape drives

Detects all overrun and underrun conditions

Built-in address mark detection circuit to simplify the read electronics

FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)

Support up to four 3.5-inch or 5.25-inch floppy disk drives

Completely compatible with industry standard 82077

360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

Support 3-mode FDD, and its Win95/98/NT/2K/XP driver

### UART

Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs

MIDI compatible

Fully programmable serial-interface characteristics:

--- 5, 6, 7 or 8-bit characters

--- Even, odd or no parity bit generation/detection

--- 1, 1.5 or 2 stop bits generation

Internal diagnostic capabilities:

--- Loop-back controls for communications link fault isolation

--- Break, parity, overrun, framing error simulation

Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to ($2^{16}$-1)

Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

### Infrared

Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

### Parallel Port

Compatible with IBM parallel port

Support PS/2 compatible bi-directional parallel port

Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification

Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification

Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port

Enhanced printer port back-drive current protection

### Keyboard Controller

Asynchronous Access to Two Data Registers and One status Register

Software compatibility with the 8042

Support PS/2 mouse

Support port 92

Support both interrupt and polling modes

Fast Gate A20 and Hardware Keyboard Reset

8 Bit Timer/ Counter

Support binary and BCD arithmetic

6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

### Game Port

Support two separate Joysticks

Support every Joystick two axis (X, Y) and two button (A, B) controllers

### MIDI Port

The baud rate is 31.25 K baud rate

16-byte input FIFO

16-byte output FIFO

### General Purpose I/O Ports

6 sets programmable general purpose I/O ports

General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, KBC control I/O pins, suspend LED output, RSMRST# signal, PWROK signal, STR (suspend to DRAM) function, VID control function,

### OnNow Functions

Keyboard Wake-Up by programmable keys

Mouse Wake-Up by programmable buttons

On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

## Hardware Monitor Functions

Smart fan control system, support "Thermal Cruise™" and "Speed Cruise™"

3 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium™ II/III/4 thermal diode output

4 external voltage detect inputs.

3 intrinsic voltage monitoring (typical for Vbat, +5VSB , +5VCC)

3 fan speed monitoring inputs

3 fan speed control (DC analog output)

Build in Case open detection circuit

WATCHDOG comparison of all monitored values

Programmable hysteresis and setting points for all monitored items

Over temperature indicate output

Issue SMI#, IRQ, OVT# to activate system protection

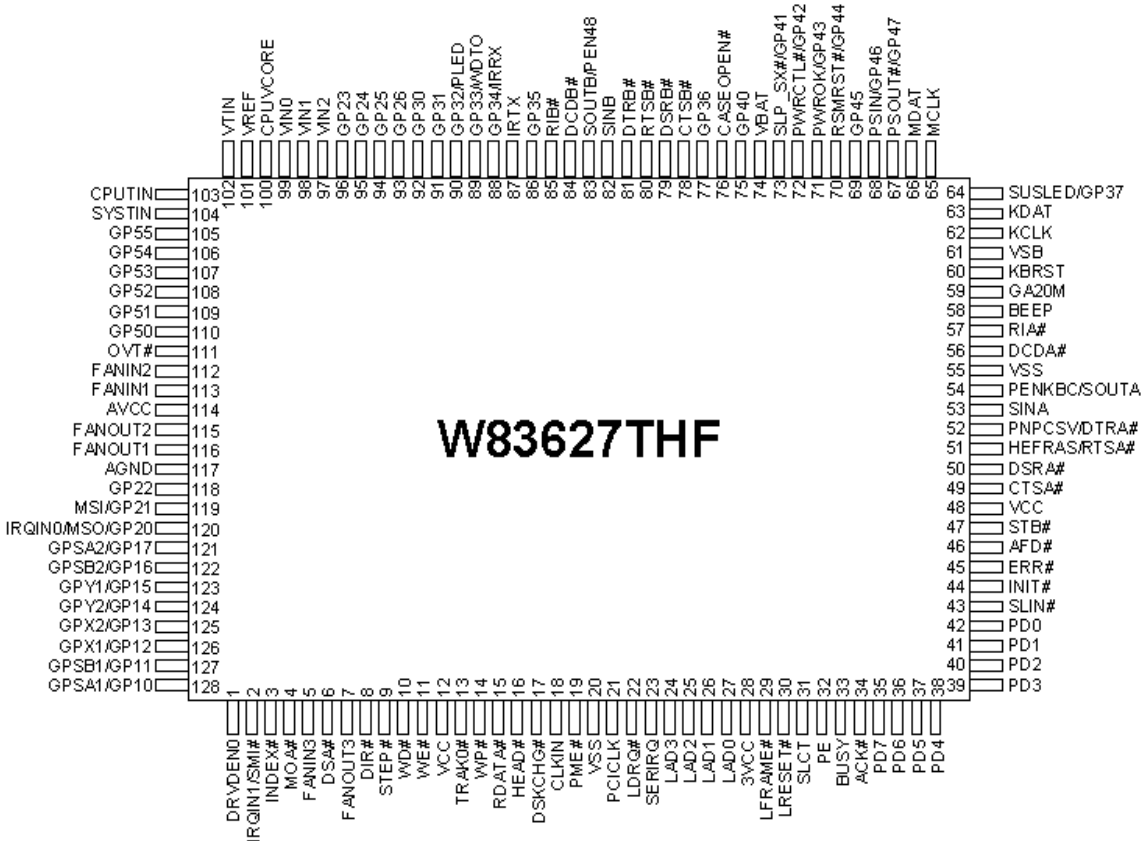
Winbond Hardware Doctor™ Support

Intel LDCM™ compatible

## Package

128-pin PQFP

## PIN CONFIGURATION FOR 627THF



## 3. PIN DESCRIPTION

Note: Please refer to Section 6.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin

AIN - Analog input pin

$IN_{cs}$ - CMOS level Schmitt-triggered input pin

$IN_{t}$ - TTL level input pin

$IN_{td}$ - TTL level input pin with internal pull down resistor

$IN_{ts}$ - TTL level Schmitt-triggered input pin

$IN_{tsp3}$ - 3.3V TTL level Schmitt-triggered input pin

$IN_{tu}$ - TTL level input pin with internal pull up resistor

$I/O_{8t}$ - TTL level bi-directional pin with 8 mA source-sink capability

$I/O_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability

$I/O_{12tp3}$ - 3.3 V TTL level bi-directional pin with 12 mA source-sink capabilities

$I/OD_{12ts}$ - TTL level bi-directional Schmitt-triggered pin. Open-drain output with 12 mA sink capability

$I/OD_{12tp3}$ - 3.3 V TTL level bi-directional pin. Open-drain output with 12 mA sink capability

$I/OD_{16cs}$ - CMOS level Schmitt-triggered bi-directional pin. Open-drain output with 16 mA sink capability

$I/OD_{24t}$ - TTL level bi-directional pin. Open-drain output with 24 mA sink capability

$OUT_{12tp3}$ - 3.3V TTL level output pin with 12 mA source-sink capability

$OUT_{8}$ - TTL level output pin with 8 mA source-sink capability

$OUT_{12}$ - TTL level output pin with 12 mA source-sink capability

$OUT_{24}$ - TTL level output pin with 24 mA source-sink capability

$OD_{8}$ - Open-drain output pin with 8 mA sink capability

$OD_{12}$ - Open-drain output pin with 12 mA sink capability

$OD_{24}$ - Open-drain output pin with 24 mA sink capability

### 3.1 LPC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| CLKIN | 18 | $IN_t$ | System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input. |
| PME# | 19 | $OD_8$ | Generated PME event. |
| PCICLK | 21 | $IN_{tsp3}$ | PCI 33 MHz clock input. |
| LDRQ# | 22 | $OUT_{12tp3}$ | Encoded DMA Request signal. |
| SERIRQ | 23 | $I/OD_{12tp3}$ | Serial IRQ input/Output. |
| LAD[3:0] | 24-27 | $I/O_{12tp3}$ | These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. |
| LFRAME# | 29 | $IN_{tsp3}$ | Indicates start of a new cycle or termination of a broken cycle. |
| LRESET# | 30 | $IN_{tsp3}$ | Reset signal. It can connect to PCIRST# signal on the host. |

### 3.2 FDC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| DRVDEN0 | 1 | $OD_{24}$ | Drive Density Select bit 0. |
| INDEX# | 3 | $IN_{cs}$ | This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| MOA# | 4 | $OD_{24}$ | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. |
| DSA# | 6 | $OD_{24}$ | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output. |
| DIR# | 8 | $OD_{24}$ | Direction of the head step motor. An open drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion |
| STEP# | 9 | $OD_{24}$ | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |
| WD# | 10 | $OD_{24}$ | Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output. |
| WE# | 11 | $OD_{24}$ | Write enable. An open drain output. |
| TRAK0# | 13 | $IN_{cs}$ | Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| WP# | 14 | $IN_{cs}$ | Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| RDATA# | 15 | $IN_{cs}$ | The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| HEAD# | 16 | $OD_{24}$ | Head select. This open drain output determines which disk drive head is active.<br>Logic 1 = side 0<br>Logic 0 = side 1 |
| DSKCHG# | 17 | $IN_{cs}$ | Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |

### 3.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SLCT | 31 | $IN_t$ | PRINTER MODE:<br>An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. |
| PE | 32 | $IN_t$ | PRINTER MODE:<br>An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| BUSY | 33 | $IN_t$ | PRINTER MODE:<br>An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. |
| ACK# | 34 | $IN_t$ | PRINTER MODE: ACK#<br>An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| ERR# | 45 | $IN_t$ | PRINTER MODE: ERR#<br>An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| SLIN# | 43 | $OD_{12}$ | PRINTER MODE: SLIN#<br>Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| INIT# | 44 | $OD_{12}$ | PRINTER MODE: INIT#<br>Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| AFD# | 46 | $OD_{12}$ | PRINTER MODE: AFD#<br>An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |

3.3 Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| STB# | 47 | $OD_{12}$ | PRINTER MODE: STB#<br>An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD0 | 42 | $I/O_{12t}$ | PRINTER MODE: PD0<br>Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD1 | 41 | $I/O_{12t}$ | PRINTER MODE: PD1<br>Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD2 | 40 | $I/O_{12t}$ | PRINTER MODE: PD2<br>Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: WP2# |
| PD3 | 39 | $I/O_{12t}$ | PRINTER MODE: PD3<br>Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD4 | 38 | $I/O_{12t}$ | PRINTER MODE: PD4<br>Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD5 | 37 | $I/O_{12t}$ | PRINTER MODE: PD5<br>Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD6 | 36 | $I/O_{12t}$ | PRINTER MODE: PD6<br>Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| PD7 | 35 | $I/O_{12t}$ | PRINTER MODE: PD7<br>Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |

### 3.4 Serial Port Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| CTSA# | 49 | $IN_t$ | Clear To Send. It is the modem control input.<br>The function of these pins can be tested by reading bit 4 of the handshake status register. |
| CTSB# | 78 | $IN_t$<br>$I/O_{12t}$ | Clear To Send. It is the modem control input.<br>The function of these pins can be tested by reading bit 4 of the handshake status register. |
| DSRA# | 50 | $IN_t$ | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| DSRB# | 79 | $IN_t$ | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| RTSA#<br>HEFRAS | 51 | $I/O_{8t}$ | UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.<br>During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address) |
| RTSB# | 80 | $I/O_{8t}$ | UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. |
| DTRA#<br>PNPCSV# | 52 | $I/O_{8t}$ | UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.<br>During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, PRT, Game port and MIDI port) |
| DTRB# | 81 | $I/O_{8t}$ | UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. |
| SINA | 53 | $IN_t$ | Serial Input. It is used to receive serial data through the communication link. |
| SINB | 82 | $IN_{tt}$ | Serial Input. It is used to receive serial data through the communication link. |

3.4 Serial Port Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SOUTA<br>PENKBC | 54 | $I/O_{8t}$ | UART A Serial Output. It is used to transmit serial data out to the communication link.<br>During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (ENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC) |
| SOUTB<br>PEN48 | 83 | $I/O_{8t}$ | UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up. |
| DCDA# | 56 | $IN_t$ | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. |
| DCDB# | 84 | $IN_t$ | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. |
| RIA# | 57 | $IN_t$ | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. |
| RIB# | 85 | $IN_t$ | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. |

## 3.5 KBC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GA20M | 59 | $OUT_{12}$ | Gate A20 output. This pin is high after system reset. (KBC P21) |
| KBRST | 60 | $OUT_{12}$ | Keyboard reset. This pin is high after system reset. (KBC P20) |
| KDAT | 63 | $I/OD_{16cs}$ | Keyboard Data. |
| MCLK | 65 | $I/OD_{16cs}$ | PS2 Mouse Clock. |
| MDAT | 66 | $I/OD_{16cs}$ | PS2 Mouse Data. |

### 3.6 Hardware Monitor Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| BEEP | 58 | $OD_8$ | Beep function for hardware monitor. This pin is low after system reset. |
| CASEOPEN# | 76 | $IN_t$ | CASE OPEN. An active low input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83627THF is power off. |
| VIN1 | 98 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VIN0 | 99 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VIN2 | 97 | AIN | 0V to 4.096V FSR Analog Inputs. |
| CPUVCORE | 100 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VREF | 101 | AOUT | Reference Voltage for temperature maturation. |
| VTIN | 102 | AIN | Temperature sensor 3 inputs. It is used for temperature maturation. |
| CPUTIN | 103 | AIN | Temperature sensor 2 inputs. It is used for CPU1 temperature maturation. |
| SYSTIN | 104 | AIN | Temperature sensor 1 input. It is used for system temperature maturation. |
| OVT# | 111 | $OD_{12}$ | Over temperature Shutdown Output. It indicated the temperature is over temperature limit. |
| FANIN3<br>FANIN2<br>FANIN1 | 5<br>112<br>113 | $I/O_{12ts}$ | 0V to +5V amplitude fan tachometer input. |
| FANOUT1<br>FANOUT2<br>FANOUT3 | 116<br>115<br>7 | AOUT | Fan speed control. Output analog voltage level to control the Fan's speed. |

## 3.7 Game Port

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GPSA1<br>GP10 | 128 | $IN_{cs}$<br>$I/OD_{12cs}$ | Active-low, Joystick I switch input 1. (Default)<br>General purpose I/O port 1 bit 0. |
| GPSB1<br>GP11 | 127 | $IN_{cs}$<br>$I/OD_{12cs}$ | Active-low, Joystick II switch input 1. (Default)<br>General purpose I/O port 1 bit 1. |
| GPX1<br>GP12 | 126 | $I/OD_{12cs}$ | Joystick I timer pin. this pin connects to X positioning variable resistors for the Joystick. (Default)<br>General purpose I/O port 1 bit 2. |
| GPX2<br>GP13 | 125 | $I/OD_{12cs}$<br>$I/OD_{12cs}$ | Joystick II timer pin. this pin connects to X positioning variable resistors for the Joystick. (Default)<br>General purpose I/O port 1 bit 3. |
| GPY2<br>GP14 | 124 | $I/OD_{12cs}$<br>$I/OD_{12cs}$ | Joystick II timer pin. this pin connects to Y positioning variable resistors for the Joystick. (Default)<br>General purpose I/O port 1 bit 4. |
| GPY1<br>GP15 | 123 | $I/OD_{12cs}$<br>$I/OD_{12cs}$ | Joystick I timer pin. this pin connects to Y positioning variable resistors for the Joystick. (Default)<br>General purpose I/O port 1 bit 5. |
| GPSB2<br>GP16 | 122 | $IN_{cs}$<br>$I/OD_{12cs}$ | Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default)<br>General purpose I/O port 1 bit 6. |
| GPSA2<br>GP17 | 121 | $IN_{cs}$<br>$I/OD_{12cs}$ | Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default)<br>General purpose I/O port 1 bit 7. |

## 3.8 General Purpose I/O Port

### 3.8.1 General Purpose I/O Port 1 (Power source is Vcc)

see 1.7 Game Port

### 3.8.2 General Purpose I/O Port 2 (Power source is Vcc)

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GP20<br>MSO<br>IRQIN0 | 120 | $I/OD_{12t}$<br>$OUT_{12}$<br>$IN_t$ | General purpose I/O port 2 bit 0.<br>MIDI serial data output. (Default)<br>IRQ channel input 0. |
| GP21<br>MSI | 119 | $I/OD_{12t}$<br>$IN_{tu}$ | General purpose I/O port 2 bit 1.<br>MIDI serial data input. It is internally pulled up by a 40 K ohms resistor. (Default) |
| GP22 | 118 | $I/OD_{12t}$ | General purpose I/O port 2 bit 2. (Default) |
| GP23 | 96 | $I/OD_{12t}$ | General purpose I/O port 2 bit 3. (Default) |
| GP24 | 95 | $I/OD_{12t}$ | General purpose I/O port 2 bit 4. (Default) |
| GP25 | 94 | $I/OD_{12t}$ | General purpose I/O port 2 bit 5. (Default) |
| GP26 | 93 | $I/OD_{12t}$ | General purpose I/O port 2 bit 6. (Default) |
| SMI#<br>IRQIN1 | 2 | $OD_{24}$<br>$IN_t$ | System Management Interrupt channel output.<br>IRQ channel input 1. |

### 3.8.3 General Purpose I/O Port 3, 4 (Power source is VSB)

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GP30 | 92 | $I/OD_{12t}$ | General purpose I/O port 3 bit 0. |
| GP31 | 91 | $I/OD_{12t}$ | General purpose I/O port 3 bit 1. |
| GP32<br>PLED | 90 | $I/OD_{24t}$<br>$OUT_{24}$ | General purpose I/O port 3 bit 2.<br>Power LED output. |
| GP33<br>WDTO | 89 | $I/OD_{12t}$<br>$OUT_{12}$ | General purpose I/O port 3 bit 3. (Default)<br>Watchdog time out output. |
| GP34<br>IRRX | 88 | $I/OD_{12ts}$<br>$IN_{ts}$ | General purpose I/O port 3 bit 4.<br>IRRX input. (Default) |
| IRTX | 87 | $OUT_{12}$ | Infrared Transmitter Output. (Default) |
| GP35 | 86 | $I/OD_{12t}$ | General purpose I/O port 3 bit 5. (Default) |
| GP37<br>SUSLED/ | 64 | $I/OD_{24t}$<br>$OUT_{24}$ | General purpose I/O port 3 bit 7.<br>Suspend LED output, it can program to flash when suspend state. This function can work without VCC. (Default) |
| GP40 | 75 | $I/OD_{8t}$ | General purpose I/O port 4 bit 0. |
| GP41<br>SLP_SX# | 73 | $I/OD_{12t}$<br>$IN_{t}$ | General purpose I/O port 4 bit 1.<br>SLP_S3# input. (Default) |
| GP42<br>PWRCTL# | 72 | $I/OD_{12t}$<br>$OD_{12}$ | General purpose I/O port 4 bit 2.<br>This pin generates the PWRCTL# signal while the power failure. (Default) |
| GP43<br>PWROK | 71 | $I/OD_{12t}$<br>$OD_{12}$ | General purpose I/O port 4 bit 3.<br>This pin generates the PWROK signal while the VCC come in. (Default) |
| GP44<br>RSMRST# | 70 | $I/OD_{12t}$<br>$OD_{12}$ | General purpose I/O port 4 bit 4.<br>This pin generates the RSMRST signal while the VSB come in. (Default) |
| GP45 | 69 | $I/OD_{12t}$ | General purpose I/O port 4 bit 5. |
| GP46<br>PSIN | 68 | $I/OD_{12t}$<br>$IN_{td}$ | General purpose I/O port 4 bit 6.<br>Panel Switch Input. This pin is high active with an internal pull down resistor. (Default) |
| GP47<br>PSOUT# | 67 | $I/OD_{12t}$<br>$OD_{12}$ | General purpose I/O port 4 bit 7.<br>Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low. (Default) |

### 3.8.4 General Purpose I/O Port 5 (Power source is VCC)

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GP50 | 110 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 0. |
| GP51 | 109 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 1. |
| GP52 | 108 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 2. |
| GP53 | 107 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 3. |
| GP54 | 106 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 4. |
| GP55 | 105 | $I/O_{12tp3}$ | General purpose I/O port 5 bit 5. |

## 3.9 POWER PINS

| SYMBOL | PIN | FUNCTION |
|---|---|---|
| VCC | 12, 48 | +5V power supply for the digital circuitry. |
| 5VSB | 61 | +5V stand-by power supply for the digital circuitry. |
| 3VCC | 28 | +3.3V power supply for driving 3V on host interface. |
| AVCC | 114 | Analog VCC input. Internally supplier to all analog circuitry. |
| VBAT | 74 | Battery voltage input. |
| AGND | 117 | Analog ground. |
| GND | 20, 55 | Ground. |

## 3.10 GPIO PIN Power Source

| SYMBOL | POWER SOURCE |
|---|---|
| GPIO port 1 | Vcc |
| GPIO port 2 | Vcc |
| GPIO port 3 | $V_{SB}$ |
| GPIO port 4 | $V_{SB}$ |
| GPIO port 5 | Vcc |

## 4. GENERAL PURPOSE I/O

W83627THF provides 36 input/output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 36 GP I/O ports are divided into five groups . The first and fifth groups are configured through control registers in logical device 7, the second group in logical device 8, and the third and forth groups in logical device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (CRF0/F3: 0 = output, 1 = input). Invert port value by setting inversion register (CRF2/F5: 0 = non-inverse, 1 = inverse). Port value is read/written through data register (CRF1/CRF4). Table 2.1 and 2.2 gives more details on GPIO's assignment. Figure 2-1 shows the GP I/O port's structure. After Power-on reset, those ports default to perform basic input function which maintains its previous settings until a battery loss condition.

| SELECTION BIT<br>0 = OUTPUT<br>1 = INPUT | INVERSION BIT<br>0 = NON INVERSE<br>1 = INVERSE | BASIC I/O OPERATIONS |
|---|---|---|
| 0 | 0 | Basic non-inverting output |
| 0 | 1 | Basic inverting output |
| 1 | 0 | Basic non-inverting input |
| 1 | 1 | Basic inverting input |

Table 2-1

Table 2-2

| GP I/O PORT DATA REGISTER | REGISTER BIT ASSIGNMENT | GP I/O PORT |
|---|---|---|
| GP1(VCC POWER) | BIT 0 | GP10 |
| | BIT 1 | GP11 |
| | BIT 2 | GP12 |
| | BIT 3 | GP13 |
| | BIT 4 | GP14 |
| | BIT 5 | GP15 |
| | BIT 6 | GP16 |
| | BIT 7 | GP17 |
| GP2(VCC POWER) | BIT 0 | GP20 |
| | BIT 1 | GP21 |
| | BIT 2 | GP22 |
| | BIT 3 | GP23 |
| | BIT 4 | GP24 |
| | BIT 5 | GP25 |
| | BIT 6 | GP26 |
| GP3(VRTC POWER) | BIT 0 | GP30 |
| | BIT 1 | GP31 |
| | BIT 2 | GP32 |
| | BIT 3 | GP33 |
| | BIT 4 | GP34 |
| | BIT7 | GP37 |
| GP4(VRTC POWER) | BIT 0 | GP40 |
| | BIT 1 | GP41 |
| | BIT 2 | GP42 |
| | BIT3 | GP43 |
| | BIT 4 | GP44 |
| | BIT5 | GP45 |
| | BIT6 | GP46 |
| | BIT 7 | GP47 |

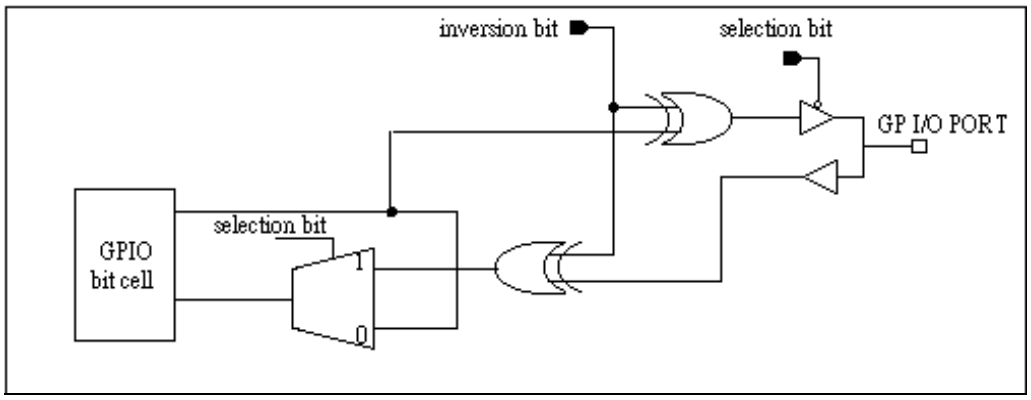



Figure 2-1

# 5. HARDWARE MONITOR

## 5.1 General Description

The W83627THF can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83627THF provides LPC interface to access hardware .

An 8-bit analog-to-digital converter (ADC) was built inside W83627THF. The W83627THF can simultaneously monitor 3 analog voltage inputs (addition monitor VBAT, 5VSB & 5VCC power), 3 fan tachometer inputs, 3 remote temperature inputs and one case-open detection signal. The remote temperature sensing can be performed by thermistors, 2N3904 NPN-type transistors, or directly from Intel™ CPU thermal diode output. Also the W83627THF provides: 3 analog outputs for fan speed control. Beep tone output for warning; SMI#(through Serial IRQ pin), OVT# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters is out of the preset range.

## 5.2 Access Interface

W83627THF uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports is set by W83627THF itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

The register structure is showed as the Figure 3-1

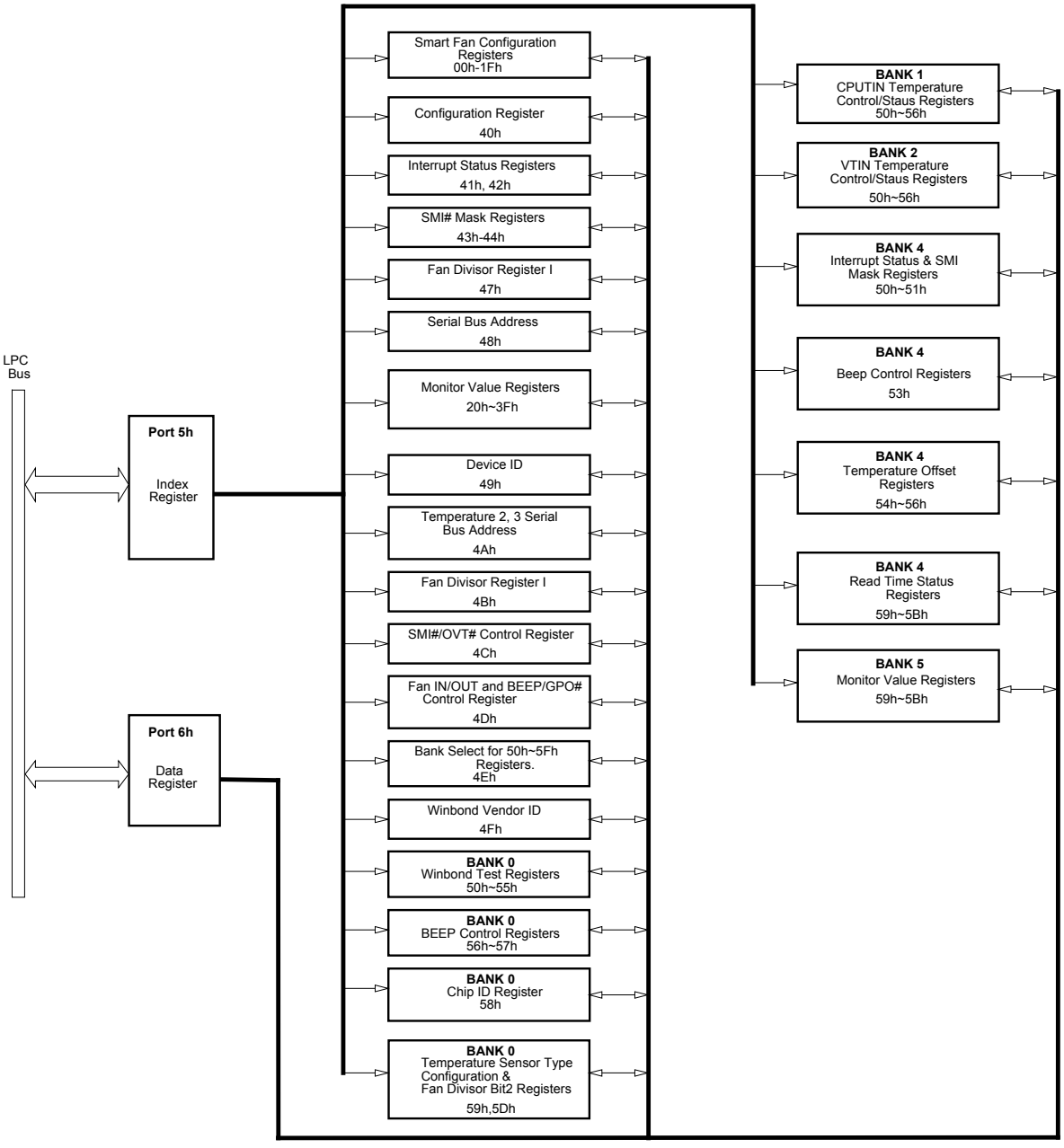



Figure 3-1 : LPC interface access diagram

## 5.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU Vcore voltage, +3.3V, battery(pin 74), AVCC(pin 114) and 5VSB voltage can directly connected to these analog inputs. The +12V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 3.2 shows.

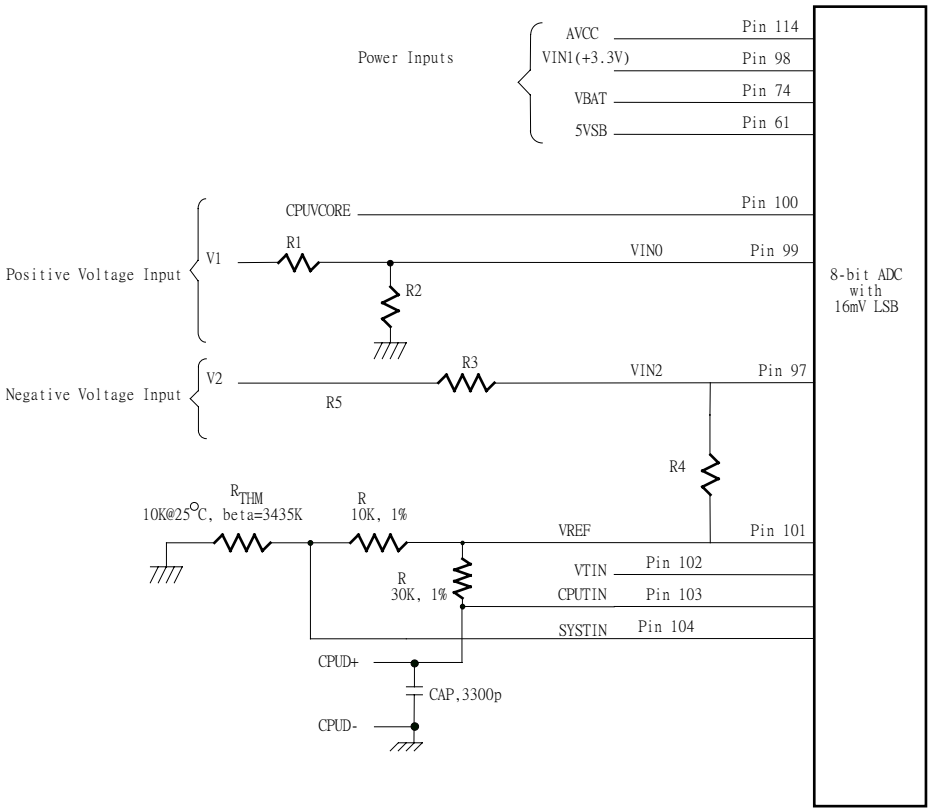



Figure. 3-2

### 5.3.1 Monitor over 4.096V voltage:

The +12V input voltage can be expressed as following equation.

$$VIN0 = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of VIN0 can be subject to less than 4.096V for the maximum input range of the 8-bit ADC.

The -12V input voltage can be expressed as following equation.

$$VIN0 = (V_2 - 3.6) \times \frac{R_4}{R3 + R4} + 3.6, where V_2 = -12$$

The value of R3 and R4 can be selected to 56K Ohms and 232K Ohms, respectively, when the input voltage V2 is -12V. The node voltage of VIN0 can be subject to less than 4.096V for the maximum input range of the 8-bit ADC.

The Pin 114 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83627THF and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The W83627THF internal two serial resistors are 34K ohms and 51K ohms so that input voltage to ADC is 3V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{51K\Omega}{51K\Omega + 34K\Omega} \cong 3V$$

where VCC is set to 5V.

The Pin 61 is connected to 5VSB voltage. W83627THF monitors this voltage and the internal two serial resistors are 34K Ω and 51K Ω so that input voltage to ADC is 3V which less than 4.096V of ADC maximum input voltage.

### 5.3.2 CPUVCORE voltage detection method:

W83627THF provides two detection methods for CPUVCORE(pin100).

(1). VRM8 method:

The LSB of this mode is 16mV. This means that the detected voltage equals to the reading of this voltage register multiplies 16mV. The formula is as the following:

Detected Voltage = $\mathrm{Re}ading * 0.016$ V

(2). VRM9 method: (Default)

The LSB of this mode is 4.88mV which is especially designed for the low voltage CPU. The formula is as the following:

Detected Voltage = $\mathrm{Re}ading * 0.00488 + 0.69$ V

### 5.3.3 Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor SYSTIN and 9-bit two's-complement for sensor CPUTIN and VTIN. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1/Bank2 CR[50h] and the LSB from the Bank1/Bank2 CR[51h] bit 7. The format of the temperature data is show in Table 3-1.

| TEMPERATURE | 8-BIT DIGITAL OUTPUT | | 9-BIT DIGITAL OUTPUT | |
|---|---|---|---|---|
| | 8-Bit Binary | 8-Bit Hex | 9-Bit Binary | 9-Bit Hex |
| +125°C | 0111,1101 | 7Dh | 0,1111,1010 | 0FAh |
| +25°C | 0001,1001 | 19h | 0,0011,0010 | 032h |
| +1°C | 0000,0001 | 01h | 0,0000,0010 | 002h |
| +0.5°C | - | - | 0,0000,0001 | 001h |
| +0°C | 0000,0000 | 00h | 0,0000,0000 | 000h |
| -0.5°C | - | - | 1,1111,1111 | 1FFh |
| -1°C | 1111,1111 | FFh | 1,1111,1110 | 1FFh |
| -25°C | 1110,0111 | E7h | 1,1100,1110 | 1CEh |
| -55°C | 1100,1001 | C9h | 1,1001,0010 | 192h |

Table 3-1

#### *5.3.3.1 Monitor temperature from thermistor:*

The W83627THF can connect three thermistors to measure three different environment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 3-2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (Pin 101).

#### *5.3.3.2 Monitor temperature from Pentium II™/Pentium III™ thermal diode or bipolar transistor 2N3904*

The W83627THF can alternate the thermistor to Pentium II™/Pentium III™ thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 3-3. The pin of Pentium II™/Pentium III™ D- is connected to AGND and the pin D+ is connected to temperature sensor pin in the W83627THF. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

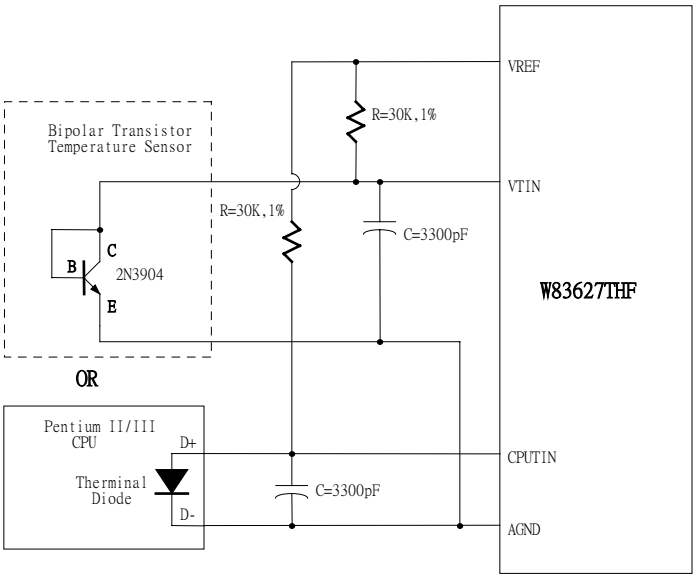



Figure 3-3

## 5.4 FAN Speed Count and FAN Speed Control

### 5.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can't be over VCC. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 3-4 ~ 3-7.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count

.

| DIVISOR | NOMINAL RPM | TIME PER REVOLUTION | COUNTS | 70% RPM | TIME FOR 70% |
|---|---|---|---|---|---|
| 1 | 8800 | 6.82 ms | *153* | 6160 | 9.84 ms |
| **2 (default)** | 4400 | 13.64 ms | *153* | 3080 | 19.48 ms |
| 4 | 2200 | 27.27 ms | *153* | 1540 | 38.96 ms |
| 8 | 1100 | 54.54 ms | *153* | 770 | 77.92 ms |
| 16 | 550 | 109.08 ms | *153* | 385 | 155.84 ms |
| 32 | 275 | 218.16 ms | *153* | 192 | 311.68 ms |
| 64 | 137 | 436.32 ms | *153* | 96 | 623.36 ms |
| 128 | 68 | 872.64 ms | *153* | 48 | 1246.72 ms |

Table 3-2

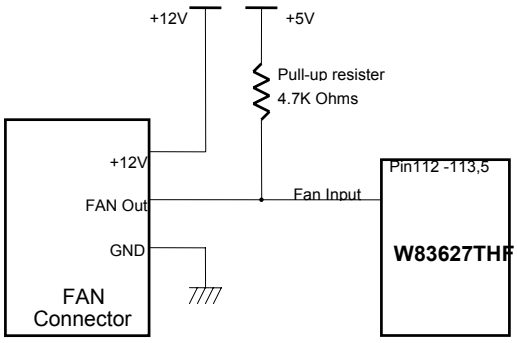



Figure 3-4. Fan with Tach Pull-Up to +5V

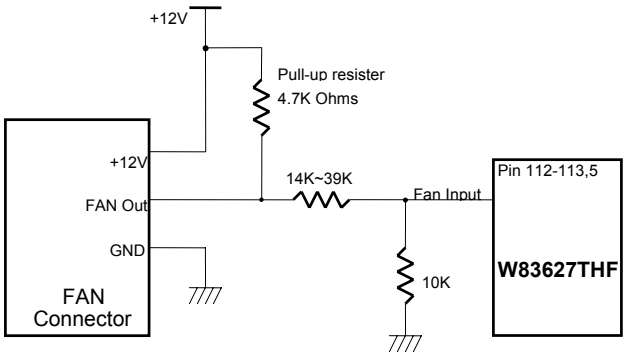
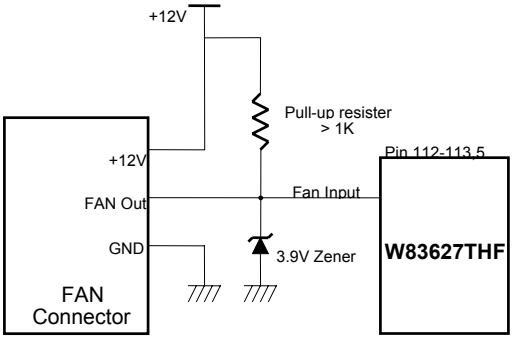
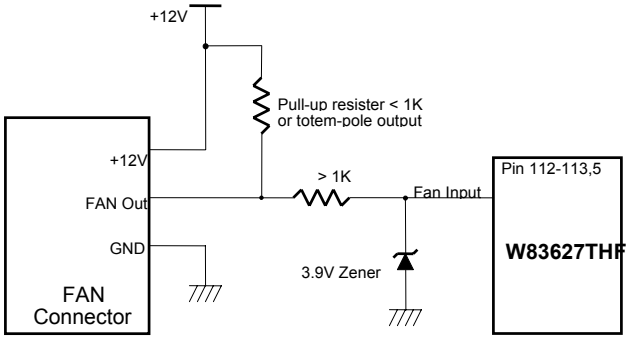



Figure 3-5. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator




and Zener Clamp
Figure 3-6. Fan with Tach Pull-Up to +12V




Totem-Pole Putput and Zener Clamp
Figure 3-7. Fan with Tach Pull-Up to +12V, or

### 5.4.2 Fan speed control

The W83627THF has a 4 bit DAC which produces 0 to 5 volts DC output that provides maximum 3 sets for fan speed control. The analog output can be programmed in the Bank0 Index 01h, Index 03h and Index 11h. The default value is 0xFY,Y is reserved nibble, that is default output value is 5 V. The expression of output voltage can be represented as follow ,

$$\text{OUTPUT VOLTAGE} = AVCC \times \frac{\text{Programmed 4 - bit Register Value}}{16}$$

The application circuit is shown as follow,

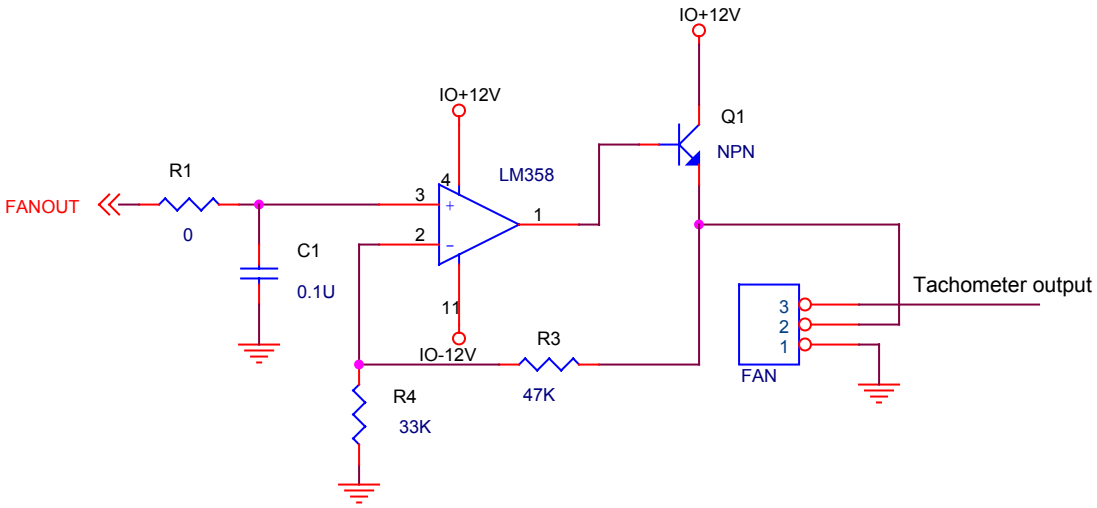



Figure 3-8

Must be take care when choosing the OP-AMP and the transistor. The OP-AMP is used for amplify the 5V range of the DC output up to 12V . The transistor should has a suitable β value to avoid its base current pulling down the OP-AMP 's output and gain the common current to operate the fan at fully speed.

## 5.5 SmartFan™ Control

SmartFan™ Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

### 5.5.1 Thermal Cruise mode

There are maximum 3 pairs of Temperature/FANOUT control at this mode: SYSTIN with FANOUT1, CPUTIN with FANOUT2, VTIN with FANOUT3. At this mode, W83627THF provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3

°C) by BIOS, as long as the real temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature ( 58°C), the fan will be turned on with a specific speed set by BIOS (ex: 3.75 V) and automatically controlled its DC voltage output with the temperature varying. Three conditions may occur :

(1) If the temperature still exceeds the high limit (ex: 58°C), DC Fan output voltage will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit(ex: 58°C) after 3 minutes, a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area(ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), DC Fan output voltage will decrease slowly to 0 until the temperature exceeds the low limit.

Figure 3-9 and 3-10 give the illustration for Thermal Cruise Mode .

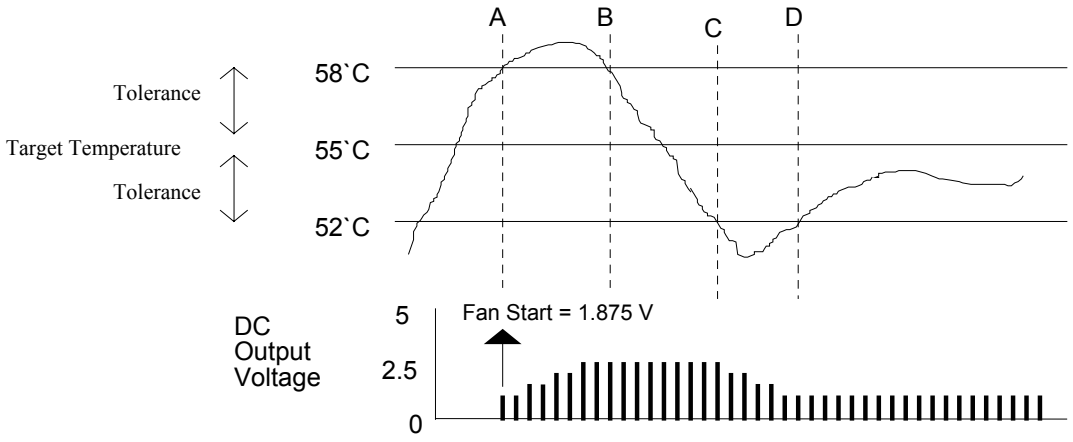



Figure 3-9

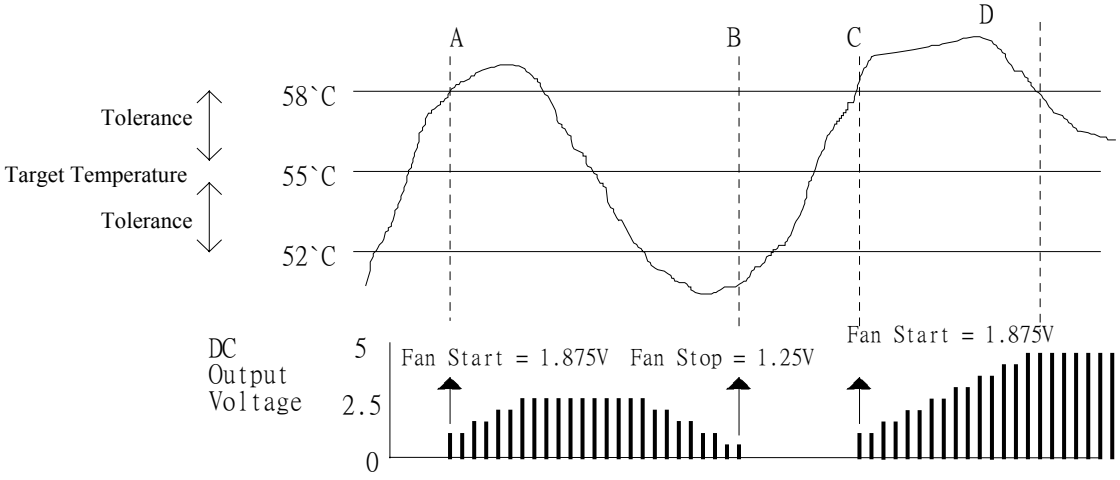



Figure 3-10

One more protection is provided that DC FAN output voltage will not be decreased to 0 in the above (3) situation in order to keep the fans running with a minimum speed. By setting CR[12h] bit3-5 to 1, FAN output voltage will be decreased to the " Stop Value " which are defined at CR[08h],CR[09h] and CR[15h].

### 5.5.2 Fan Speed Cruise mode

There are 3 pairs of FANIN/FANOUT control at this mode: FANIN1 with FANOUT1, FANIN2 with FANOUT2, FANIN3 with FANOUT3. At this mode, W83627THF provides the Smart Fan system which can control the fan speed automatically depend on current fan speeds to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ± 10 ) by BIOS. As long as the fan speed count is the specific range, output voltage will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), output voltage will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit(ex. 160-10), output voltage will be decreased to keep the count higher than the low limit. See Figure 3-11 example.

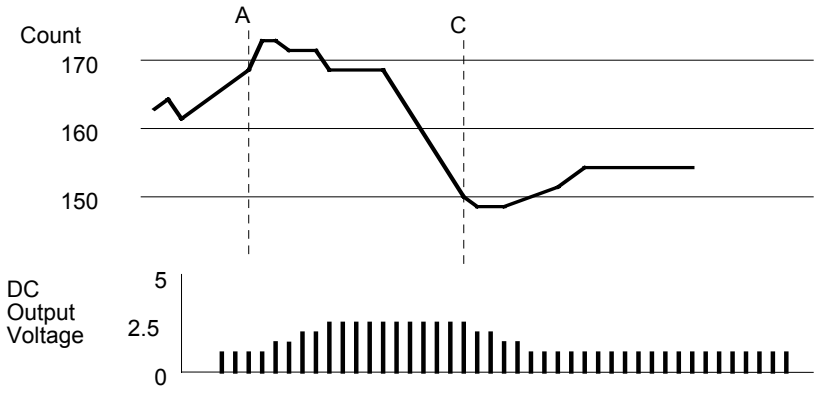



Figure 3-11

### 5.5.3 Manual Control Mode

Smart Fan control system can be disabled and the fan speed control algorithmic can be programmed by BIOS or application software. The programming method is just as section 3.4.2.

## 5.6 SMI# interrupt mode

The SMI#/IRQIN1 pin(pin2) is a multi-function pin. The SMI# function is selected at Configuration Register CR[2Ah] bit 2.

### 5.6.1 Voltage SMI# mode :

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 3-12 )

### 5.6.2 Fan SMI# mode :

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 3-13 )

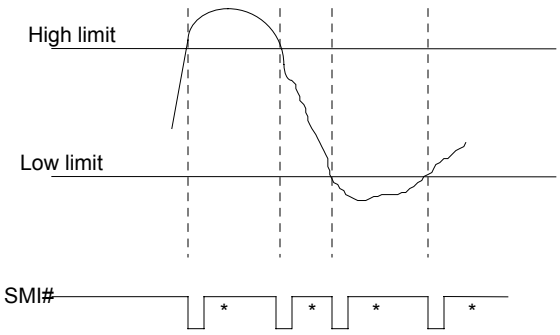



Figure 3-12

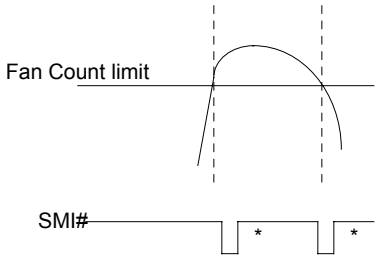



Figure 3-13

*Interrupt Reset when Interrupt Status Registers are read

### 5.6.3 The W83627THF temperature sensor 1(SYSTIN) SMI# interrupt has 3 modes:

**(1) Comparator Interrupt Mode**

Setting the $T_{HYST}$ (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds $T_O$ (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_O$ , the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding $T_O$ and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below $T_O$. (Figure 3-14 ) .

Setting the $T_{HYST}$ lower than $T_O$ will set temperature sensor 1 SMI# to the Interrupt Mode. The following are two kinds of interrupt modes, which are selected by Index 4Ch bit5 :

**(2) Two-Times Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$ , then reset, if the temperature remains above the $T_{HYST}$ , the interrupt will not occur. (Figure 3-15 )

**(3) One-Time Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will not cause an interrupt. Once an interrupt event has occurred by exceeding $T_O$ , then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding $T_O$. (Figure 3-16 )

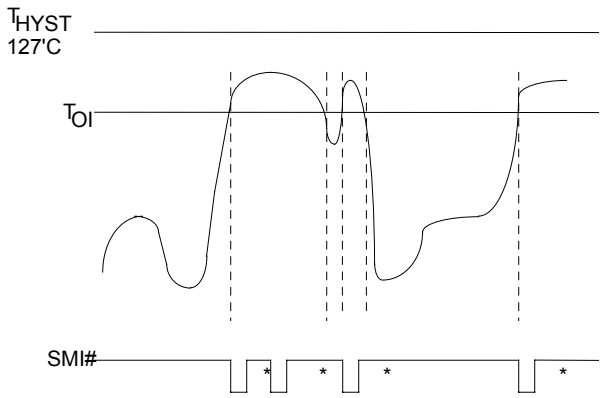



Figure 3-14

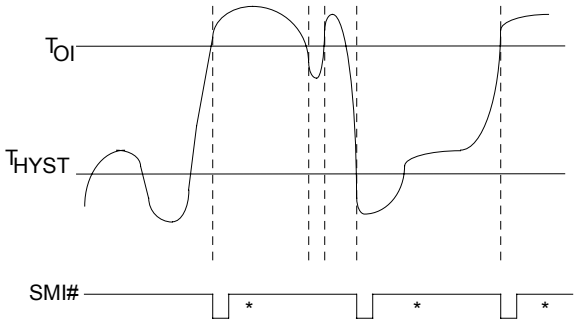
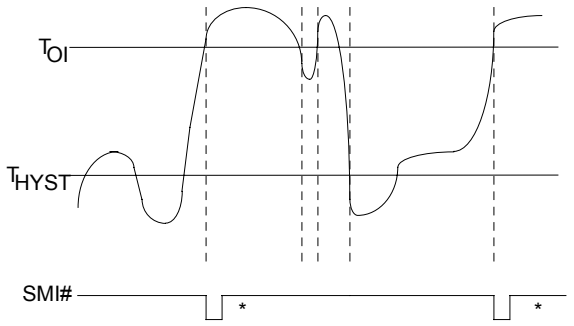



Figure 3-15

*Interrupt Reset when Interrupt Status Registers are read




*Interrupt Reset when Interrupt Status Registers are read

Figure 3-16

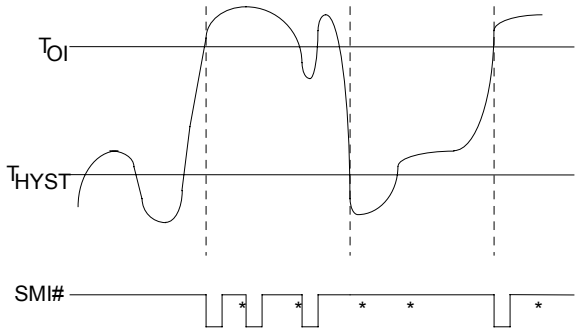
### 5.6.4 The W83627THF temperature sensor 2(CPUTIN) and sensor 3(VTIN) SMI# interrupt has two modes and it is programmed at CR[4Ch] bit 6.

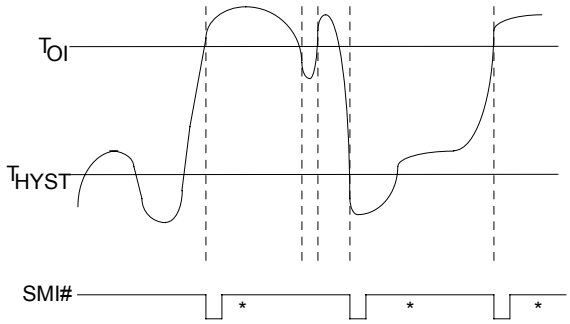
**(1) Comparator Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding $T_O$ and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below $T_{HYST}$. ( Figure 3-17 )

**(2) Two-Times Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$ , then reset, if the temperature remains above the $T_{HYST}$ , the interrupt will not occur. (Figure 3-18 )




*Interrupt Reset when Interrupt Status Registers are read

Figure 3-17

Figure 3-18

## 5.7 OVT# interrupt mode

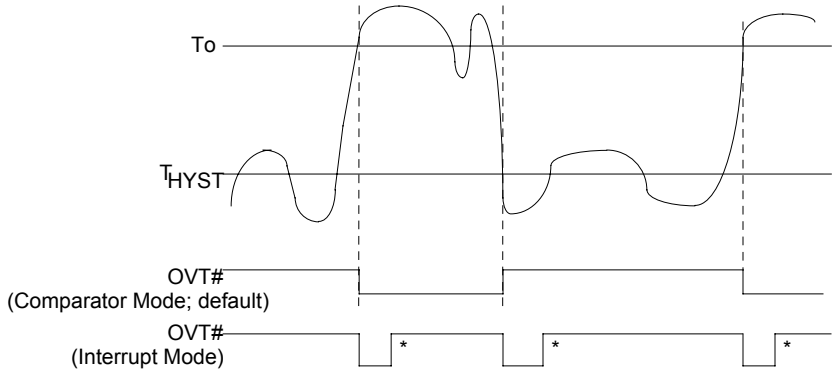
The OVT# mode selection bits are at Bank0 Index18h bit4, Bank1 Index52h bit1 and Bank2 Index52h bit1.

**(1) Comparator Mode :**

Temperature exceeding $T_O$ causes the OVT# output activated until the temperature is less than $T_{HYST}$. ( Figure 3-19)

**(2) Interrupt Mode:**

Temperature exceeding $T_O$ causes the OVT# output activated indefinitely until reset by reading temperature sensor registers. Temperature exceeding $T_O$, then OVT# reset, and then temperature going below $T_{HYST}$ will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding $T_O$ , then reset, if the temperature remains above $T_{HYST}$ , the OVT# will not be activated again.( Figure 3-19)




*Interrupt Reset when Temperature sensor registers are read

Figure 3-19

## 5.8 REGISTERS AND RAM

Address Port and Data Port are set in the register CR60 and CR61 of Logical Device B which is Hardware Monitor Device. The value in CR60 is high byte and that in CR61 is low byte. For example, setting CR60 to 02 and CR61 to 90 cause the Address Port to be 0x295 and Data Port to be 0x296.

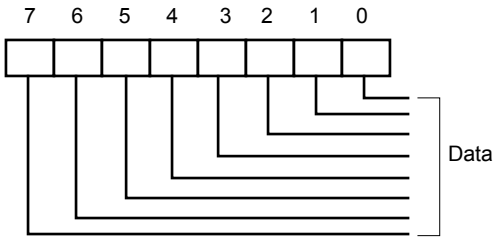
### 5.8.1 Address Port (Port x5h)

Address Port: Port x5h

Power on Default Value 00h

Attribute: Bit 6:0 Read/write , Bit 7: Reserved

Size: 8 bits




Bit7: Reserved

Bit 6-0: Read/Write

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Address Pointer (Power On default 00h) | | | | | | |
| (Power On default 0) | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

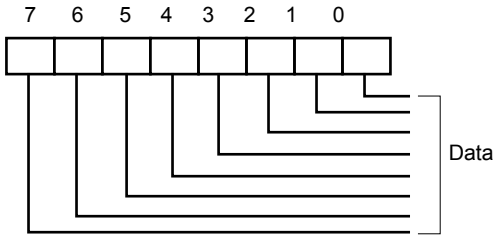
### 5.8.2 Data Port (Port x6h)

Data Port: Port x6h

Power on Default Value 00h

Attribute: Read/write

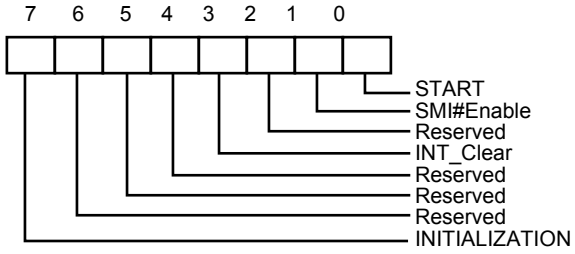
Size: 8 bits




Bit 7-0: Data to be read from or to be written to RAM and Register.

### 5.8.3 Configuration Register — Index 40h

Register Location: 40h
Power on Default Value 03h
Attribute: Read/write
Size: 8 bits




Bit 7: A one restores power on default value to some registers. This bit clears itself since the power on default is zero.

Bit 6: Reserved

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

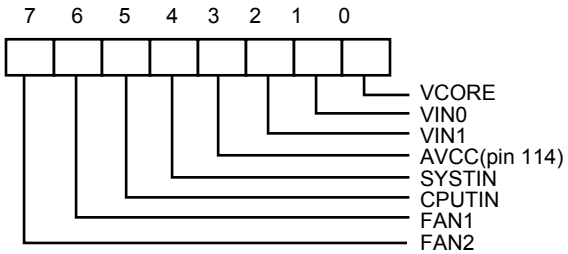
Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

**Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

### 5.8.4 Interrupt Status Register 1— Index 41h

Register Location: 41h
Power on Default Value 00h
Attribute: Read Only
Size: 8 bits



Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.

Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.

Bit 5: A one indicates a High limit of CPUTIN temperature has been exceeded.

Bit 4: A one indicates a High limit of SYSTIN temperature has been exceeded .

Bit 3: A one indicates a High or Low limit of AVCC(pin 114) has been exceeded.

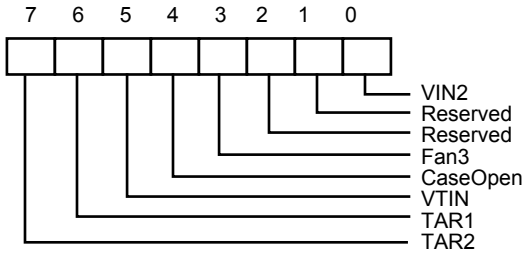
Bit 2: A one indicates a High or Low limit of VIN1 has been exceeded.

Bit 1: A one indicates a High or Low limit of VIN0 has been exceeded.

Bit 0: A one indicates a High or Low limit of VCORE has been exceeded.

### 5.8.5 Interrupt Status Register 2 — Index 42h

Register Location: 42h
Power on Default Value 00h
Attribute: Read Only
Size: 8 bits




Bit 7: A one indicates that the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 6: A one indicates that the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 5: A one indicates a High or Low limit of VTIN temperature has been exceeded.

Bit 4: A one indicates case has been opened.

Bit 3: A one indicates the fan count limit of FAN3 has been exceeded .

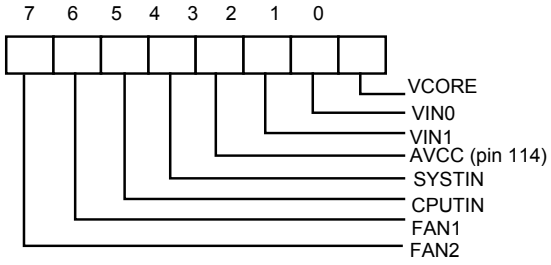
Bit 2: Reserved.

Bit 1: Reserved.

Bit 0: A one indicates a High or Low limit of VIN2 has been exceeded.

### 5.8.6 SMI# Mask Register 1 — Index 43h

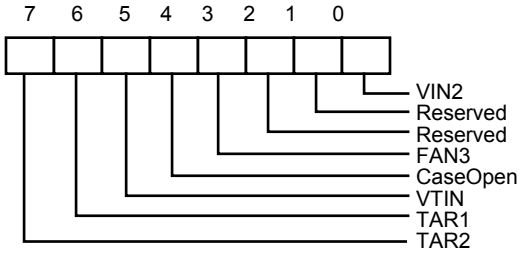
Register Location: 43h
Power on Default Value FEh
Attribute: Read/Write
Size: 8 bits




Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

### 5.8.7 SMI# Mask Register 2 — Index 44h

Register Location: 44h
Power on Default Value FFh
Attribute: Read/Write
Size: 8 bits

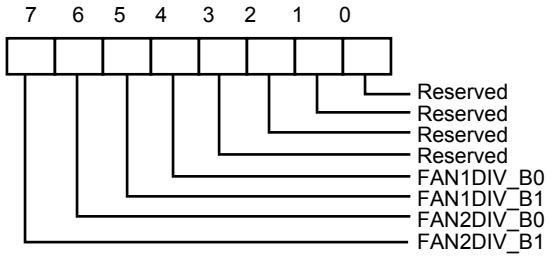



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

### 5.8.8 Reserved Register — Index 45h—46h

### 5.8.9 Fan Divisor Register I — Index 47h

Register Location: 47h
Power on Default Value: 5Fh
Attribute: Read/Write
Size: 8 bits




Bit 7-6: FAN2 Divisor bit1:0 .
Bit 5-4: FAN1 Divisor bit1:0.

Note : Please refer to Bank0 CR[5Dh] , Fan divisor table.

### 5.8.10 Value RAM — Index 20h- 3Fh

| ADDRESS A6-A0 | DESCRIPTION |
|---|---|
| 20h | VCORE reading |
| 21h | VIN0 reading |
| 22h | VIN1 reading |
| 23h | AVCC(pin 114)reading |
| 24h | VIN2 reading |
| 25h | Reserved |
| 26h | Reserved |
| 27h | SYSTIN temperature sensor reading |
| 28h | FAN1 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. |
| 29h | FAN2 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. |

5.8.10 Value RAM — Index 20h- 3Fh, continued

| ADDRESS A6-A0 | DESCRIPTION |
|---|---|
| 2Bh | VCORE High Limit (Power on default value is 1.75V) |
| 2Ch | VCORE Low Limit (Power on default value is 0V) |
| 2Dh | VIN0 High Limit |
| 2Eh | VIN0 Low Limit |
| 2Fh | VIN1 High Limit |
| 30h | VIN1 Low Limit |
| 31h | AVCC(pin 114) High Limit |
| 32h | AVCC(pin 114) Low Limit |
| 33h | VIN2 High Limit |
| 34h | VIN2 Low Limit |
| 35h | Reserved |
| 36h | Reserved |
| 37h | Reserved |
| 38h | Reserved |
| 39h | SYSTIN temperature sensor High Limit |
| 3Ah | SYSTIN temperature sensor Hysteresis Limit |
| 3Bh | FAN1 Fan Count Limit<br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3Ch | FAN2 Fan Count Limit<br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3Dh | FAN3 Fan Count Limit<br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3E- 3Fh | Reserved |

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

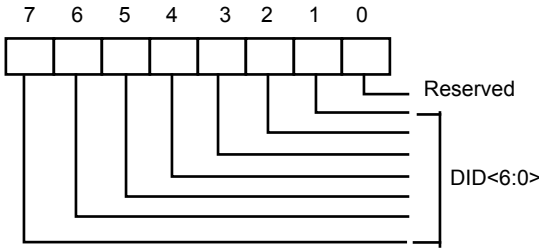
### 5.8.11 Device ID Register - Index 49h

Register Location: 49h

Power on Default Value 03h

Attribute: bit<7:1> Read Only; bit<0> Read/Write

Size: 8 bits




Bit 7-1: Read Only - Device ID<6:0>

Bit 0 :Reserved.

### 5.8.12 Reserved Register — Index 4Ah

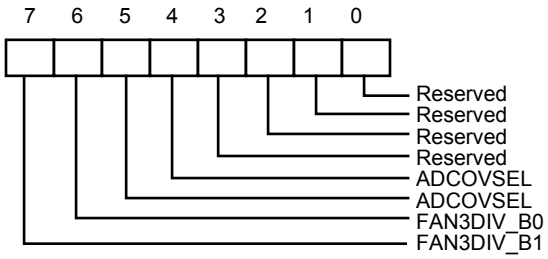
### 5.8.13 Fan Divisor Register II - Index 4Bh

Register Location: 4Bh

Power on Default Value <7:0> 44h.

Attribute: Read/Write

Size: 8 bits




Bit 7-6:Fan3 speed divisor.

Please refer to Bank0 CR[5Dh] , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default. ADC clock select 22.5 Khz.

<5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4)

<5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16)

<5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)

Bit 3-2: These two bits should be set to 01h. The default value is 01h.

Bit 1-0: Reserved.

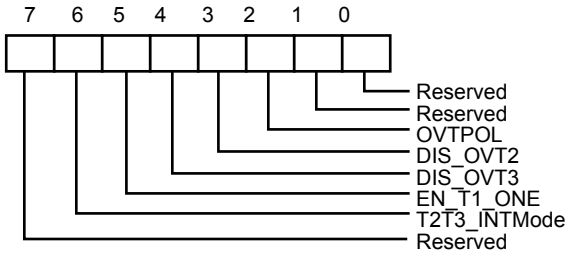
### 5.8.14 SMI#/OVT# Control Register- Index 4Ch

Register Location: 4Ch

Power on Default Value 18h

Attribute: Read/Write

Size: 8 bits




Bit 7: Reserved. User Defined.

Bit 6: Set to 1, the SMI# output type of Temperature CPUTIN/VTIN is set to Comparator Interrupt mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (default 0)

Bit 5: Set to 1, the SMI# output type of temperature SYSTIN is One-Time interrupt mode. Set to 0, the SMI# output type is Two-Times interrupt mode.

Bit 4: Disable temperature sensor VTIN over-temperature (OVT) output if set to 1. Default 0, enable VTIN OVT output through pin OVT#.

Bit 3: Disable temperature sensor CPUTIN over-temperature (OVT) output if set to 1. Default 0, enable CPUTIN OVT output through pin OVT#.

Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

Bit 1: Reserved.

Bit 0: Reserved.

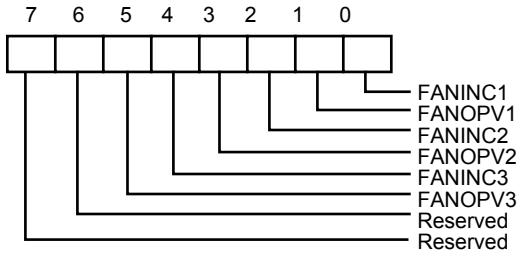
### 5.8.15 FAN IN/OUT and BEEP Control Register- Index 4Dh

Register Location: 4Dh

Power on Default Value 15h

Attribute: Read/Write

Size: 8 bits




Bit 7~6: Reserved.

Bit 5: FAN 3 output value if FANINC3 sets to 0. Write 1, pin 5 generates a logic high signal. Write 0, pin 5 generates a logic low signal. This bit is default 0.

Bit 4: FAN 3 Input Control. Set to 1, pin 5 acts as FAN tachometer input, which is default value. Set to 0, this pin 5 acts as FAN control signal and the output value of FAN control is set by this register bit 5.

Bit 3: FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 112 always generate logic high signal. Write 0, pin 112 always generates logic low signal. This bit default 0.

Bit 2: FAN 2 Input Control. Set to 1, pin 112 acts as FAN tachometer input, which is default value. Set to 0, this pin 112 acts as FAN control signal and the output value of FAN control is set by this register bit 3.

Bit 1: FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 113 always generate logic high signal. Write 0, pin 113 always generates logic low signal. This bit default 0.

Bit 0: FAN 1 Input Control. Set to 1, pin 113 acts as FAN tachometer input, which is default value. Set to 0, this pin 113 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

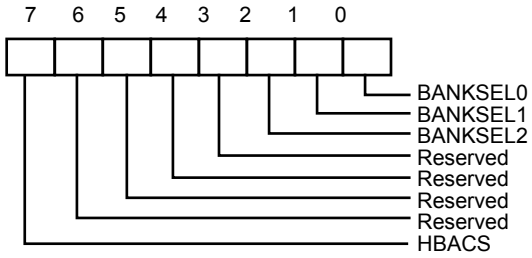
### 5.8.16 Register 50h ~ 5Fh Bank Select Register - Index 4Eh

Register Location: 4Eh

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits




Bit 7: HBACS- High byte access. Set to 1, access Register 4Fh high byte register.

Set to 0, access Register 4Fh low byte register. Default 1.

Bit 6-3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

Set to 0, select Bank0.

Set to 1, select Bank1.

Set to 2, select Bank2.

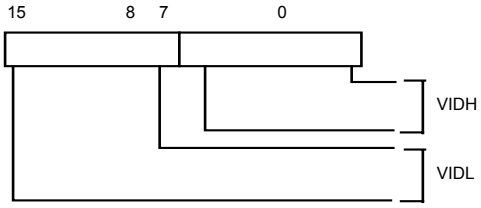
### 5.8.17 Winbond Vendor ID Register - Index 4Fh

Register Location: 4Fh

Power on Default Value <15:0> = 5CA3h

Attribute: Read Only

Size: 16 bits




Bit 15-8: Vendor ID High Byte if CR4E.bit7=1.Default 5Ch.

Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

### 5.8.18 Winbond Test Register -- Index 50h - 55h (Bank 0)

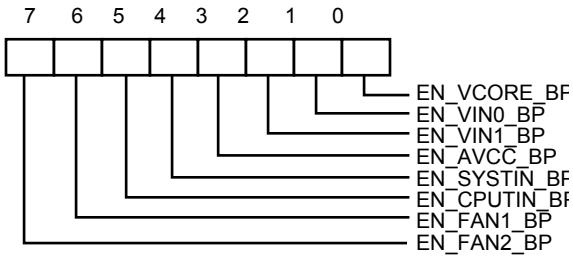
### 5.8.19 BEEP Control Register 1-- Index 56h (*Bank 0*)

Register Location: 56h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: BEEP output control for FAN 2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 6: BEEP output control for FAN 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 5: BEEP output control for temperature CPUTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for temperature SYSTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for AVCC(pin 114) if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2: BEEP output control for VIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN0 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for CPUVCORE if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

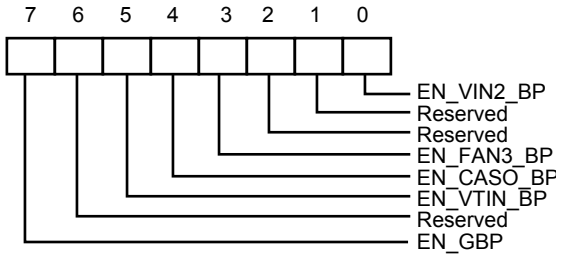
### 5.8.20 BEEP Control Register 2-- Index 57h (*Bank 0*)

Register Location: 57h

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits




Bit 7: Global BEEP Control. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.

Bit 6: Reserved.

Bit 5: BEEP output control for temperature VTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for case open if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for FAN 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2-1: Reserved.

Bit 0: BEEP output control for VIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

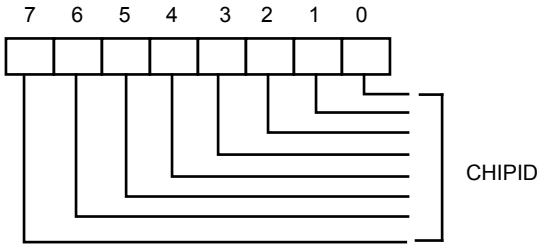
### 5.8.21 Chip ID -- Index 58h (*Bank 0*)

Register Location: 58h

Power on Default Value 90h

Attribute: Read Only

Size: 8 bits




Bit 7-0: Winbond Chip ID number. Read this register will return 90h.

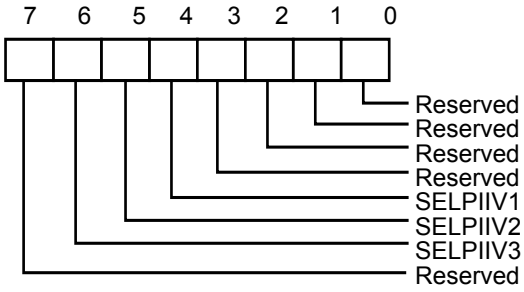
### 5.8.22 Diode Selection Register -- Index 59h (*Bank 0*)

Register Location: 59h

Power on Default Value 70h

Attribute: Read/Write

Size: 8 bits




Bit 7 : Reserved

Bit 6: Diode mode selection of temperature VTIN if index 5Dh bit3 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 5: Diode mode selection of temperature CPUTIN if index 5Dh bit2 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 4: Diode mode selection of temperature SYSTIN if index 5Dh bit1 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 3-0: Reserved

### 5.8.23 Reserved -- Index 5Ah (*Bank 0*)

### 5.8.24 Reserved -- Index 5Bh (*Bank 0*)

### 5.8.25 Reserved -- Index 5Ch (*Bank 0*)

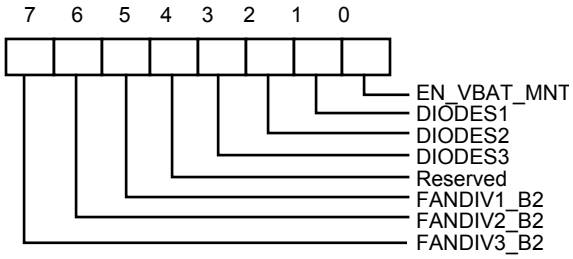
### 5.8.26 VBAT Monitor Control Register -- Index 5Dh (*Bank 0*)

Register Location: 5Dh

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7: Fan3 divisor Bit2.

Bit 6: Fan2 divisor Bit2.

Bit 5: Fan1 divisor Bit2.

Bit 4: Reserved.

Bit 3: Sensor type selection of VTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 2: Sensor type selection of CPUTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor type selection of SYSTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. After set this bit from 0 to 1, the monitored value will be updated to the VBAT reading value register after one monitor cycle time.

**Fan divisor table :**

| Bit 2 | Bit 1 | Bit 0 | Fan Divisor | Bit 2 | Bit 1 | Bit 0 | Fan Divisor |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 16 |
| 0 | 0 | 1 | 2 | 1 | 0 | 1 | 32 |
| 0 | 1 | 0 | 4 | 1 | 1 | 0 | 64 |
| 0 | 1 | 1 | 8 | 1 | 1 | 1 | 128 |

Table 3-3

### 5.8.27 Reserved Register --5Eh (*Bank 0*)

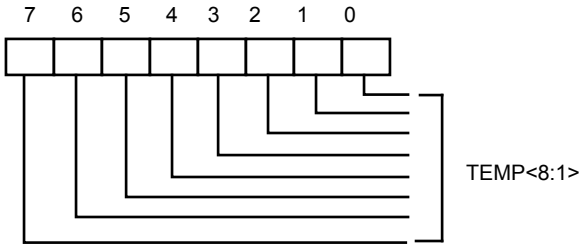
### 5.8.28 Reserved Register --5Fh (*Bank 0*)

### 5.8.29 CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (*Bank 1*)

Register Location: 50h

Attribute: Read Only

Size: 8 bits



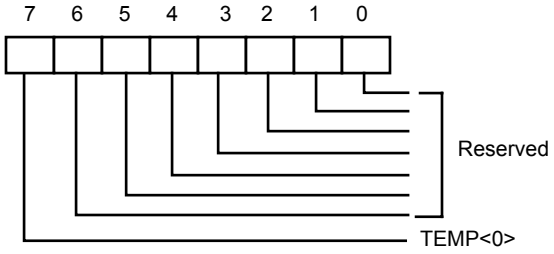

Bit 7: Temperature <8:1> of CPUTIN sensor, which is high byte, means 1°C.

### 5.8.30 CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank 1*)

Register Location: 51h

Attribute: Read Only

Size: 8 bits




Bit 7: Temperature <0> of CPUTIN sensor, which is low byte, means 0.5°C.

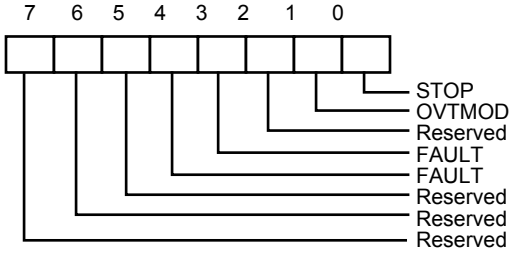
Bit 6-0: Reserved.

### 5.8.31 CPUTIN Temperature Sensor Configuration Register - Index 52h (*Bank 1*)

Register Location: 52h

Power on Default Value 00h

Size: 8 bits




Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

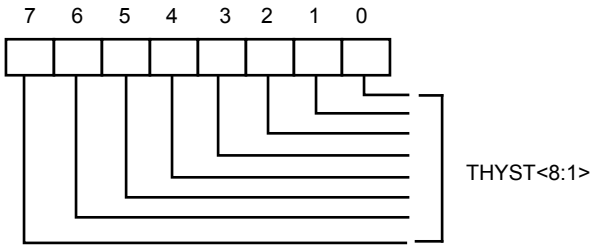
### 5.8.32 CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 1*)

Register Location: 53h

Power on Default Value 4Bh

Attribute: Read/Write

Size: 8 bits




Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

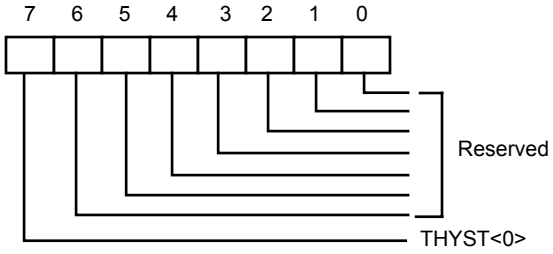
### 5.8.33 CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 1*)

Register Location: 54h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

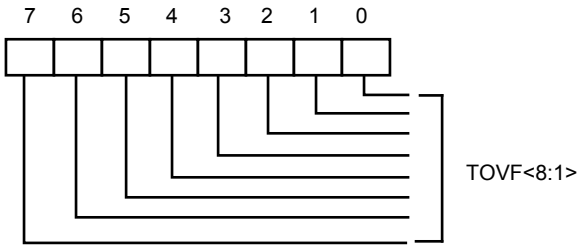
### 5.8.34 CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (*Bank1*)

Register Location: 55h

Power on Default Value 50h

Attribute: Read/Write

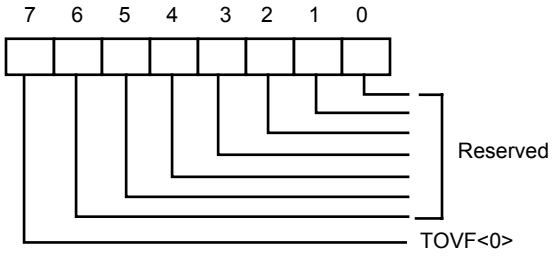
Size: 8 bits




Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

### 5.8.35 CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (*Bank 1*)

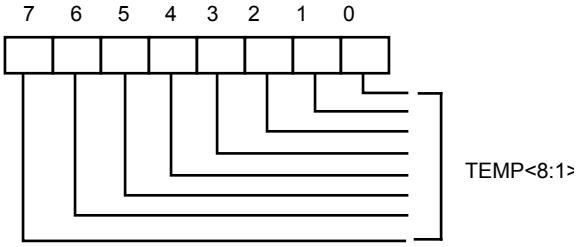
Register Location: 56h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits




Bit 7: Over-temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

### 5.8.36 VTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (*Bank 2*)

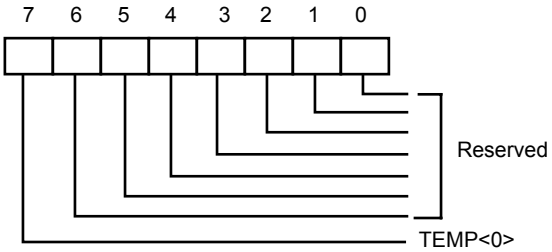
Register Location: 50h
Attribute: Read Only
Size: 8 bits




Bit 7: Temperature <8:1> of sensor 2, which is high byte, means 1°C.

### 5.8.37 VTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank 2*)

Register Location: 51h
Attribute: Read Only
Size: 8 bits

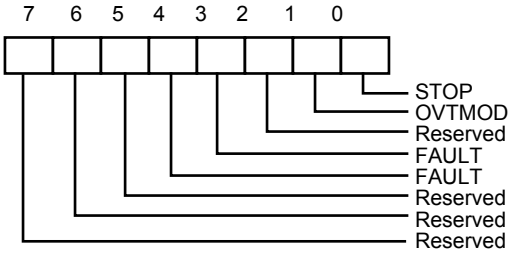



Bit 7: Temperature <0> of sensor3, which is low byte, means 0.5°C.

Bit 6-0: Reserved.

### 5.8.38 VTIN Temperature Sensor Configuration Register - Index 52h (*Bank 2*)

Register Location: 52h
Power on Default Value 00h
Size: 8 bits




Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

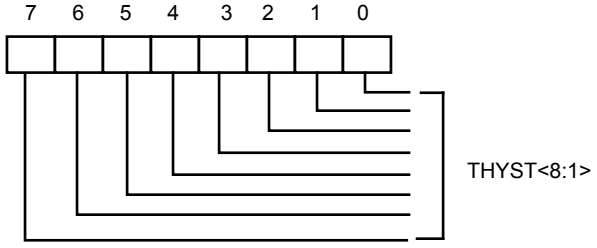
### 5.8.39 VTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 2*)

Register Location: 53h

Power on Default Value 4Bh

Attribute: Read/Write

Size: 8 bits




Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

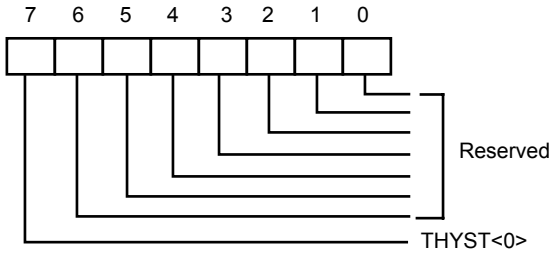
### 5.8.40 VTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 2*)

Register Location: 54h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

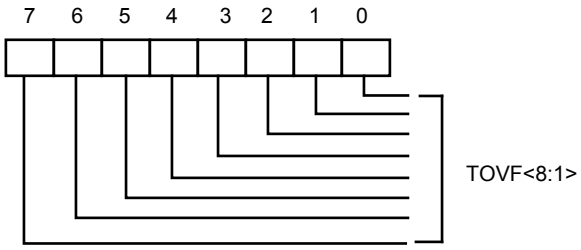
### 5.8.41 VTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (*Bank 2*)

Register Location: 55h

Power on Default Value 50h

Attribute: Read/Write

Size: 8 bits




Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

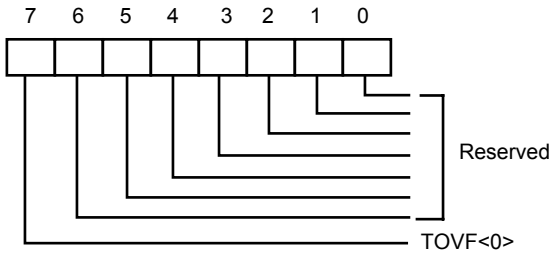
### 5.8.42 VTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (*Bank 2*)

Register Location: 56h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

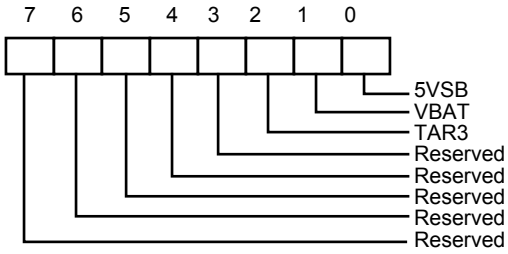
### *5.8.43* Interrupt Status Register 3 -- Index 50h (BANK4)

Register Location: 50h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7-3: Reserved.

Bit 2: A one indicates that the VTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™ .

Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.

Bit 0: A one indicates a High or Low limit of 5VSB has been exceeded.

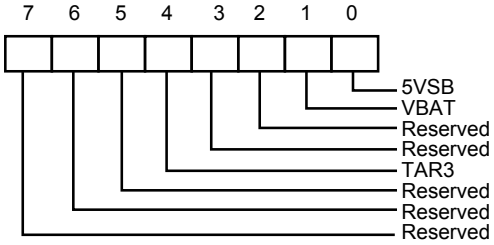
### 5.8.44 SMI# Mask Register 3 -- Index 51h (BANK 4)

Register Location: 51h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits




Bit 7-5: Reserved.

Bit 4: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 2-3: Reserved.

Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

### 5.8.45 Reserved Register -- Index 52h (*Bank 4*)

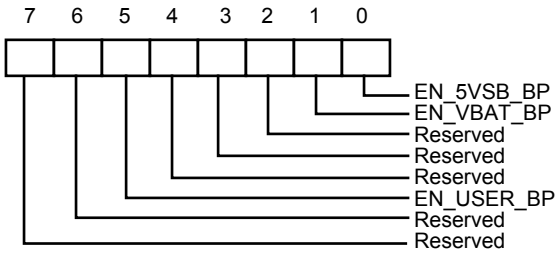
### 5.8.46 BEEP Control Register 3-- Index 53h (*Bank 4*)

Register Location: 53h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)

Bit 4-2: Reserved.

Bit 1: BEEP output control for VBAT if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for 5VSB if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

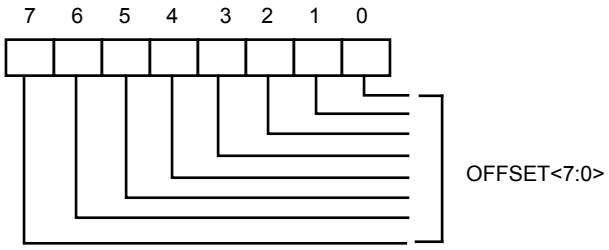
### 5.8.47 SYSTIN Temperature Sensor Offset Register -- Index 54h (*Bank 4*)

Register Location: 54h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7-0: SYSTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

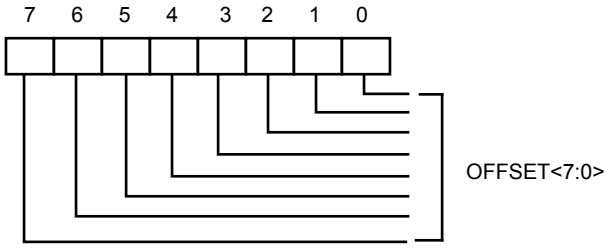
### 5.8.48 CPUTIN Temperature Sensor Offset Register -- Index 55h (*Bank 4*)

Register Location: 55h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7-0: CPUTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

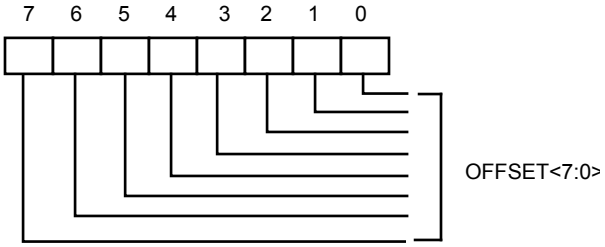
### 5.8.49 VTIN Temperature Sensor Offset Register -- Index 56h (*Bank 4*)

Register Location: 56h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit 7-0: VTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

### 5.8.50 Reserved Register -- Index 57h--58h (*Bank4)*

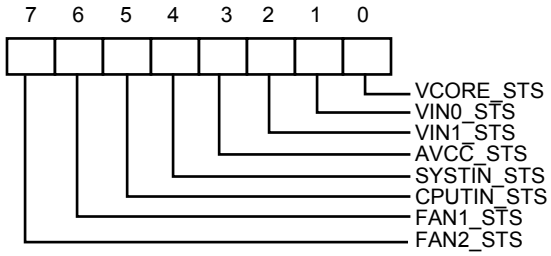
### 5.8.51 Real Time Hardware Status Register I -- Index 59h (*Bank 4*)

Register Location: 59h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 6: FAN 1 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 5: CPUTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 4: SYSTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 3: AVCC Voltage Status. Set 1, the voltage of AVCC is over the limit value. Set 0, the voltage of AVCC is in the limit range.

Bit 2: VIN1 Voltage Status. Set 1, the voltage of VIN1 is over the limit value. Set 0, the voltage of VIN1 is in the limit range.

Bit 1: VIN0 Voltage Status. Set 1, the voltage of VIN0 is over the limit value. Set 0, the voltage of VIN0 is in the limit range.

Bit 0: VCORE Voltage Status. Set 1, the voltage of VCORE is over the limit value. Set 0, the voltage of VCORE is in the limit range.

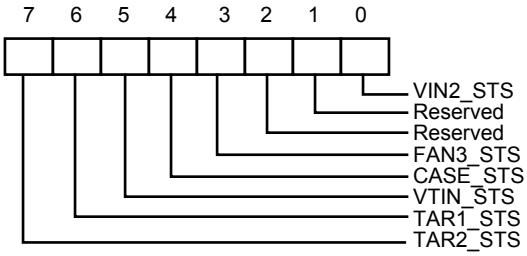
### 5.8.52 Real Time Hardware Status Register II -- Index 5Ah (*Bank 4*)

Register Location: 5Ah

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7: Smart Fan 2 warning status. Set 1, the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 6: Smart Fan 1 warning status. Set 1, the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 5: VTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 4: Case Open Status. Set 1, the case open is detected and latched. Set 0, the case is not latched open.

Bit 3: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 2-1: Reserved.

Bit 0: VIN2 Voltage Status. Set 1, the voltage of VIN2 is over the limit value. Set 0, the voltage of VIN2 is in the limit range.

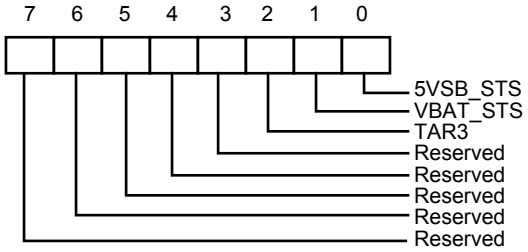
### 5.8.53 Real Time Hardware Status Register III -- Index 5Bh (*Bank 4*)

Register Location: 5Bh

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7-2: Reserved.

Bit 2: Smart Fan 3 warning status. Set 1, the VTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 1: VBAT Voltage Status. Set 1, the voltage of VBAT is over the limit value. Set 0, the voltage of VBAT is during the limit range.

Bit 0: 5VSB Voltage Status. Set 1, the voltage of 5VSB is over the limit value. Set 0, the voltage of 5VSB is in the limit range.

### 5.8.54 Reserved Register -- Index 5Ch (*Bank 4*)

### 5.8.55 Reserved Register -- Index 5Dh (*Bank 4*)

### *5.8.56* Value RAM 2— Index 50h - 5Ah *(BANK 5)*

| ADDRESS A6-A0 | DESCRIPTION |
|---|---|
| 50h | 5VSB reading |
| 51h | VBAT reading. The reading is meaningless if EN_VBAT_MNT bit(CR5D bit0) is not set. |
| 52h | Reserved |
| 53h | Reserved |
| 54h | 5VSB High Limit |
| 55h | 5VSB Low Limit. |
| 56h | VBAT High Limit |
| 57h | VBAT Low Limit |

### 5.8.57 Winbond Test Register -- Index 50h (*Bank 6*)

### 5.8.58 Reserved Register--Index00h (*Bank 0*)

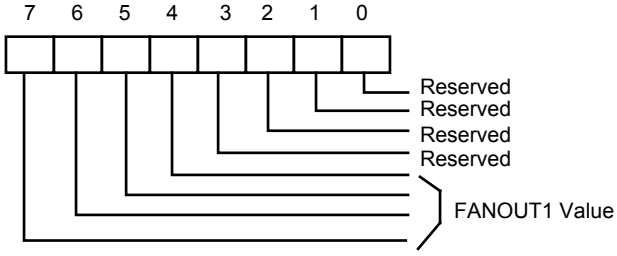
### 5.8.59 FANOUT1 Output Value Control Register-- 01h (*Bank 0*)

Register Location: 01h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits




Bit 7-4: FANPOUT1 voltage control.

$$\textbf{OUTPUT Voltage} = AVCC * \frac{FANOUT}{16}$$

**If AVCC= 5V , output voltage table is**

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | OUTPUT VOLTAGE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2.5 |
| 0 | 0 | 0 | 1 | 0.3125 | 1 | 0 | 0 | 1 | 2.8125 |
| 0 | 0 | 1 | 0 | 0.625 | 1 | 0 | 1 | 0 | 3.125 |
| 0 | 0 | 1 | 1 | 0.9735 | 1 | 0 | 1 | 1 | 3.4375 |
| 0 | 1 | 0 | 0 | 1.25 | 1 | 1 | 0 | 0 | 3.75 |
| 0 | 1 | 0 | 1 | 1.5625 | 1 | 1 | 0 | 1 | 4.0625 |
| 0 | 1 | 1 | 0 | 1.875 | 1 | 1 | 1 | 0 | 4.375 |
| 0 | 1 | 1 | 1 | 2.1875 | 1 | 1 | 1 | 1 | 4.6875 |

Table 3-4 .

### 5.8.60 Reserved Register—Index02h (*Bank 0*)

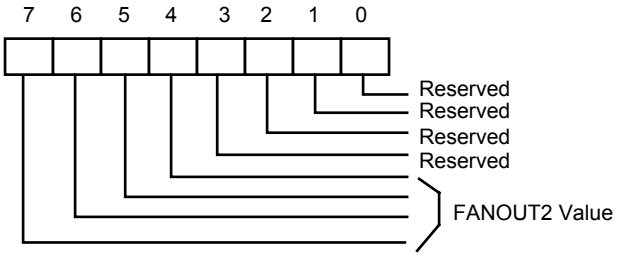
### 5.8.61 FANOUT2 Output Value Control Register-- 03h (*Bank 0*)

Register Location: 03h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits




Bit 7-4: FANPOUT2 voltage control.

$$\textbf{OUTPUT Voltage} = AVCC * \frac{FANOUT}{16}$$

Note: See the Table 3-4

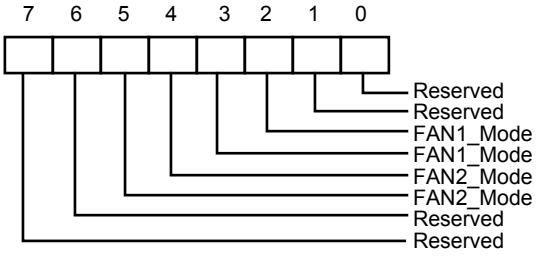
### 5.8.62 FAN Configuration Register I -- Index 04h (*Bank 0*)

Register Location: 04h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit7-6: Reserved

Bit5-4: FANOUT2 mode control.

Set 00, FANOUT2 is as Manual Mode. (Default).

Set 01, FANOUT2 is as Thermal Cruise Mode.

Set 10, FANOUT2 is as Fan Speed Cruise Mode.

Set 11, reserved and no function.

Bit3-2: FANOUT1 mode control.

Set 00, FANOUT1 is as Manual Mode. (Default).

Set 01, FANOUT1 is as Thermal Cruise Mode.

Set 10, FANOUT1 is as Fan Speed Cruise Mode.

Set 11, reserved and no function.

Bit 1-0:Reserved.

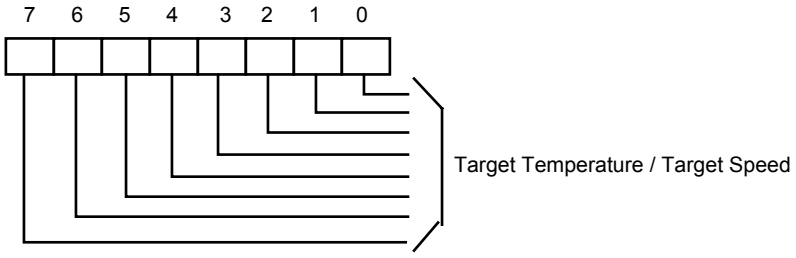
### 5.8.63 SYSTIN Target Temperature Register/ Fan 1 Target Speed Register -- Index 05h (*Bank 0*)

Register Location: 05h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




(1).When at Thermal Cruise mode:

Bit7: Reserved.

Bit6-0: SYSTIN Target Temperature.

(2).When at Fan Speed Cruise mode:

Bit7-0: Fan 1 Target Speed.

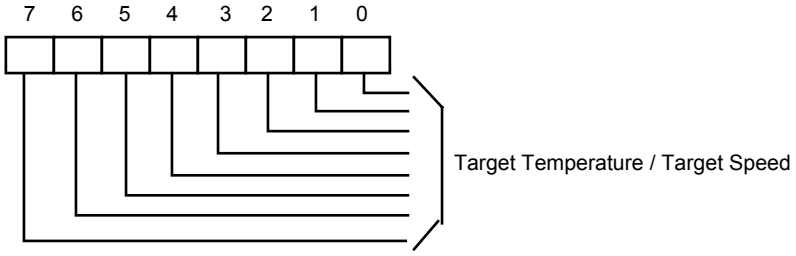
### 5.8.64 CPUTIN Target Temperature Register/ Fan 2 Target Speed Register -- Index 06h (*Bank 0*)

Register Location: 06h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




(1).When at Thermal Cruise mode:

Bit7: Reserved.

Bit6-0: CPUTIN Target Temperature.

(2).When at Fan Speed Cruise mode:

Bit7-0: Fan 2 Target Speed.

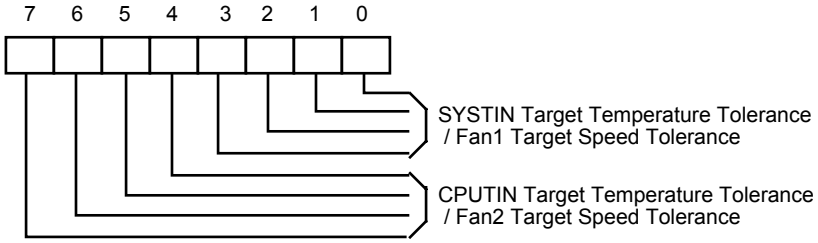
### 5.8.65 Tolerance of Target Temperature or Target Speed Register -- Index 07h (*Bank 0*)

Register Location: 07h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




(1).When at Thermal Cruise mode:

Bit7-4: Tolerance of CPUTIN Target Temperature.

Bit3-0: Tolerance of SYSTIN Target Temperature.

(2).When at Fan Speed Cruise mode:

Bit7-4: Tolerance of Fan 2 Target Speed.

Bit3-0: Tolerance of Fan 1 Target Speed.

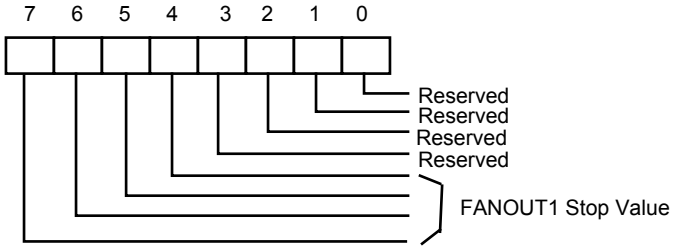
### 5.8.66 FANOUT1 Stop Value Register -- Index 08h (*Bank 0*)

Register Location: 08h

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, FANOUT1 voltage will decrease to this register value. This register should be written a non-zero minimum output value.

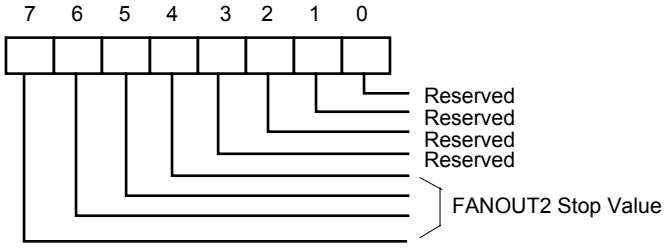
### 5.8.67 FANOUT2 Stop Value Register -- 09h (*Bank 0*)

Register Location: 09h

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, FANOUT2 voltage will decrease to this register value. This register should be written a non-zero minimum output value.

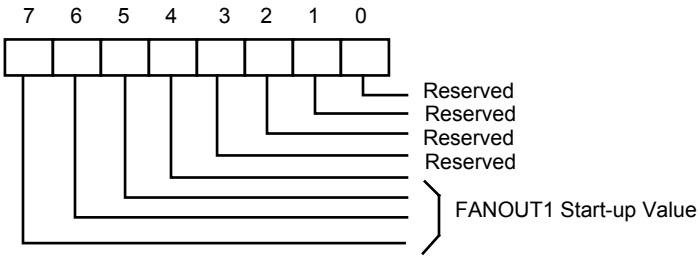
### 5.8.68 FANOUT1 Start-up Value Register -- Index 0Ah (*Bank 0*)

Register Location: 0Ah

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, FANOUT1 voltage will increase from 0 to this register value to provide a minimum value to turn on the fan.

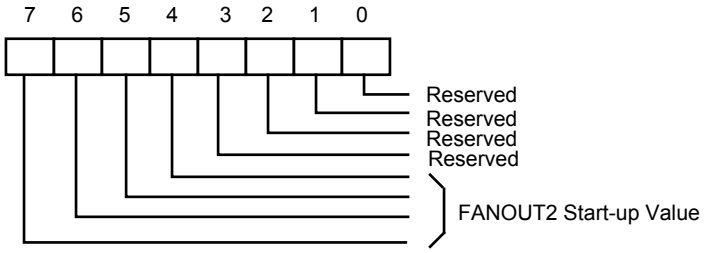
### 5.8.69 FANOUT2 Start-up Value Register -- Index 0Bh (*Bank 0*)

Register Location: 0Bh

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, FANOUT2 voltage will increase from 0 to this register value to provide a minimum value to turn on the fan.

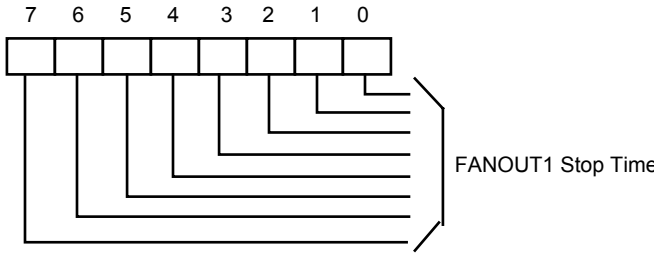
### 5.8.70 FANOUT1 Stop Time Register -- Index 0Ch (*Bank 0*)

Register Location: 0Ch

Power on Default Value 3Ch

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, this register determines the time of which FANOUT1 voltage is from stop value to 0. The unit of this register is 0.1 second. The default time is 6 seconds.

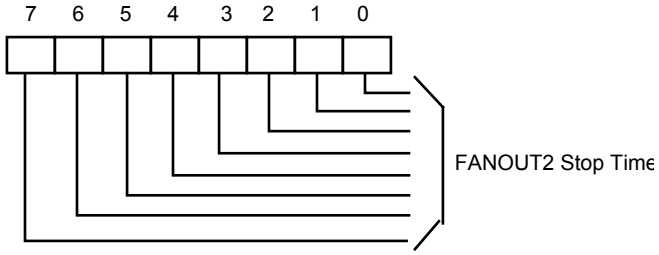
### 5.8.71 FANOUT2 Stop Time Register -- Index 0Dh (*Bank 0*)

Register Location: 0Dh

Power on Default Value 3Ch

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, this register determines the time of which FANOUT2 voltage is from stop value to 0. The unit of this register is 0.1 second. The default time is 6 seconds.

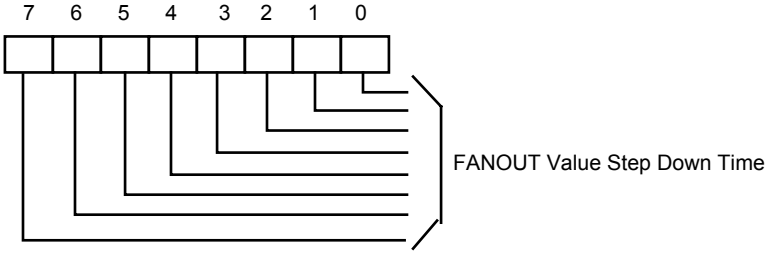
### 5.8.72 Fan Output Step Down Time Register -- Index 0Eh (*Bank 0*)

Register Location: 0Eh

Power on Default Value 0Ah

Attribute: Read/Write

Size: 8 bits




This register determines the speed of FANOUT decreasing the voltage in Smart Fan Control mode. The Unit is 1.6 second.

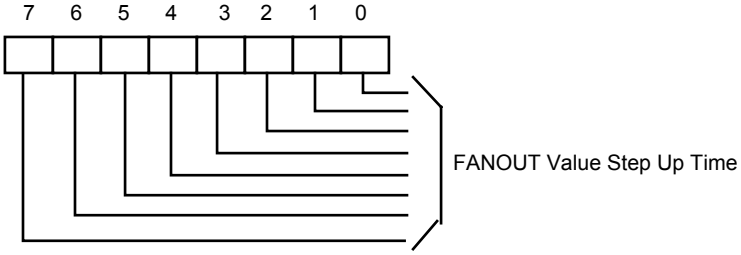
### 5.8.73 Fan Output Step Up Time Register -- Index 0Fh (*Bank 0*)

Register Location: 0Fh

Power on Default Value 0Ah

Attribute: Read/Write

Size: 8 bits




This register determines the speed of FANOUT increasing the voltage in Smart Fan Control mode. The Unit is 1.6 second

### 5.8.74 Reserved Register—Index10h (*Bank 0*)

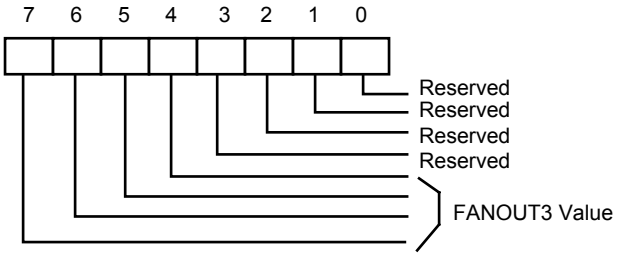
### 5.8.75 FANOUT3 Output Value Control Register-- 11h (*Bank 0*)

Register Location: 11h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits




Bit 7-4: FANPOUT3 voltage control.

$$\textbf{OUTPUT Voltage} = AVCC * \frac{FANOUT}{16}$$

Note: See the Table 3-4

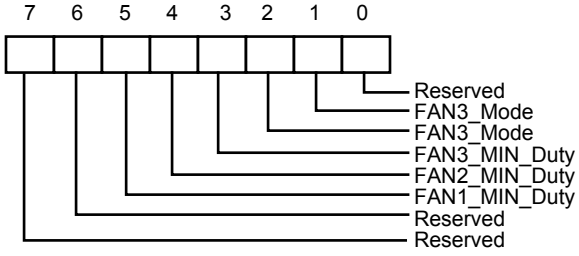
### 5.8.76 FAN Configuration Register II -- Index 12h (*Bank 0*)

Register Location: 12h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




Bit7-6: Reserved

Bit 5: Set 1, FANOUT1 voltage will decrease to and keep the value set in Index 08h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANOUT1 duty cycle will decrease to 0 when temperature goes below target range.

Bit 4: Set 1, FANOUT2 duty cycle will decrease to and keep the value set in Index 09h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANOUT2 duty cycle will decrease to 0 when temperature goes below target range.

Bit 3: Set 1, FANOUT3 duty cycle will decrease to and keep the value set in Index 15h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANOUT3 duty cycle will decrease to 0 when temperature goes below target range.

Bit2-1: FANOUT3 mode control.

Set 00, FANOUT3 is as Manual Mode. (Default).

Set 01, FANOUT3 is as Thermal Cruise Mode.

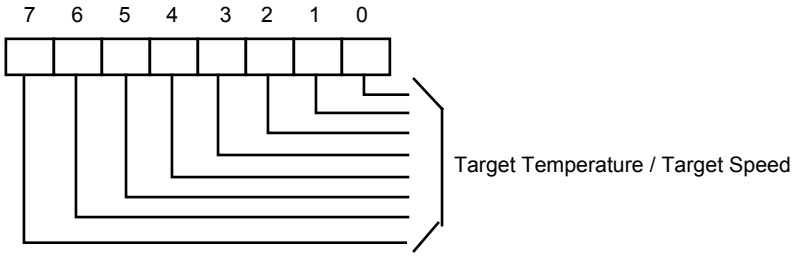
Set 10, FANOUT3 is as Fan Speed Cruise Mode.

Set 11, reserved and no function.

Bit 0:Reserved.

### 5.8.77 VTIN Target Temperature Register/ Fan 3 Target Speed Register -- Index 13h (*Bank 0*)

| | |
|---|---|
| Register Location: | 13h |
| Power on Default Value | 00h |
| Attribute: | Read/Write |
| Size: | 8 bits |




(1).When at Thermal Cruise mode:

Bit7: Reserved.

Bit6-0: VTIN Target Temperature.

(2).When at Fan Speed Cruise mode:

Bit7-0: Fan 3 Target Speed.

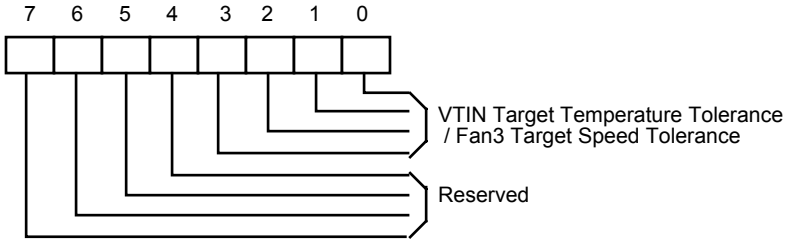
### 5.8.78 Tolerance of Target Temperature or Target Speed Register -- Index 14h (*Bank 0*)

Register Location: 14h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits




(1).When at Thermal Cruise mode:

Bit3-0: Tolerance of VTIN Target Temperature.

(2).When at Fan Speed Cruise mode:

Bit3-0: Tolerance of Fan 3 Target Speed.

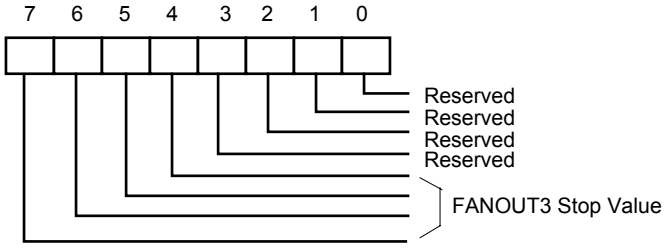
### 5.8.79 FANOUT3 Stop Value Register -- Index 15h (*Bank 0*)

Register Location: 15h

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, FANOUT3 value will decrease to register value. This register should be written a non-zero minimum output value.

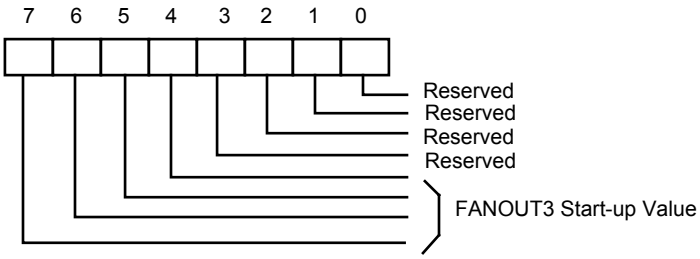
### 5.8.80 FANOUT3 Start-up Value Register -- Index 16h (*Bank 0*)

Register Location: 16h

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, FANOUT3 value will increase from 0 to this register value to provide a minimum voltage to turn on the fan.

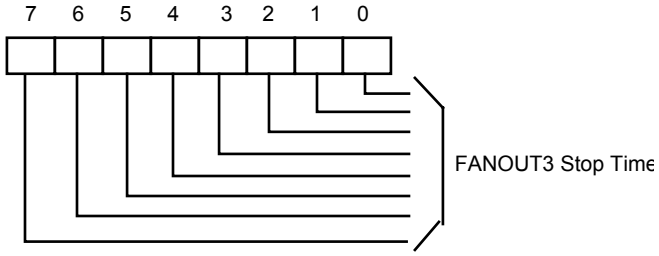
### 5.8.81 FANOUT3 Stop Time Register -- Index 17h (*Bank 0*)

Register Location: 17h

Power on Default Value 3Ch

Attribute: Read/Write

Size: 8 bits




When at Thermal Cruise mode, this register determines the time of which FANOUT3 voltage is from stop value to 0. The unit of this register is 0.1 second. The default time is 6 seconds.

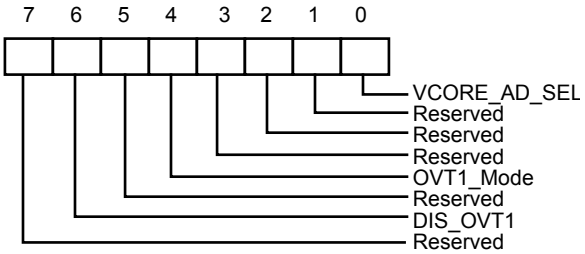
### 5.8.82 VRM & OVT Configuration Register -- Index 18h (*Bank 0*)

Register Location: 18h

Power on Default Value 43h

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved.

Bit 6: Set to 1, disable temperature sensor SYSTIN over-temperature (OVT) output. Set to 0, enable the SYSTIN OVT output.

Bit 5: Reserved.

Bit 4: SYSTIN OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 3-1: Reserved.

Bit 0: CPUVCORE pin voltage detection method selection. Set to 1, VRM9 formula is selected. Set to 0, VRM8 formula is selected. This bit default value is 1.

### 5.8.83 Reserved -- Index 19h (*Bank 0*)

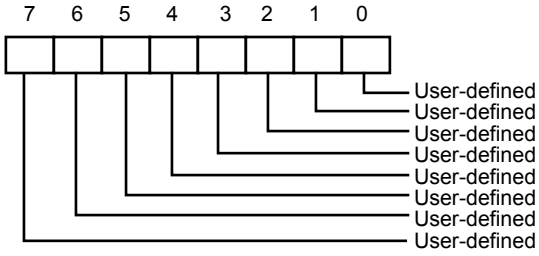
### 5.8.84 User Defined Register -- Index 1A- 1Bh (*Bank 0*)

Register Location: 1A-1Bh

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits

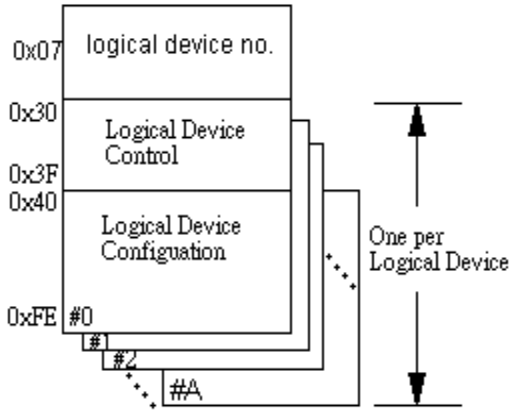



Bit 7-0: User can write any value into these bits and read.

### 5.8.85 Reserved Register-- Index 1Ch-1Fh (*Bank 0*)

# 6. PLUG AND PLAY CONFIGURATION

The W83627THF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83627THF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), KBC (logical device 5), GPIO1,5 (logical device 7), GPIO2 (logical device 8), GPIO3,4 (logical device 9), ACPI ((logical device A), and hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.




## 6.1 Compatible PnP

### 6.1.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

| HEFRAS | address and value |
|---|---|
| 0 | write 87h to the location 2Eh twice |
| 1 | write 87h to the location 4Eh twice |

After Power-on reset, the value on RTSA# (pin 43) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh). After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration

registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

### 6.1.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83627THF enters the default operating mode. Before the W83627THF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

### 6.1.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh (as described in section 12.2.1) on PC/AT systems, the EFDRs are read/write registers with port address 2Fh or 4Fh (as described in section 9.2.1) on PC/AT systems.

## 6.2 Configuration Sequence

To program W83627THF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

### 6.2.1 Enter the extended function mode

To place the chip into the extended function mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers(EFERs, i.e. 2Eh or 4Eh).

### 6.2.2 Configuration the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register(EFIR) and Extended Function Data Register(EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip(Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

### 6.2.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

### 6.2.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;--------------------------------------------------------------------------------
; Enter the extended function mode ,interruptible double-write       |
;--------------------------------------------------------------------------------
MOV     DX,2EH
MOV     AL,87H
OUT     DX,AL
OUT     DX,AL
;--------------------------------------------------------------------------
; Configuration logical device 1, configuration register CRF0     |
;--------------------------------------------------------------------------
MOV     DX,2EH
MOV     AL,07H
OUT     DX,AL           ; point to Logical Device Number Reg.
MOV     DX,2FH
MOV     AL,01H
OUT     DX,AL           ; select logical device 1
;
MOV     DX,2EH
MOV     AL,F0H
OUT     DX,AL           ; select CRF0
MOV     DX,2FH
MOV     AL,3CH
OUT     DX,AL           ; update CRF0 with value 3CH
;----------------------------------------
; Exit extended function mode     |
;----------------------------------------
MOV     DX,2EH
MOV     AL,AAH
OUT     DX,AL
```

# 7. CONFIGURATION REGISTER

## 7.1 Chip (Global) Control Register

**CR02 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 : SWRST --> Soft Reset.

**CR07**

Bit 7 - 0 : LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

**CR20**

Bit 7 - 0 : DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x82(read only).

CR21

Bit 7 - 0 : DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x83
(read only, 1 is version no.).

CR22 (Default 0xff)

Bit 7 : RESERVED.

Bit 6 : HMPWD

= 0 Power down

= 1 No Power down

Bit 5 : URBPWD

= 0 Power down

= 1 No Power down

Bit 4 : URAPWD

= 0 Power down

= 1 No Power down

Bit 3 : PRTPWD

= 0 Power down

= 1 No Power down

Bit 2 - 1 : Reserved.

Bit 0 : FDCPWD

= 0 Power down

= 1 No Power down

**CR23 (Default 0x00)**

Bit 7 - 1 : RESERVED.

Bit 0 : IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

**CR24 (Default 0s110s1sb)**

Bit 7 : Reserved

Bit 6 : CLKSEL

= 0 The clock input on Pin 18 should be 24 Mhz.

= 1 The clock input on Pin 18 should be 48 Mhz.

The corresponding power-on setting pin is SOUTB (pin 83).

Bit 5 - 3 : Reserved

Bit 2 : ENKBC

= 0 KBC is disabled after hardware reset.

= 1 KBC is enabled after hardware reset.

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is SOUTA (pin 54).

Bit 1 : Reserved. Must be 1.

Bit 0 : PNPCSV

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

When trying to make a change to this bit, new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCSV to 0 first and then reset it to 1 to reset these PnP registers if the present value of PNPCSV is 1. The corresponding power-on setting pin is NDTRA (pin 52).

**CR25 (Default 0x00)**

Bit 7 - 6 : Reserved

Bit 5 : URBTRI

Bit 4 : URATRI

Bit 3 : PRTTRI

Bit 2 - 1 : Reserved

Bit 0 : FDCTRI.

**CR26 (Default 0s000000b)**

Bit 7 : SEL4FDD

= 0 Select two FDD mode.

= 1 Select four FDD mode.

Bit 6 : HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is NRTSA (pin 51).

HEFRAS Address and Value

= 0 Write 87h to the location 2Eh twice.

= 1 Write 87h to the location 4Eh twice.

Bit 5 : LOCKREG

= 0 Enable R/W Configuration Registers

= 1 Disable R/W Configuration Registers.

Bit 4 : Reserved

Bit 3 : DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2 : DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on electing IRQ.

Bit 1 : DSUALGRQ

= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ.

= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ.

Bit 0 : DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

**CR28 (Default 0x00)**

Bit 7 - 3 : Reserved.

Bit 2 - 0 : PRTMODS2 - PRTMODS0

= 0xx Parallel Port Mode

= 100 Reserved

= 101 External FDC Mode

= 110 Reserved

= 111 External two FDC Mode

**CR29 (GPIO Group 1 multiplexed pin selection register 1. VCC powered. Default 0x00)**

Bit 7, 6 Port Select (select pin 121 ~ 128 as Game Port, General Purpose I/O Port 1 decoding feature.

= 00 Game Port.

= 01 General Purpose I/O Port 1.

= 10 Reserved.

= 11 Reserved.

Bit 5 PIN105S.

= 0 GP55

= 1 Winbond Test Mode

Bit 4 XUR_SEL. It selects the function of pin 78 ~ 85.

= 0 Pin 78 ~ 85 serve as URB function.

= 1 Winbond Test Mode

Bit 3 - 2 Reserved.

Bit 1, 0 PIN120S1, PIN120S0

= 00 MSO (MIDI Serial Output).

= 01 GP20

= 10 Reserved

= 11 IRQIN0 (select IRQ resource through CRF4 Bit 7-4 of Logical Device 8).

**CR2A (GPIO2 multiplexed pin selection register. VCC powered. Default 0x00)**

Bit 7, 6 PIN119S1, PIN119S0.

= 00 MSI.

= 01 GP21.

= 10 Winbond Test Mode

= 11 Reserved.

Bit 5 PIN118S.
= 0 GP22.
= 1 Winbond Test Mode
Bit 4 PIN96S.
= 0 GP23.
= 1 Winbond Test Mode.
Bit 3 PIN95S.
= 0 GP24.
= 1 Winbond Test Mode
Bit 2 PIN94S.
= 0 GP25.
= 1 Winbond Test Mode.
Bit 1 PIN93S.
= 0 GP26.
= 1 Winbond Test Mode
Bit 0 PIN2S
= 0 SMI#.
= 1 IRQIN1 (select IRQ resource through CRF4 Bit 7-4 of Logical Device8).

**CR2B (GPIO3 multiplexed pin selection register 3. VSB powered. Default 0x00ssssssb)**

Bit 7 Reserved
Bit 6 PIN86S.
= 0 GP35.
= 1 Winbond Test Mode
Bit 5, 4 PIN88S1, PIN88S0.
= 00 IRRX.
= 01 GP34.
= 10 Winbond Test Mode
= 11 Reserved
Bit 3, 2 PIN89S1, PIN89S0.
= 00 GP33.
= 01 WDTO.
= 10 Reserved
= 11 Reserved

Bit 1, 0 PIN90S1, PIN90S0.
= 00 GP32.
= 01 PLED.
= 10 Reserved.
= 11 Reserved.

**CR2C (GPIO3 multiplexed pin selection register 2. VSB powered. Default 0xssssss00b)**

Bit 7, 6 : PIN91S1, PIN91S0.
= 00 GP31.
= 01 Reserved.
= 10 Reserved.
= 11 Reserved

Bit 5, 4 : PIN92S1, PIN92S0.
= 00 GP30.
= 01 Reserved.
= 10 Reserved.
= 11 Reserved

Bit 3, 2 : PIN64S1, PIN64S0.
= 00 SUSLED.
= 01 GP37.
= 10 Reserved.
= 11 Reserved.

Bit 1 : PIN87S.
= 0 IRTX.
= 1 Winbond Test Mode.

Bit 0 : Reserved.

**CR2D (GPIO4 multiplexed pin selection register. VSB powered. Default 0x00s00000b)**

Bit 7 : PIN67S.
= 0 PSOUT#.
= 1 GP47.

Bit 6 : PIN68S.
= 0 PSIN.
= 1 GP46.

Bit 5 : PIN69S.
= 0 GP45.
= 1 Reserved.
Bit 4 : PIN70S.
= 0 RSMRST#.
= 1 GP44.
Bit 3 : PIN71S.
= 0 PWROK.
= 1 GP43.
Bit 2 : PIN72S.
= 0 PWRCTL#.
= 1 GP42.
Bit 1 : PIN73S.
= 0 SLP_SX#.
= 1 GP41.
Bit 0 : PIN75S.
= 0 GP40
= 1 Winbond Test Mode

**CR2E (Default 0x00)**

Test Modes: Reserved for Winbond.

**CR2F (Default 0x00)**

Test Modes: Reserved for Winbond.

### 7.1.1 Logical Device 0 (FDC)

**CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resource for FDC.

**CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)**

Bit 7 - 3 : Reserved.

Bit 2 - 0 : These bits select DRQ resource for FDC.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04 - 0x07 No DMA active

**CRF0 (Default 0x0E)**

**FDD Mode Register**

Bit 7 : FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

= 0 The internal pull-up resistors of FDC are turned on.(Default)

= 1 The internal pull-up resistors of FDC are turned off.

Bit 6 : INTVERTZ

This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.

= 1 FDD interface signals are active high.

Bit 5 : DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4 : Swap Drive 0, 1 Mode

= 0 No Swap (Default)

= 1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 :Interface Mode

= 11 AT Mode (Default)

= 10 (Reserved)

= 01 PS/2

= 00 Model 30

Bit 1 : FDC DMA Mode
= 0 Burst Mode is enabled
= 1 Non-Burst Mode (Default)
Bit 0 : Floppy Mode
= 0 Normal Floppy Mode (Default)
= 1 Enhanced 3-mode FDD

**CRF1 (Default 0x00)**

Bit 7 - 6 : Boot Floppy
= 00 FDD A
= 01 FDD B
= 10 FDD C
= 11 FDD D
Bit 5, 4 : Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
Bit 3 - 2 : Density Select
= 00 Normal (Default)
= 01 Normal
= 10 1 (Forced to logic 1)
= 11 0 (Forced to logic 0)
Bit 1 : DISFDDWR
= 0 Enable FDD write.
= 1 Disable FDD write(forces pins WE, WD stay high).
Bit 0 : SWWP
= 0 Normal, use WP to determine whether the FDD is write protected or not.
= 1 FDD is always write-protected.

**CRF2 (Default 0xFF)**

Bit 7 - 6 : FDD D Drive Type
Bit 5 - 4 : FDD C Drive Type
Bit 3 - 2 : FDD B Drive Type
Bit 1 - 0 : FDD A Drive Type

**CRF4 (Default 0x00)**

**FDD0 Selection:**

Bit 7 : Reserved.

Bit 6 : Pre-comp. Disable.

= 1 Disable FDC Pre-compensation.

= 0 Enable FDC Pre-compensation.

Bit 5 : Reserved.

Bit 4 - 3 : DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format

= 01 3-mode drive

= 10 2 Meg Tape

= 11 Reserved

Bit 2 : Reserved.

Bit 1:0 : DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

**CRF5 (Default 0x00)**

FDD1 Selection: Same as FDD0 of CRF4.

**TABLE A**

| DRIVE RATE TABLE SELECT | | DATA RATE | | SELECTED DATA RATE | | SELDEN |
|---|---|---|---|---|---|---|
| DRTS1 | DRTS0 | DRATE1 | DRATE0 | MFM | FM | |
| 0 | 0 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 300K | 150K | 0 |
| | | 1 | 0 | 250K | 125K | 0 |
| 0 | 1 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 500K | 250K | 0 |
| | | 1 | 0 | 250K | 125K | 0 |
| 1 | 0 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 2Meg | --- | 0 |
| | | 1 | 0 | 250K | 125K | 0 |

TABLE B

| DTYPE0 | DTYPE1 | DRVDEN0(pin 2) | DRVDEN1(pin 3) | DRIVE TYPE |
|---|---|---|---|---|
| 0 | 0 | SELDEN | DRATE0 | 4/2/1 MB 3.5”“<br>2/1 MB 5.25”<br>2/1.6/1 MB 3.5” (3-MODE) |
| 0 | 1 | DRATE1 | DRATE0 | |
| 1 | 0 | $\overline{\text{SELDEN}}$ | DRATE0 | |
| 1 | 1 | DRATE0 | DRATE1 | |

### 7.1.2 Logical Device 1 (Parallel Port)

**CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (All modes supported, EPP is only available when the base address is on 8 byte boundary).

**CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit [3:0] : These bits select IRQ resource for Parallel Port.

**CR74 (Default 0x04)**

Bit 7 - 3 : Reserved.

Bit 2 - 0 : These bits select DRQ resource for Parallel Port.

0x00 = DMA0

0x01 = DMA1

0x02 = DMA2

0x03 = DMA3

0x04 - 0x07 = No DMA active

**CRF0 (Default 0x3F)**

Bit 7 : Reserved.

Bit 6 - 3 : ECP FIFO Threshold.

Bit 2 - 0 : Parallel Port Mode (CR28 PRTMODS2 = 0)

= 100 Printer Mode (Default)

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP - 1.9 and SPP mode

= 101 EPP - 1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP - 1.9 mode

= 111 ECP and EPP - 1.7 mode.

### 7.1.3 Logical Device 2 (UART A)

**CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resource for Serial Port 1.

**CRF0 (Default 0x00)**

Bit 7 - 2 : Reserved.

Bit 1 - 0 : SUACLKB1, SUACLKB0

= 00 UART A clock source is 1.8462 Mhz (24MHz/13)

= 01 UART A clock source is 2 Mhz (24MHz/12)

= 10 UART A clock source is 24 Mhz (24MHz/1)

= 11 UART A clock source is 14.769 Mhz (24mhz/1.625)

### 7.1.4 Logical Device 3 (UART B)

**CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit [3:0] : These bits select IRQ resource for Serial Port 2.

**CRF0 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 : RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters - time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2 : TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0 : SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 Mhz (24MHz/13)

= 01 UART B clock source is 2 Mhz (24MHz/12)

= 10 UART B clock source is 24 Mhz (24MHz/1)

= 11 UART B clock source is 14.769 Mhz (24mhz/1.625)

**CRF1 (Default 0x00)**

Bit 7 : Reserved.

Bit 6 : IRLOCSEL. IR I/O pins' location select.

= 0 Through SINB/SOUTB.

= 1 Through IRRX/IRTX.

Bit 5 : IRMODE2. IR function mode selection bit 2.

Bit 4 : IRMODE1. IR function mode selection bit 1.

Bit 3 : IRMODE0. IR function mode selection bit 0.

| IR MODE | IR FUNCTION | IRTX | IRRX |
|---|---|---|---|
| 00X | Disable | tri-state | high |
| 010* | IrDA | Active pulse 1.6 μS | Demodulation into SINB/IRRX |
| 011* | IrDA | Active pulse 3/16 bit time | Demodulation into SINB/IRRX |
| 100 | ASK-IR | Inverting IRTX/SOUTB pin | routed to SINB/IRRX |
| 101 | ASK-IR | Inverting IRTX/SOUTB & 500 KHZ clock | routed to SINB/IRRX |
| 110 | ASK-IR | Inverting IRTX/SOUTB | Demodulation into SINB/IRRX |
| 111* | ASK-IR | Inverting IRTX/SOUTB & 500 KHZ clock | Demodulation into SINB/IRRX |

Note: The notation is normal mode in the IR function.

Bit 2 : HDUPLX. IR half/full duplex function select.

= 0 The IR function is Full Duplex.

= 1 The IR function is Half Duplex.

Bit 1 : TX2INV

= 0 The SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

= 1 Inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0 : RX2INV.

= 0 The SINB pin of UART B function or IRRX pin of IR function in normal condition.

= 1 Inverse the SINB pin of UART B function or IRRX pin of IR function

### 7.1.5 Logical Device 5 (KBC)

**CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x00, 0x60 if PNPCSV = 0 during POR, default 0x00 otherwise)**

These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

**CR62, CR 63 (Default 0x00, 0x64 if PNPCSV = 0 during POR, default 0x00 otherwise)**

These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

**CR70 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit [3:0] : These bits select IRQ resource for KINT (keyboard).

**CR72 (Default 0x0C if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit [3:0] : These bits select IRQ resource for MINT (PS2 Mouse)

**CRF0 (Default 0x80)**

Bit 7 - 6 : KBC clock rate selection

= 00 Select 6MHz as KBC clock input.

= 01 Select 8MHz as KBC clock input.

= 10 Select 12Mhz as KBC clock input.

= 11 Select 16Mhz as KBC clock input.

Bit 5 - 3 : Reserved.

Bit 2 = 0 Port 92 disable.

= 1 Port 92 enable.

Bit 1 = 0 Gate20 software control.

= 1 Gate20 hardware speed up.

Bit 0 = 0 KBRST software control.

= 1 KBRST hardware speed up.

### 7.1.6 Logical Device 7 (Game Port and MIDI Port and GPIO Port 1 and 5)

**CR30 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 = 1 Enable GPIO port 5.

= 0 Disable GPIO port 5.

Bit 2 = 1 Enable MIDI Port.

= 0 MIDI Port is disabled if bit 0 of this register is also 0.

Bit 1 = 1 Enable game Port.

= 0 Game Port is disabled if bit 0 of this register is also 0.

Bit 0 = 1 Enable GPIO port 1, game Port and MIDI Port.

= 0 Disable GPIO port 1. Game Port and MIDI Port are enabled/disabled by bit 1 and 2 of this register respectively.

**CR60, CR 61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)**

These two registers select the Game Port base address [0x100:0xFFF] on 1 byte boundary.

**CR62, CR 63 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)**

These two registers select the MIDI Port base address [0x100:0xFFF] on 2 byte boundary.

**CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)**

Bit 7 - 4 : Reserved.

Bit [3:0] : These bits select IRQ resource for MIDI Port .

**CRF0 (GP1[7:0] I/O selection register. Default 0xFF)**

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

**CRF1 (GP1[7:0] data register. Default 0x00)**

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

**CRF2 (GP1[7:0] inversion register. Default 0x00)**

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

**CRF3 (GP5[5:0] I/O selection register. Default 0xFF)**

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

**CRF4 (GP5[5:0] data register. Default 0x00)**

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

**CRF5 (GP5[5:0] inversion register. Default 0x00)**

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

### 7.1.7 Logical Device 8 (GPIO Port 2 This power of the Port is VCC source)

**CR30 (GP2[7:0] Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activate GPIO2.

= 0 GPIO2 is inactive.

**CRF0 (GP2[7:0] I/O selection register. Default 0xFF)**

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

**CRF1 (GP2[7:0] data register. Default 0x00)**

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

**CRF2 (GP2[7:0] inversion register. Default 0x00)**

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

**CRF3 (Default 0x00)**

Bit 7 - 4 : These bits select IRQ resource for IRQIN1.

Bit 3 - 0 : These bits select IRQ resource for IRQIN0.

**CRF4 (Reserved)**

**CRF5 (PLED mode register. Default 0x00)**

Bit 7-6 : Select PLED mode
= 00 Power LED pin is tri-stated.
= 01 Power LED pin is driven low.
= 10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle
= 11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

Bit 5-4 : Reserved

Bit 3 : Select WDTO counter type.
= 0 By second
= 1 By minute

Bit 2 : Enable the rising edge of keyboard Reset (P20) to force Time-out event.
= 0 Disable
= 1 Enable

Bit 1-0 : Reserved

**CRF6 (Default 0x00)**

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. If the Bit 7 and Bit 6 are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit 7 - 0 = 0x00 Time-out Disable
= 0x01 Time-out occurs after 1 second/minute
= 0x02 Time-out occurs after 2 second/minutes
= 0x03 Time-out occurs after 3 second/minutes
.....
= 0xFF Time-out occurs after 255 second/minutes

**CRF7 (Default 0x00)**

Bit 7 : Mouse interrupt reset Enable or Disable
= 1 Watch Dog Timer is reset upon a Mouse interrupt
= 0 Watch Dog Timer is not affected by Mouse interrupt

Bit 6 : Keyboard interrupt reset Enable or Disable
= 1 Watch Dog Timer is reset upon a Keyboard interrupt
= 0 Watch Dog Timer is not affected by Keyboard interrupt

Bit 5 : Force Watch Dog Timer Time-out, Write only*
= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4 : Watch Dog Timer Status, R/W
= 1 Watch Dog Timer time-out occurred
= 0 Watch Dog Timer counting

Bit 3 -0 : These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

### 7.1.8 Logical Device 9 (GPIO Port 3, 4. These two ports are powered by VSB)

**CR30 (Default 0x00)**

Bit 7 - 2 : Reserved

Bit 1 = 1 Activate GPIO4.
= 0 GPIO4 is inactive.

Bit 0 = 1 Activate GPIO3.
= 0 GPIO3 is inactive.

**CRF0 (GP3[7:0] I/O selection register. Default 0xFF)**

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

**CRF1 (GP3[7:0] data register. Default 0x00)**

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

**CRF2 (GP3[7:0] inversion register. Default 0x00)**

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

**CRF3 (SUSLED mode register. Default 0x00)**

Bit 7-6 : Select Suspend LED mode

= 00 Suspend LED pin is drove low.

= 01 Suspend LED pin is tri-stated.

= 10 Suspend LED pin is a 1Hz toggle pulse with 50 duty cycle.

= 11 Suspend LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

This mode selection bit 7-6 keep its settings until VSB power loss.

Bit 5 - 0 : Reserved.

**CRF4 (GP4[7:0] I/O selection register. Default 0xFF)**

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

**CRF5 (GP4[7:0] data register. Default 0x00)**

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

**CRF6 (GP4[7:0] inversion register. Default 0x00)**

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

## 7.2 Logical Device A (ACPI)

(The CR30,70,F0~F9 are VCC power source; CR E0~E7 are VRTC power source)

**CR30 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR70 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resources for $\overline{\text{PME}}$.

**CRE0 (Default 0x00)**

Bit 7 : DIS-PANSW_IN. Disable panel switch input to turn system power supply on.

= 0 PANSW_IN is wire-ANDed and connected to PANSW_OUT.

= 1 PANSW_IN is blocked and can not affect PANSW_OUT.

Bit 6 : ENKBWAKEUP. Enable Keyboard to wake-up system via PANSW_OUT.

= 0 Disable Keyboard wake-up function.

= 1 Enable Keyboard wake-up function.

Bit 5 : ENMSWAKEUP. Enable Mouse to wake-up system via PANSW_OUT.

= 0 Disable Mouse wake-up function.

= 1 Enable Mouse wake-up function.

Bit 4 : MSRKEY.

This bit combining with MSXKEY (bit 1 of CRE0 of logical device A) and ENMDAT_UP (bit 7 of CRE6 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

| ENMDAT_UP | MSRKEY | MSXKEY | WAKE UP EVENT |
|---|---|---|---|
| 1 | x | 1 | Any button click or any movement |
| 1 | x | 0 | one click of left/right button |
| 0 | 0 | 1 | one click of left button |
| 0 | 1 | 1 | one click of right button |
| 0 | 0 | 0 | two times click of left button |
| 0 | 1 | 0 | two times click of right button |

Bit 3 Reserved

Bit 2 : KB/MS Swap. Enable Keyboard/Mouse port-swap.

= 0 Keyboard/Mouse ports are not swapped.

= 1 Keyboard/Mouse ports are swapped.

Bit 1 : MSXKEY.

This bit combining with MSRKEY (bit 4 of CRE0 of logical device A) and ENMDAT_UP (bit 7 of CRE6 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

| ENMDAT_UP | MSRKEY | MSXKEY | WAKE UP EVENT |
|---|---|---|---|
| 1 | x | 1 | Any button click or any movement |
| 1 | x | 0 | one click of left/right button |
| 0 | 0 | 1 | one click of left button |
| 0 | 1 | 1 | one click of right button |
| 0 | 0 | 0 | two times click of left button |
| 0 | 1 | 0 | two times click of right button |

Bit 0 : KBXKEY. Enable any character received from Keyboard to wake-up the system

= 0 Only predetermined specific key combination can wake up the system.

= 1 Any character received from Keyboard can wake up the system.

**CRE1 (Default 0x00) Keyboard Wake-Up Index Register**

This register is used to indicate which Keyboard Wake-Up Shift register or Predetermined key Register is to be read/written via CRE2. The first set of wake up key combination is in the range of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combination can be read through 0x10 – 0x1E.

**CRE2 Keyboard Wake-Up Data Register**

This register holds the value of wake-up key register indicated by CRE1. This register can be read/written.

**CRE3 (Read only) Keyboard/Mouse Wake-Up Status Register**

Bit 7-5 : Reserved.

Bit 4 : PWRLOSS_STS: This bit is set when power loss occurs.

Bit 3 Reserved

Bit 2 : PANSW_STS. The Panel switch event is caused by PANSW_IN. This bit is cleared by reading this register.

Bit 1 : Mouse_STS. The Panel switch event is caused by Mouse wake-up event. This bit is cleared by reading this register.

Bit 0 : Keyboard_STS. The Panel switch event is caused by Keyboard wake-up event. This bit is cleared by reading this register.

**CRE4 (Default 0x00)**

Bit 7 : Power loss control bit 2.

= 0 Disable ACPI resume

= 1 Enable ACPI resume

Bit 6-5 : Power loss control bit <1:0>

= 00 System always turn off when come back from power loss state.

= 01 System always turn on when come back from power loss state.

= 10 System turn on/off when come back from power loss state depend on the state before power loss.

= 11 Reserved.

Bit 4 : Reserved

Bit 3 : Keyboard wake-up type select for wake-up the system from S1/S2.

= 0 LA.CRE0.bit0 determines how system wake up from S1/S2.

= 1 Any key.

Bit 2 : Enable all wake-up event set in CRE0 can wake-up the system from S1/S2 state. This bit is cleared when wake-up event occurs.

= 0 Disable.

= 1 Enable.

Bit 1 - 0 : Reserved. Must be 00b.

**CRE5 (Default 0x00)**

Bit 7 : Reserved.

Bit 6 - 0 : Compared Code Length. When the compared codes are storied in the data register, these data length should be written to this register.

**CRE6 (Default 0x00)**

Bit 7 ENMDAT_UP. This bit combining with MSRKEY (bit 4 of CRE0 of logical device A) and MSXKEY (bit 1 of CRE0 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

| ENMDAT_UP | MSRKEY | MSXKEY | WAKE UP EVENT |
|---|---|---|---|
| 1 | x | 1 | Any button click or any movement |
| 1 | x | 0 | one click of left/right button |
| 0 | 0 | 1 | one click of left button |
| 0 | 1 | 1 | one click of right button |
| 0 | 0 | 0 | two times click of left button |
| 0 | 1 | 0 | two times click of right button |

Bit6 Chassis Status Clear

= 1 Clear CASEOPEN# (Pin76) event.

= 0 Disable Clear Function.

Bit 5 - 0 Reserved

**CRE7 (Default 0x00)**

Bit 7 ENKD3. Enable the third set of keyboard wake-up key combinations. Its values are accessed through keyboard wake-up index register (CRE1 of logical device A) and keyboard wake-up data register (CRE2 of logical device A) at index from 40h to 4eh.

= 0 disable wake-up function of the third set of key combinations.

= 1 enable wake-up function of the third set of key combinations.

Bit 6 ENKD2. Enable the second set of keyboard wake-up key combinations. Its values are accessed through keyboard wake-up index register (CRE1 of logical device A) and keyboard wake-up data register (CRE2 of logical device A) at index from 30h to 3eh.

= 0 disable wake-up function of the second set of key combinations.

= 1 enable wake-up function of the second set of key combinations.

Bit 5 ENWIN98KEY. Enable WIN98 keyboard dedicated key to wake up system through PANSW_OUT if keyboard wake up function is enabled.

= 0 Disable WIN98 keyboard wake up.

= 1 Enable WIN98 keyboard wake up.

Bit 4 EN_ONPSOUT. Enable to issue a 0.5s long PSOUT# pulse when system returns from power loss state and is supposed to be on as described in CRE4 bit 6, 5 of logical device A.

= 0 Disable this function for Intel's Chipset.

= 1 Enable this function for Clone's chipset.

Bit 3 SELWDTORST: Select whether Watch Dog timer function is reset by LRESET_L signal or PWROK signal.

=0 Watch Dog timer function is reset by LRESET_L signal.

=1 Watch Dog timer function is reset by PWROK signal.

Bit 2 Reserved

Bit 1 Reserved

Bit 0 Reserved

**CRF0 (Default 0x00)**

Bit 7 : CHIPPME. Chip level auto power management enable.
= 0 disable the auto power management functions
= 1 enable the auto power management functions.

Bit 6 Reserved

Bit 5 : MIDIPME. MIDI port auto power management enable.
= 0 disable the auto power management functions
= 1 enable the auto power management functions.

Bit 4 : Reserved. Return zero when read.

Bit 3 : PRTPME. Printer port auto power management enable.
= 0 disable the auto power management functions.
= 1 enable the auto power management functions.

Bit 2 : FDCPME. FDC auto power management enable.
= 0 disable the auto power management functions.
= 1 enable the auto power management functions.

Bit 1 : URAPME. UART A auto power management enable.
= 0 disable the auto power management functions.
= 1 enable the auto power management functions.

Bit 0 : URBPME. UART B auto power management enable.
= 0 disable the auto power management functions.
= 1 enable the auto power management functions.

**CRF1 (Default 0x00)**

Bit 7 : WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

= 0 the chip is in the sleeping state.

= 1 the chip is in the working state.

Bit 6 - 5 : Devices' trap status.

Bit 4 : Reserved. Return zero when read.

Bit 3 - 0 : Devices' trap status.

**CRF3 (Default 0x00)**

Bit 7 - 0 : Device's IRQ status.

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7 : Reserved.

Bit 6 : Reserved.

Bit 5 : MOUIRQSTS. MOUSE IRQ status.

Bit 4 : KBCIRQSTS. KBC IRQ status.

Bit 3 : PRTIRQSTS. printer port IRQ status.

Bit 2 : FDCIRQSTS. FDC IRQ status.

Bit 1 : URAIRQSTS. UART A IRQ status.

Bit 0 : URBIRQSTS. UART B IRQ status.

**CRF4 (Default 0x00)**

Bit 7 : Reserved. Return zero when read.

Bit 6 - 0 : These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a1. Writing a 0 has no effect.

Bit 6 :Reserved

Bit 5 : HMIRQSTS. Hardware monitor IRQ status.

Bit 4 : WDTIRQSTS. Watch dog timer IRQ status.

Bit 3 Reserved

Bit 1 : IRQIN1STS. IRQIN1 status.

Bit 0 : IRQIN0STS. IRQIN0 status.

**CRF6 (Default 0x00)**

Bit 7 - 0 : Enable bits of the $\overline{SMI}$ / $\overline{PME}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to any IRQ of the devices. $\overline{SMI}$ / $\overline{PME}$ logic output = (MOUIRQEN and MOUIRQSTS) or (KBCIRQEN and KBCIRQSTS) or (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS) or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS) or

(HMIRQEN and HMIRQSTS) or (WDTIRQEN and WDTIRQSTS) or

(IRQIN3EN and IRQIN3STS) or (IRQIN2EN and IRQIN2STS) or

(IRQIN1EN and IRQIN1STS) or (IRQIN0EN and IRQIN0STS)

Bit 7 Reserved.

Bit 6 Reserved

Bit 5 : MOUIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MOUSE's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MOUSE's IRQ.

Bit 4 : KBCIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to KBC's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to KBC's IRQ.

Bit 3 : PRTIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to printer port's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to printer port's IRQ.

Bit 2 : FDCIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to FDC's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1 : URAIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART A's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0 : URBIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART B's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART B's IRQ.

**CRF7 (Default 0x00)**

Bit 7 : Reserved. Return zero when read

Bit 6 - 0 : Enable bits of the $\overline{SMI}$ / $\overline{PME}$ generation due to the GPIO IRQ function or device's IRQ.

Bit 6 Reserved

Bit 5 : HMIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to hardware monitor's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to hardware monitor's IRQ.

Bit 4 : WDTIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to watch dog timer's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to watch dog timer's IRQ.

Bit 3 Reserved

Bit 2 : MIDIIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

Bit 1 : IRQIN1EN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN1's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN1's IRQ.

Bit 0 : IRQIN0EN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN0's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN0's IRQ.

**CRF9 (Default 0x00)**

Bit 7 - 3 : Reserved. Return zero when read.

Bit 2 : PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for

the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

= 0 the power management events will generate an $\overline{SMI}$ event

= 1 the power management events will generate an $\overline{PME}$ event.

Bit 1 : FSLEEP: This bit selects the fast expiry time of individual devices.

= 0 1 second.

= 1 8 mS

Bit 0 : SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

= 0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

= 1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

**CRFE, FF (Default 0x00)**

Reserved for Winbond test.

## 7.3 Logical Device B (Hardware Monitor)

**CR30 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x00, 0x00)**

These two registers select Hardware Monitor base address [0x100:0xFFF] on 8-byte boundary.

**CR70 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ channel for Hardware Monitor.

# 8. AC/DC SPECIFICATIONS

## 8.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage (5V) | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to $V_{DD}$+0.5 | V |
| RTC Battery Voltage $V_{BAT}$ | 2.2 to 4.0 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -55 to +150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 8.2 DC CHARACTERISTICS

($T_a$ = 0 °C to 70 °C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V)

| PARAMETER | SYM. | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| RTC Battery Quiescent Current | $I_{BAT}$ | | | 2.4 | uA | $V_{BAT}$ = 2.5 V |
| ACPI Stand-by Power Supply Quiescent current | $I_{BAT}$ | | | 2.0 | mA | $V_{SB}$ = 5.0 V, All ACPI pins are not connected. |
| **$IN_{cs}$ - CMOS level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 1.3 | 1.5 | 1.7 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 3.2 | 3.5 | 3.8 | V | $V_{DD}$ = 5 V |
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD}$ = 5 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_t$ - TTL level input pin** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_{td}$ - TTL level input pin with internal pull down resistor** | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| pull down resistor | R | | | 47 | KΩ | |
| **$IN_{ts}$ - TTL level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.8 | 0.9 | 1.0 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.8 | 1.9 | 2.0 | V | $V_{DD}$ = 5 V |
| Hystersis | $V_{TH}$ | 0.8 | 1.0 | | V | $V_{DD}$ = 5 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_{tsp3}$ - 3.3 V TTL level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD}$ = 3.3 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD}$ = 3.3 V |
| Hystersis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$ = 3.3 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 3.3 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_{tu}$ - TTL level input pin with internal pull up resistor** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| pull up resistor | R | 40 | | | KΩ | |
| **$I/O_{8t}$ - TTL level bi-directional pin with source-sink capability of 8 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 8 mA |

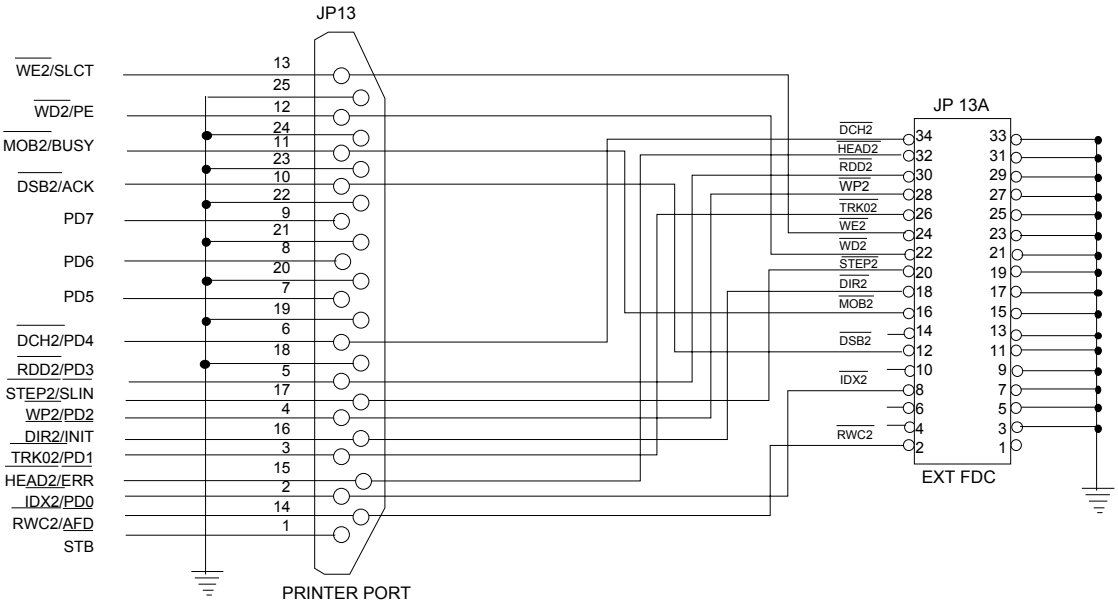
| | | | | | | |
|---|---|---|---|---|---|---|
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/O_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/O_{12tp3}$ - 3.3 V TTL level bi-directional pin with source-sink capability of 12 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 3.3 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/OD_{12ts}$ - TTL level bi-directional Schmitt-triggered pin. Open-drain output with 12 mA sink capability** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.8 | 0.9 | 1.0 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.8 | 1.9 | 2.0 | V | $V_{DD}$ = 5 V |
| Hystersis | $V_{TH}$ | 0.8 | 1.0 | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/OD_{12tp3}$ – 3.3 V TTL level bi-directional pin. Open-drain output with 12 mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 3.3V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |

| | | | | | | |
|---|---|---|---|---|---|---|
| **$I/OD_{16cs}$ - CMOS level Schmitt-triggered bi-directional pin. Open-drain output with 16 mA sink capability** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 1.3 | 1.5 | 1.7 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 3.2 | 3.5 | 3.8 | V | $V_{DD}$ = 5 V |
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD}$ = 5 V |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 16 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$I/OD_{24t}$ - TTL level bi-directional pin. Open-drain output with 24 mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5 V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$OD_8$ - Open-drain output pin with sink capability of 8 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| **$OD_{12}$ - Open-drain output pin with sink capability of 12 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| **$OD_{24}$ - Open-drain output pin with sink capability of 24 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| **$OUT_8$ - TTL level output pin with source-sink capability of 8 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -8 mA |
| **$OUT_{12}$ - TTL level output pin with source-sink capability of 12 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| **$OUT_{24}$ - TTL level output pin with source-sink capability of 24 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -24 mA |
| **$OUT_{12tp3}$ - 3.3 V TTL level output pin with source-sink capability of 12 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |

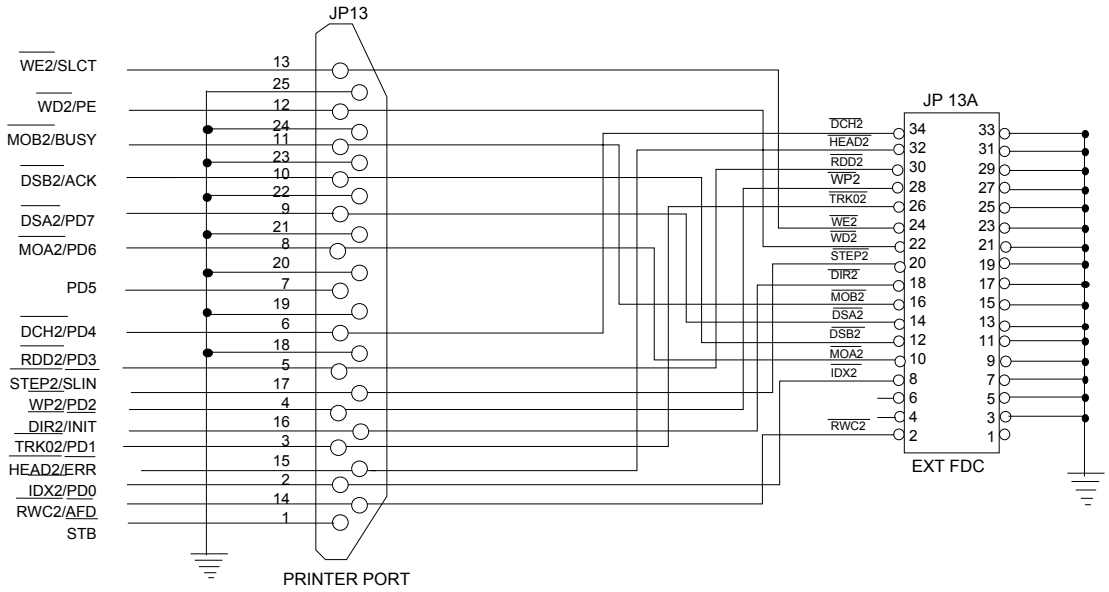
# 9. APPLICATION CIRCUITS

## 9.1 Parallel Port Extension FDD



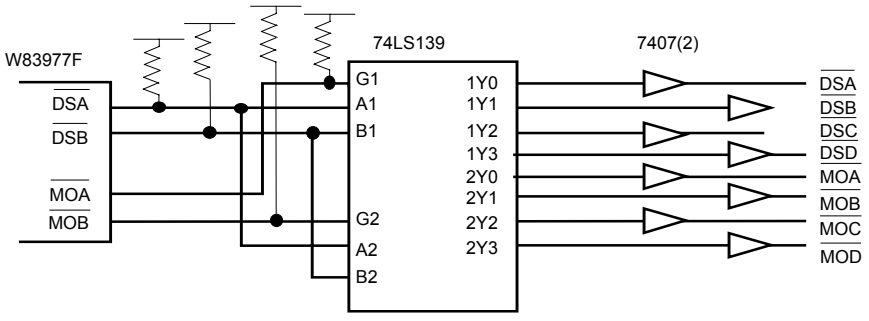

**Parallel Port Extension FDD Mode Connection Diagram**

## 9.2 Parallel Port Extension 2FDD



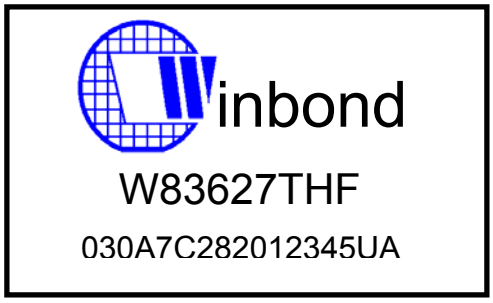

**Parallel Port Extension 2FDD Connection Diagram**

## 9.3 Four FDD Mode



## 10. HOW TO READ THE TOP MARKING

Example: The top marking of W83627THF

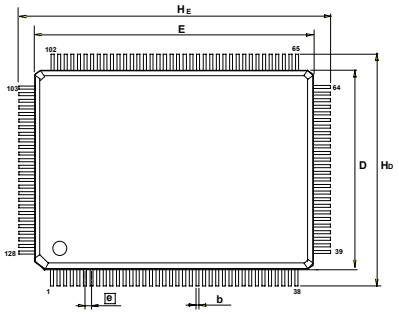



1st line: Winbond logo
2nd line: the type number: W83627THF
3rd line: the tracking code 030A7C282012345UA

**030**: packages made in '00, week 30
**A**: assembly house ID; A means ASE, S means SPIL.... etc.
**7**: code version; 7 means code 007
**C**: IC revision; A means version A, B means version B
**282012345**: wafer production series lot number
**UA**: Winbond internal use.

## 11. PACKAGE DIMENSIONS

### (128-pin QFP)




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| $A_1$ | 0.25 | 0.35 | 0.45 | 0.010 | 0.014 | 0.018 |
| $A_2$ | 2.57 | 2.72 | 2.87 | 0.101 | 0.107 | 0.113 |
| b | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 19.90 | 20.00 | 20.10 | 0.783 | 0.787 | 0.791 |
| e | —— | 0.50 | —— | — | 0.020 | — |
| $H_D$ | 17.00 | 17.20 | 17.40 | 0.669 | 0.677 | 0.685 |
| $H_E$ | 23.00 | 23.20 | 23.40 | 0.905 | 0.913 | 0.921 |
| L | 0.65 | 0.80 | 0.95 | 0.025 | 0.031 | 0.037 |
| $L_1$ | —— | 1.60 | —— | — | 0.063 | — |
| y | —— | —— | 0.08 | — | — | 0.003 |
| θ | 0 | —— | 7 | 0 | — | 7 |

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".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*Please note that all data and specifications are subject to change without notice.*
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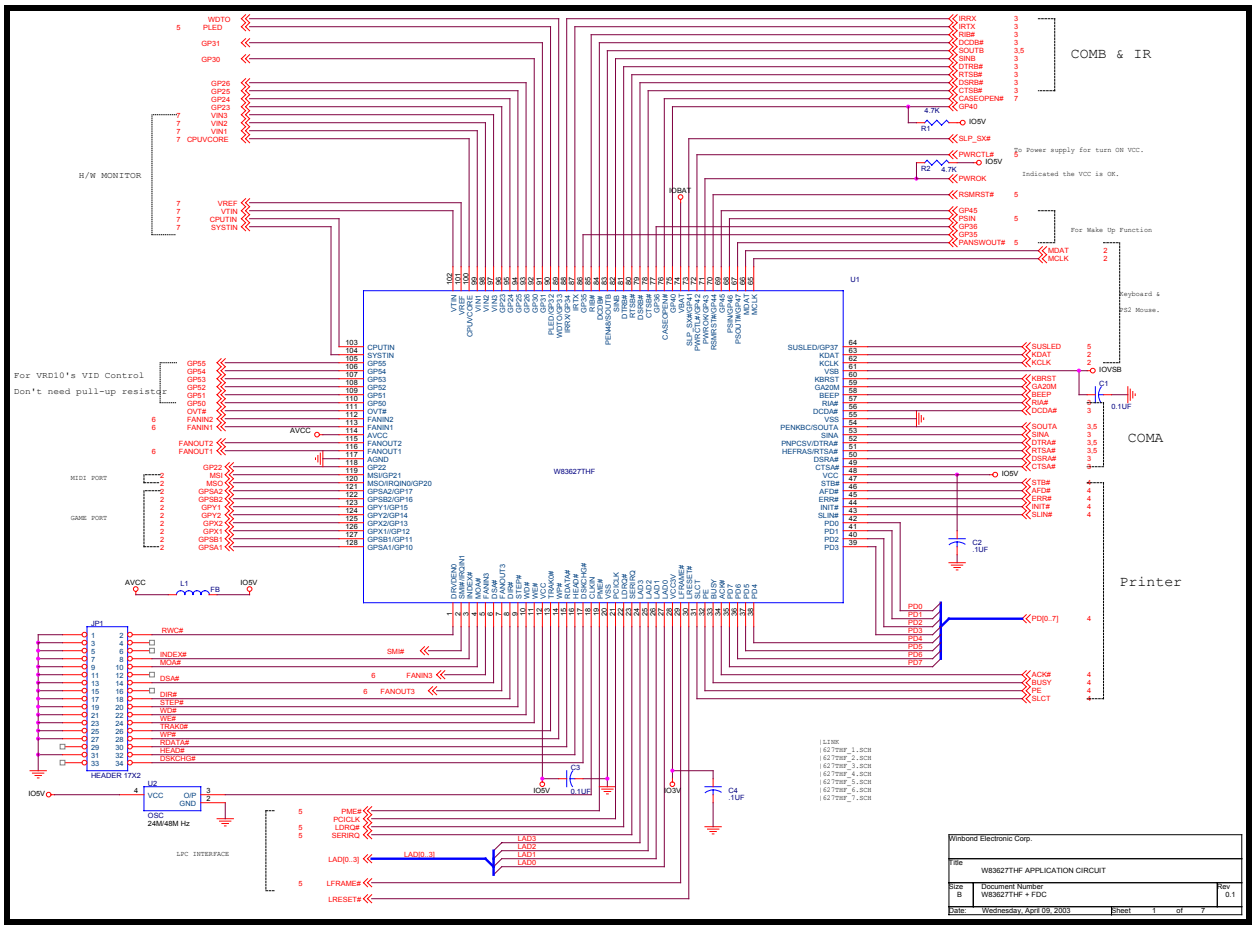
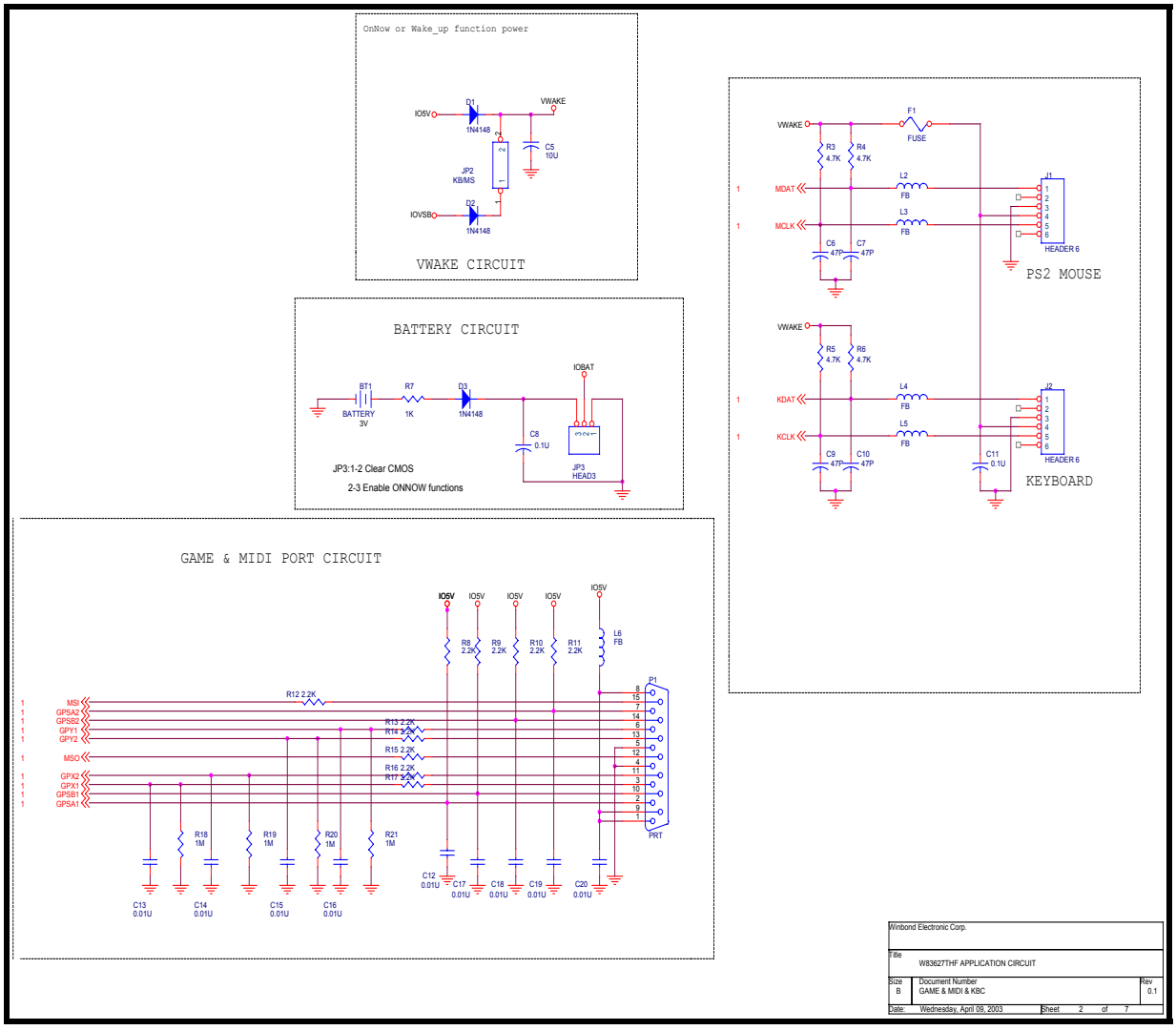
## 12. APPENDIX A : DEMO CIRCUIT




OnNow or Wake_up function power
IO5V
D1
1N4148
VWAKE
C5
10U
JP2
KB/MS
IOVSB
D2
1N4148
VWAKE CIRCUIT
BATTERY CIRCUIT
BT1
BATTERY
3V
R7
1K
D3
1N4148
IOBAT
C8
0.1U
JP3
HEAD3
JP3:1-2 Clear CMOS
2-3 Enable ONNOW functions
VWAKE
F1
FUSE
R3
4.7K
R4
4.7K
MDAT
MCLK
L2
FB
L3
FB
C6
47P
C7
47P
J1
HEADER 6
PS2 MOUSE
R5
4.7K
R6
4.7K
KDAT
KCLK
L4
FB
L5
FB
C9
47P
C10
47P
C11
0.1U
J2
HEADER 6
KEYBOARD
GAME & MIDI PORT CIRCUIT
L6
FB
R8
2.2K
R9
2.2K
R10
2.2K
R11
2.2K
R12 2.2K
R13 2.2K
R14 2.2K
R15 2.2K
R16 2.2K
R17 2.2K
MSI
GPSA2
GPSB2
GPY1
GPY2
MSO
GPX2
GPX1
GPSB1
GPSA1
P1
PRT
R18
1M
R19
1M
R20
1M
R21
1M
C12
0.01U
C17
0.01U
C18
0.01U
C19
0.01U
C20
0.01U
C13
0.01U
C14
0.01U
C15
0.01U
C16
0.01U
Winbond Electronic Corp.
Title
W83627THF APPLICATION CIRCUIT
Size
B
Document Number
GAME & MIDI & KBC
Rev
0.1
Date:
Wednesday, April 09, 2003
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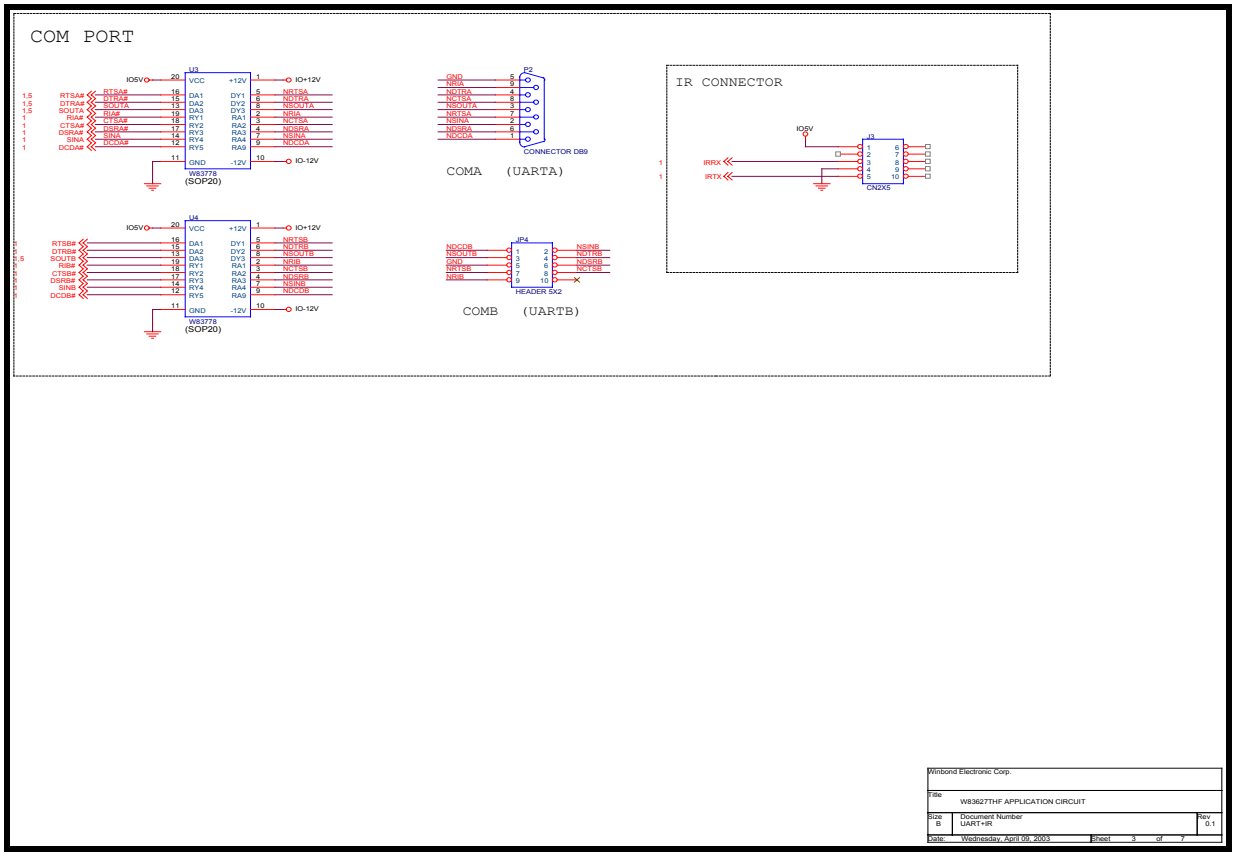
7


COM PORT
IO5V
U3
VCC
+12V
IO+12V
GND
-12V
IO-12V
W83778
(SOP20)
RTSA#
DTRA#
SOUTA
RIA#
CTSA#
DSRA#
SINA
DCDA#
NRTSA
NDTRA
NSOUTA
NRIA
NCTSA
NDSRA
NSINA
NDCDA
U4
RTSB#
DTRB#
SOUTB
RIB#
CTSB#
DSRB#
SINB
DCDB#
NRTSB
NDTRB
NSOUTB
NRIB
NCTSB
NDSRB
NSINB
NDCDB
P2
CONNECTOR DB9
COMA (UARTA)
JP4
HEADER 5X2
COMB (UARTB)
IR CONNECTOR
J3
IRRX
IRTX
CN2X5
Winbond Electronic Corp.
Title
W83627THF APPLICATION CIRCUIT
Size
B
Document Number
UART+IR
Rev
0.1
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Wednesday, April 09, 2003
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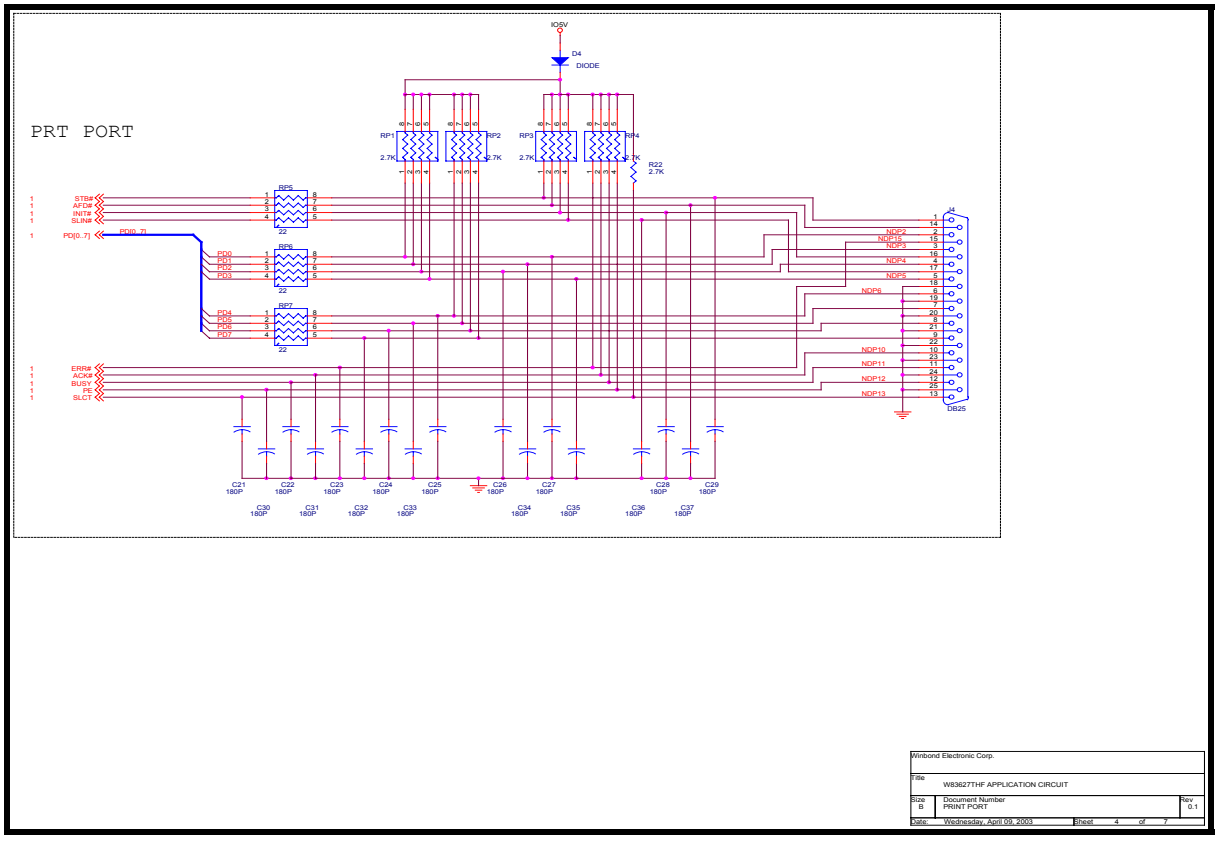
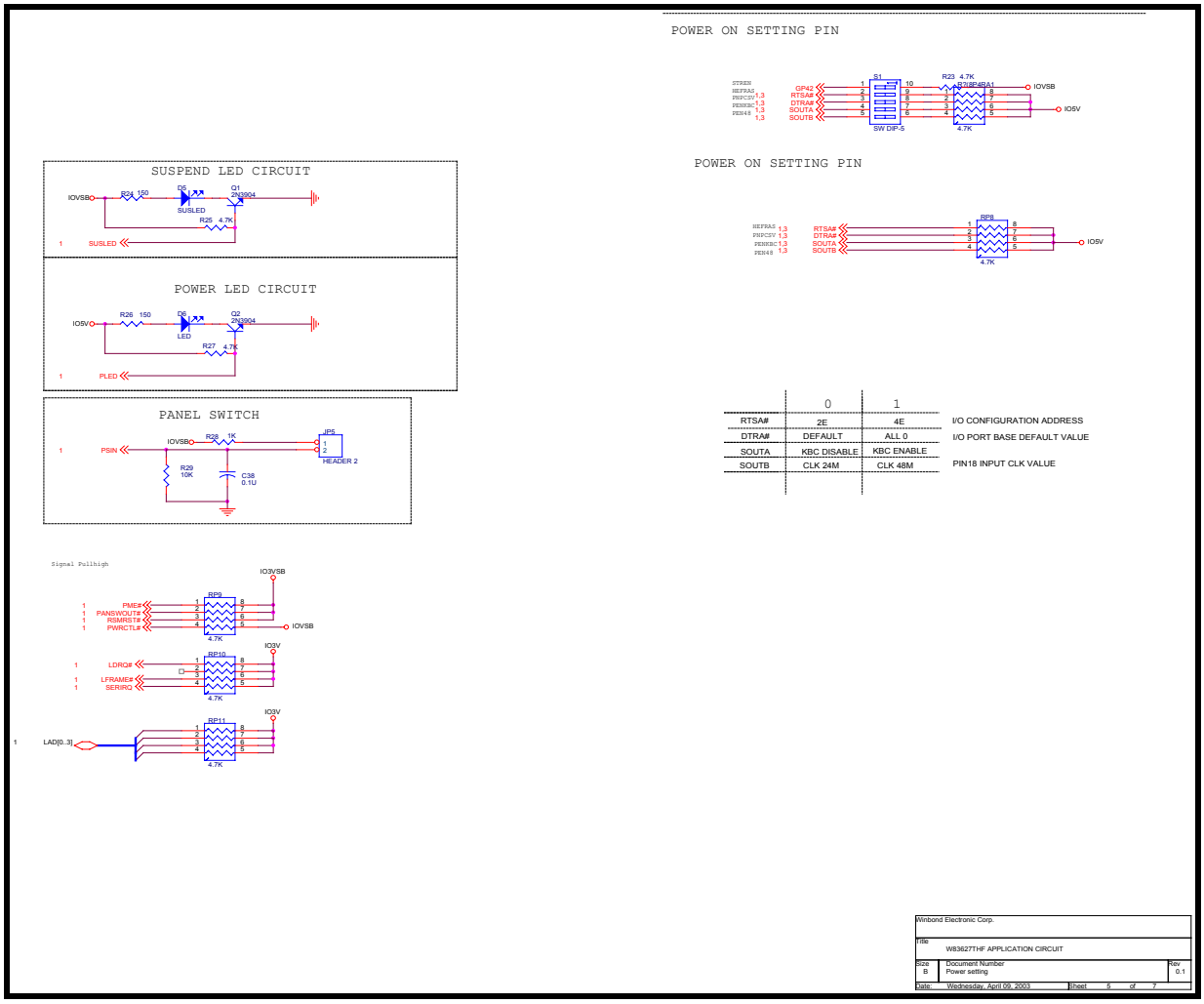
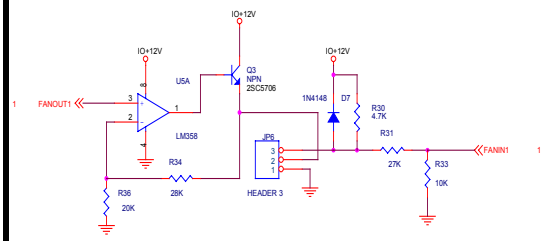

PRT PORT
IO5V
D4
DIODE
RP1
RP2
RP3
RP4
2.7K
R22
2.7K
RP5
RP6
RP7
22
STB#
AFD#
INIT#
SLIN#
PD[0..7]
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
ERR#
ACK#
BUSY
PE
SLCT
NDP2
NDP15
NDP3
NDP4
NDP5
NDP6
NDP10
NDP11
NDP12
NDP13
DB25
C21 180P
C22 180P
C23 180P
C24 180P
C25 180P
C26 180P
C27 180P
C28 180P
C29 180P
C30 180P
C31 180P
C32 180P
C33 180P
C34 180P
C35 180P
C36 180P
C37 180P
Winbond Electronic Corp.
Title
W83627THF APPLICATION CIRCUIT
Size B
Document Number
PRINT PORT
Rev 0.1
Date: Wednesday, April 09, 2003
Sheet 4 of 7

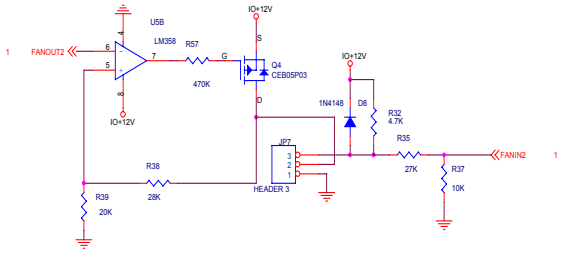

POWER ON SETTING PIN
SW DIP-5
4.7K
IOVSB
IO5V
POWER ON SETTING PIN
SUSPEND LED CIRCUIT
SUSLED
POWER LED CIRCUIT
LED
PANEL SWITCH
HEADER 2
Signal Pullhigh
IO3VSB
PME#
PANSWOUT#
RSMRST#
PWRCTL#
LDRQ#
LFRAME#
SERIRQ
LAD[0..3]
RTSA#
DTRA#
SOUTA
SOUTB
0
1
2E
4E
I/O CONFIGURATION ADDRESS
DEFAULT
ALL 0
I/O PORT BASE DEFAULT VALUE
KBC DISABLE
KBC ENABLE
CLK 24M
CLK 48M
PIN18 INPUT CLK VALUE
Winbond Electronic Corp.
W83627THF APPLICATION CIRCUIT
Power setting
Wednesday, April 09, 2003

Circuit for DC FAN speed control

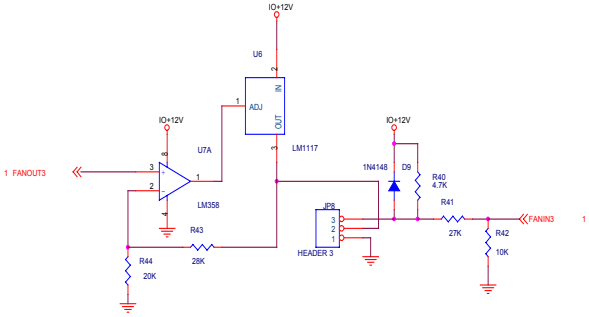
Type 1 : Transistor 2SC5706




Type 2 : PMOS CEB05P03



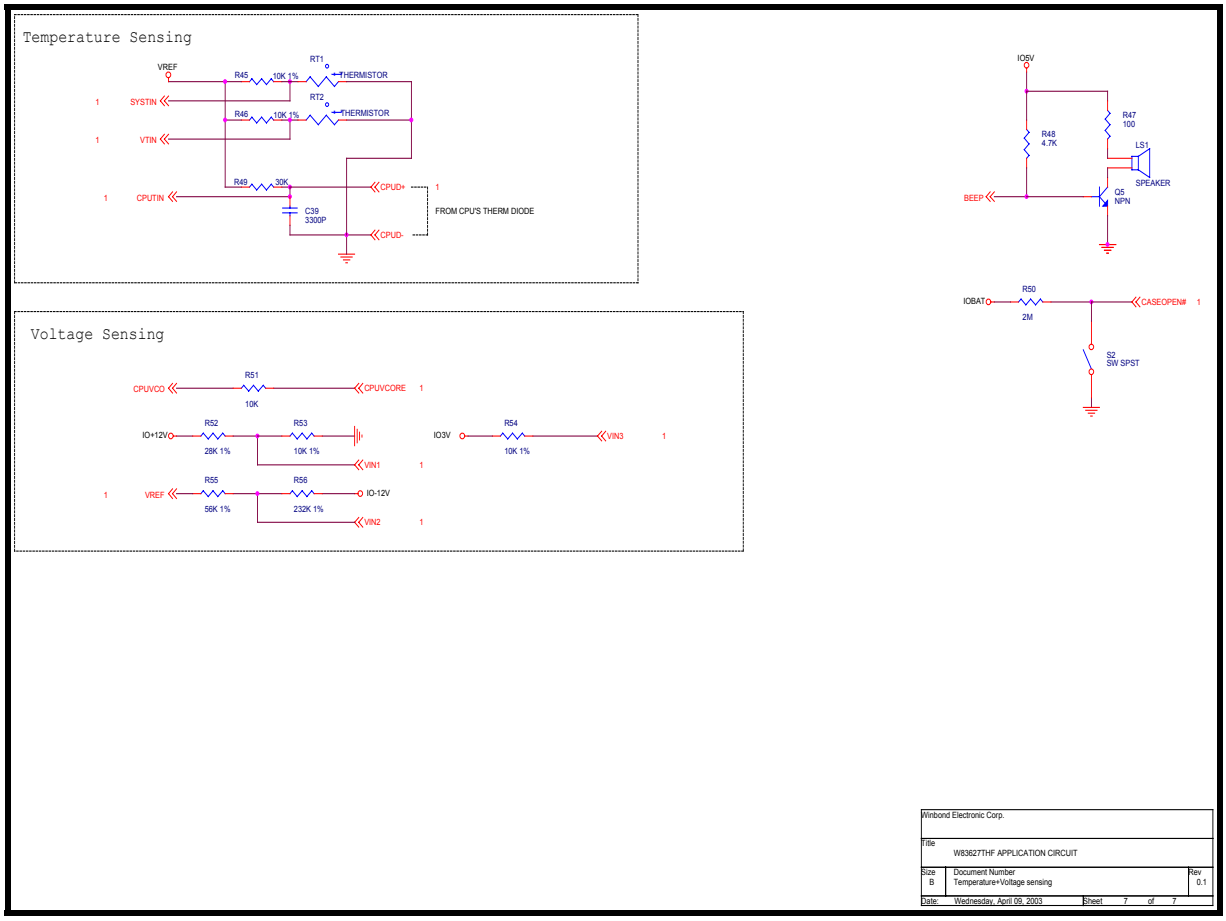

Type 3 : LDO LM1117




Note :

1. Transistor,MOSFET,LDO
   We suggest TO-252 or TO-262 type of package
2. Use 2SC5706, Max. FANVCC is 10.2V
3. Use CEB05P03, Max. FANVCC is 12V
4. Use LM1117, Max. FANVCC max is 10.8V

| | | |
|---|---|---|
| Winbond Electronic Corp. | | |
| Title: W83627THF APPLICATION CIRCUIT | | |
| Size: B | Document Number: FAN Control | Rev: 0.1 |
| Date: Wednesday, April 09, 2003 | Sheet 6 of 7 | |


Temperature Sensing
VREF
R45 10K 1%
RT1
THERMISTOR
SYSTIN
R46 10K 1%
RT2
THERMISTOR
VTIN
R49 30K
CPUTIN
CPUD+
C39 3300P
CPUD-
FROM CPU'S THERM DIODE
Voltage Sensing
CPUVCO
R51 10K
CPUVCORE
IO+12V
R52 28K 1%
R53 10K 1%
VIN1
IO3V
R54 10K 1%
VIN3
VREF
R55 56K 1%
R56 232K 1%
IO-12V
VIN2
IO5V
R47 100
R48 4.7K
LS1
SPEAKER
BEEP
Q5 NPN
IOBAT
R50 2M
CASEOPEN#
S2 SW SPST
Winbond Electronic Corp.
Title
W83627THF APPLICATION CIRCUIT
Size B
Document Number
Temperature+Voltage sensing
Rev 0.1
Date: Wednesday, April 09, 2003
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