

GaAs PHEMT MMIC MODULATOR DRIVER AMPLIFIER, DC - 20.0 GHz

Typical Applications

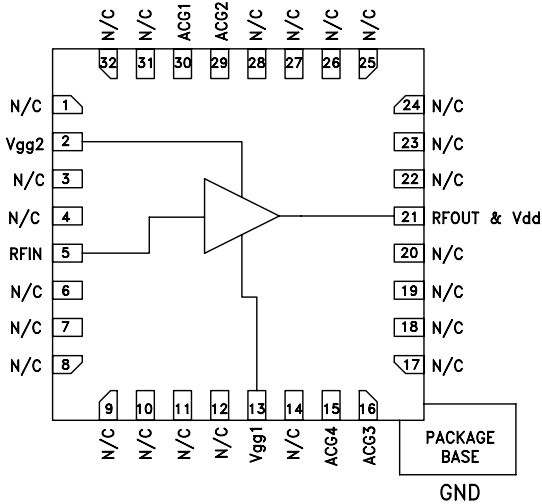
The HMC465LP5 wideband driver is ideal for:

- OC192 LN/MZ Modulator Driver
- Microwave Radio & VSAT
- Test Instrumentation
- Military EW, ECM & C³I

Features

- Gain: 15 dB
- Output Voltage to 10Vpk-pk
- +24 dBm Saturated Output Power
- Supply Voltage: +8V @160 mA
- 50 Ohm Matched Input/Output
- 25mm² Leadless SMT Package

Functional Diagram



General Description

The HMC465LP5 is a GaAs MMIC PHEMT Distributed Driver Amplifier packaged in a leadless 5 x 5 mm surface mount package which operates between DC and 20 GHz. The amplifier provides 15 dB of gain, 3 dB noise figure and +25 dBm of saturated output power while requiring only 160 mA from a +8V supply. Gain flatness is excellent at ±0.25 dB as well as +/- 4 deg deviation from linear phase from DC - 10 GHz making the HMC465LP5 ideal for OC192 fiber optic LN/MZ modulator driver amplifier as well as test equipment applications. The HMC465LP5 amplifier I/Os are internally matched to 50 Ohms.

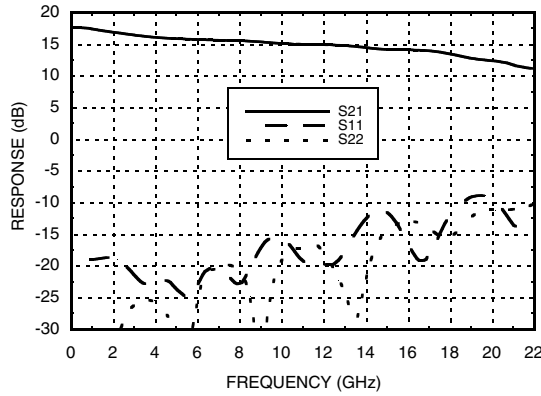
Electrical Specifications, $T_A = +25^\circ C, V_{dd} = 8V, V_{gg2} = 1.5V, I_{dd} = 160 mA^*$

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range	DC - 6.0			6.0 - 12.0			12.0 - 20.0			GHz
Gain	13	16		12	15		9.5	12.5		dB
Gain Flatness		±0.75			±0.25			±1.5		dB
Gain Variation Over Temperature		0.015	0.02		0.020	0.025		0.035	0.045	dB/ °C
Noise Figure		3.0			3.0			4.0		dB
Input Return Loss		20			15			8		dB
Output Return Loss		22			17			12		dB
Output Power for 1 dB Compression (P1dB)	21	24		20	23		16	20		dBm
Saturated Output Power (P _{sat})		25.5			25			23		dBm
Output Third Order Intercept (IP3)		32			28			24		dBm
Saturated Output Voltage		10			10			8		Vpk-pk
Group Delay Variation		±15			±15					pSec
Supply Current (I _{dd}) (V _{dd} = 8V, V _{gg1} = -0.6V Typ.)		160			160			160		mA

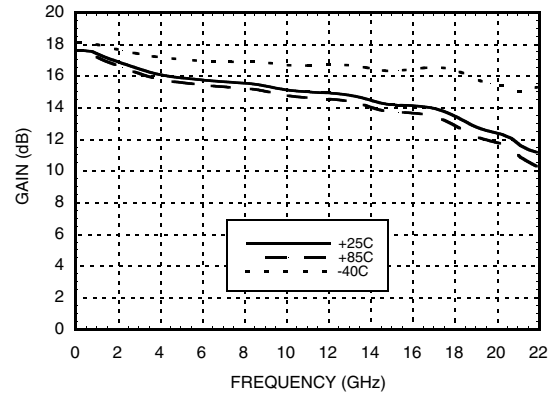
* Adjust V_{gg1} between -2 to 0V to achieve I_{dd}= 160 mA typical.

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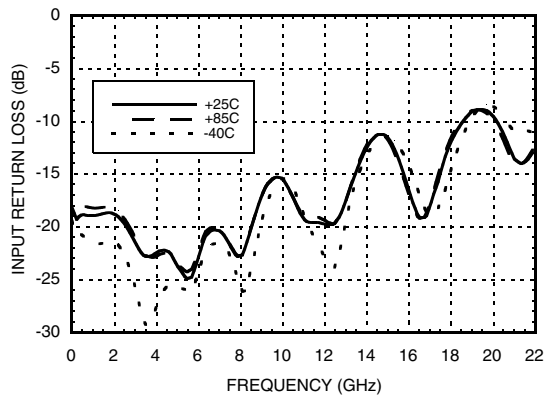
Gain & Return Loss



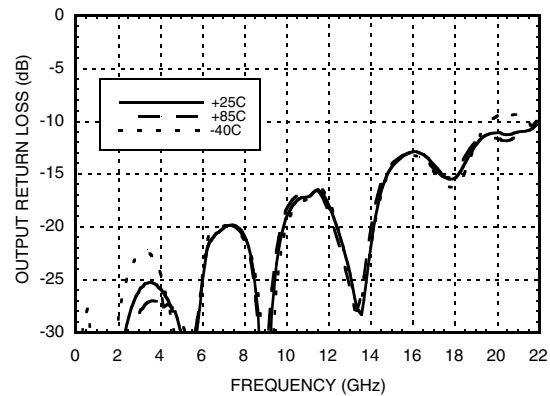
Gain vs. Temperature



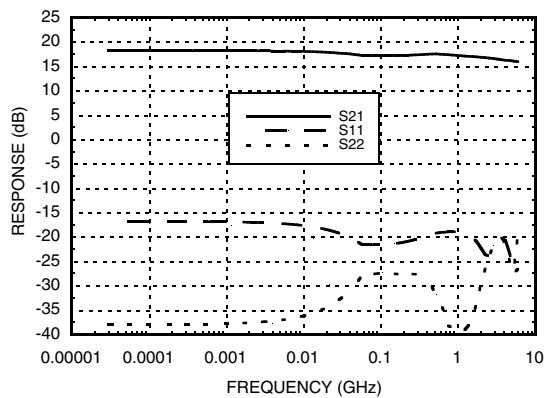
Input Return Loss vs. Temperature



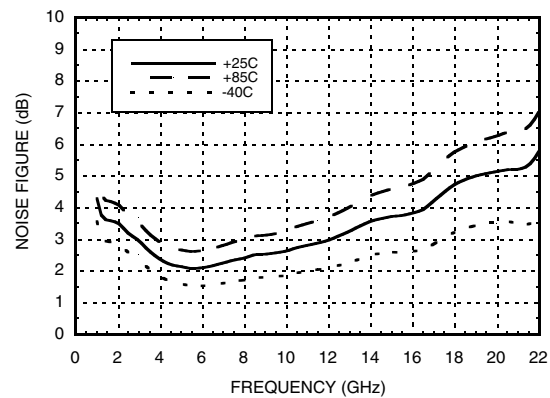
Output Return Loss vs. Temperature



Low Frequency Gain & Return Loss



Noise Figure vs. Temperature

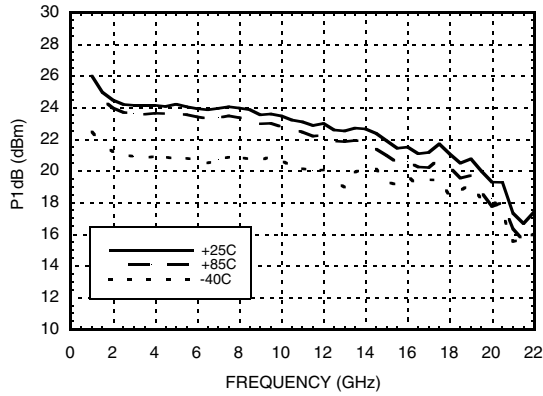


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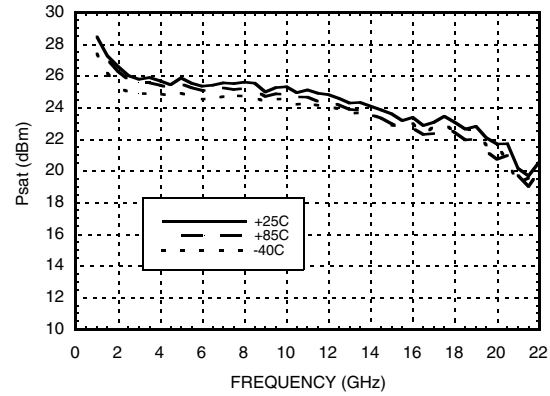
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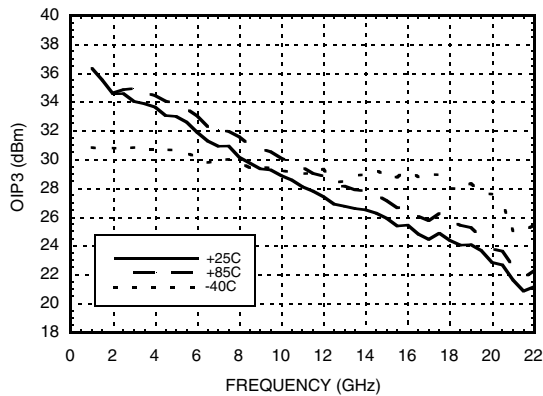
P1dB vs. Temperature



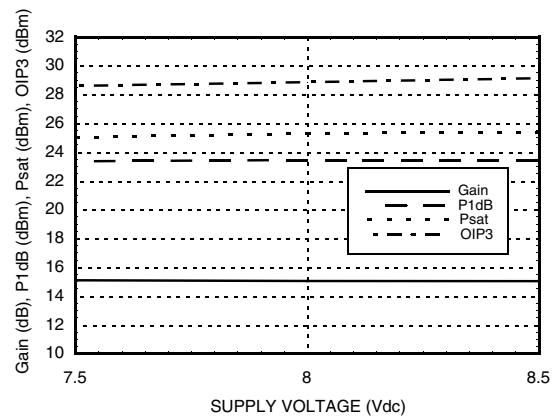
Psat vs. Temperature



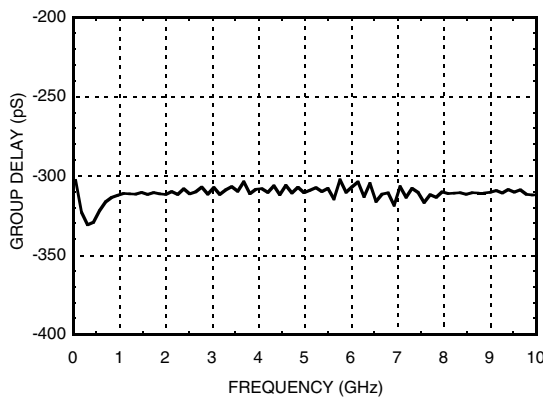
Output IP3 vs. Temperature



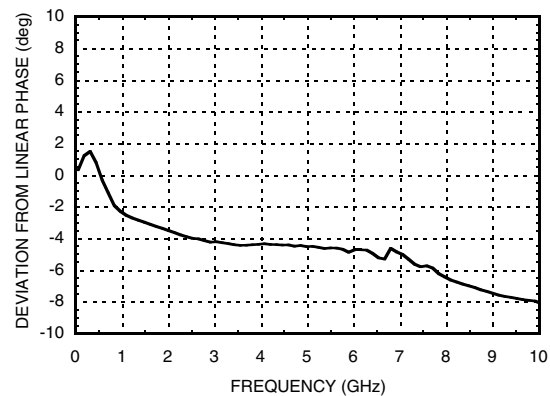
Gain, Power & OIP3 vs. Supply Voltage @ 10 GHz, Idd= 160mA



Group Delay



Deviation from Linear Phase



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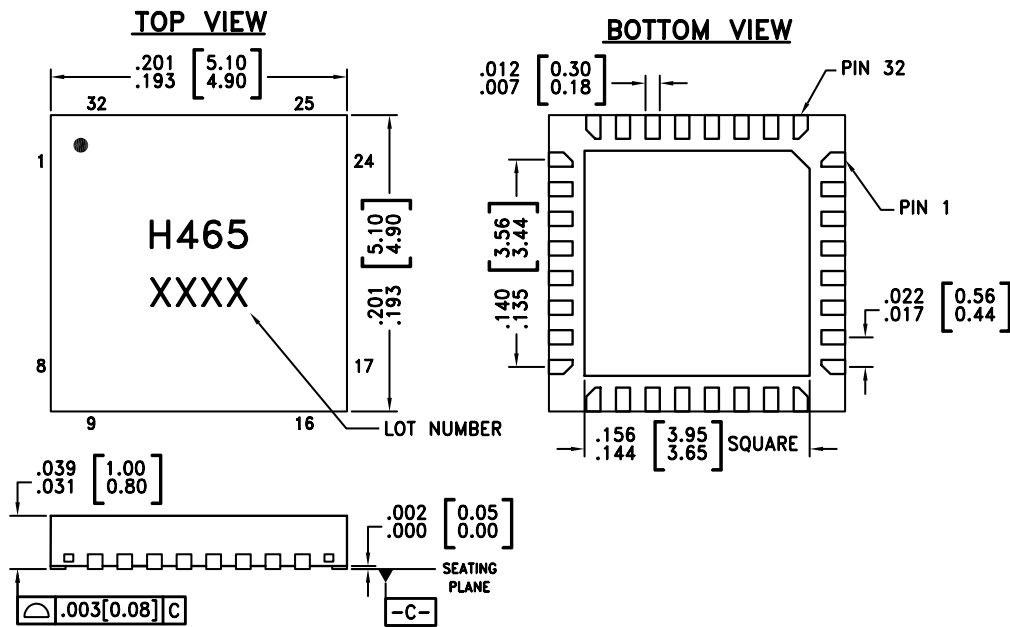
Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+9.0 Vdc
Gate Bias Voltage (Vgg1)	-2.0 to 0 Vdc
Gate Bias Voltage (Vgg2)	(Vdd -8.0) Vdc to Vdd
RF Input Power (RFIn)(Vdd = +8.0 Vdc)	+23 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 24 mW/°C above 85 °C)	1.56 W
Thermal Resistance (channel to ground paddle)	41.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+7.5	161
+8.0	160
+8.5	159

Outline Drawing



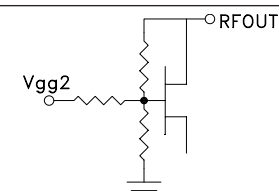
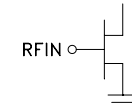
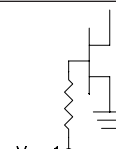
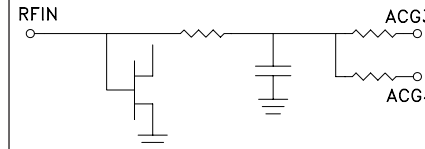
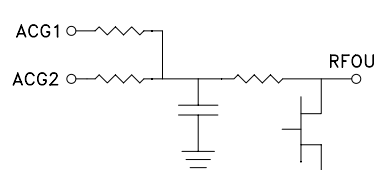

NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS]
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX
7. PACKAGE WRAP SHALL NOT EXCEED 0.05mm
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order Online at www.hittite.com

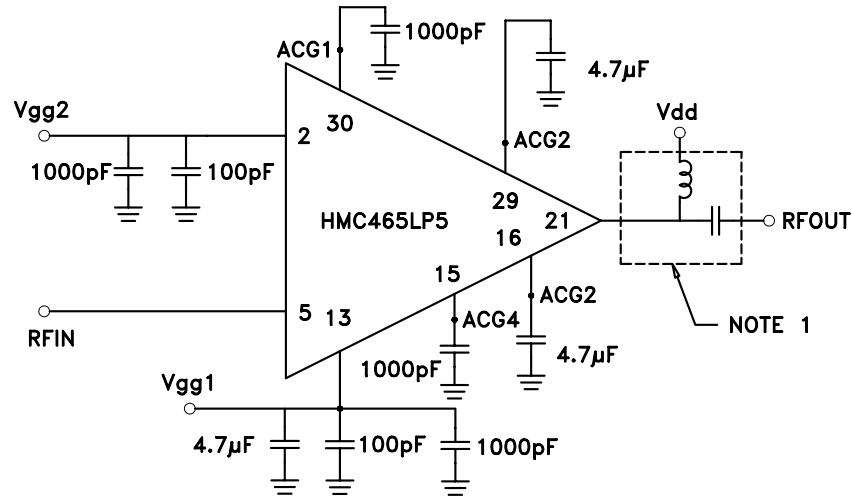
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Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 3, 4, 6-12, 14, 17, 18, 20, 22-28, 31, 32	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
2	Vgg2	Gate Control 2 for amplifier. +1.5V should be applied to Vgg2 for nominal operation.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms from DC - 20.0 GHz.	
13	Vgg1	Gate Control 1 for amplifier.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	

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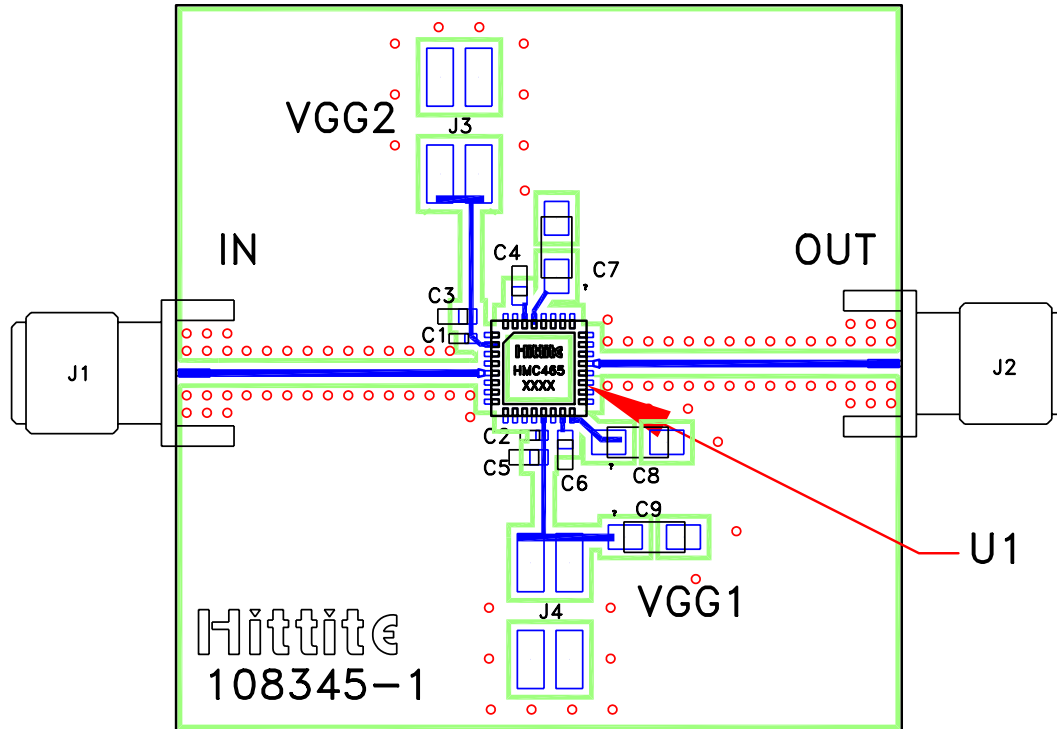
Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

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Evaluation PCB



List of Materials for Evaluation PCB 108347 *

Item	Description
J1 - J2	SRI K Connector
J3 - J4	2mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3 - C6	1000 pF Capacitor, 0603 Pkg.
C7 - C9	4.7 μ F Capacitor, Tantalum
U1	HMC465LP5
PCB**	108345 Evaluation PCB

** Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

* Reference this number when ordering complete evaluation PCB.



v00.0404

HMC465LP5

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Notes:

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