

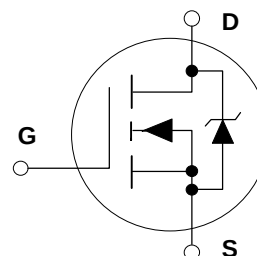
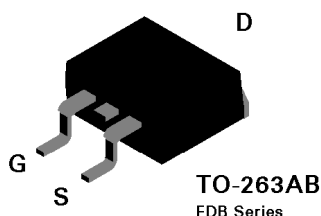
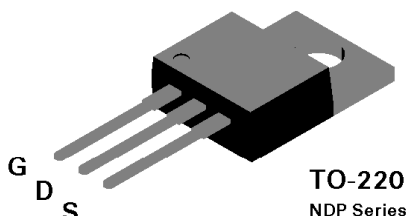
NDP508A / NDP508AE / NDP508B / NDP508BE **NDB508A / NDB508AE / NDB508B / NDB508BE** **N-Channel Enhancement Mode Field Effect Transistor**

General Description

These N-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 19 and 17A, 80V. $R_{DS(ON)} = 0.08$ and 0.10Ω .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design (3 million/in²) for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.



Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDP508A NDB508A	NDP508AE NDB508AE	NDP508B NDB508B	NDP508BE NDB508BE	Units
V_{DS}	Drain-Source Voltage	80		80		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1\text{ M}\Omega$)	80		80		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		± 20		V
	- Nonrepetitive ($t_p < 50\text{ }\mu\text{s}$)	± 40		± 40		V
I_D	Drain Current - Continuous	19		17		A
	- Pulsed	57		51		A
P_D	Total Power Dissipation @ $T_c = 25^\circ\text{C}$	75		75		W
	Derate above 25°C	0.5		0.5		W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		-65 to 175		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		275		$^\circ\text{C}$

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)							
E _{AS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 25 V, I _D = 19 A	NDP508AE NDP508BE			55	mJ
I _{AR}	Maximum Drain-Source Avalanche Current		NDB508AE NDB508BE			19	A
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	ALL	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	ALL			250	μA
		T _J = 125°C				1	mA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	ALL			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	ALL			-100	nA
ON CHARACTERISTICS (Note 2)							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	ALL	2	2.9	4	V
		T _J = 125°C		1.4	2.3	3.6	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 9.5 A	NDP508A NDP508AE NDB508A		0.057	0.08	Ω
		T _J = 125°C	NDB508AE		0.097	0.16	Ω
		V _{GS} = 10 V, I _D = 8.5 A	NDP508B NDP508BE NDB508B			0.1	Ω
		T _J = 125°C	NDB508BE			0.2	Ω
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 10 V	NDP508A NDP508AE NDB508A NDB508AE	19			A
			NDP508B NDP508BE NDB508B NDB508BE	17			A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 9.5 A	ALL	6	9.6		S
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	ALL		750	900	pF
C _{oss}	Output Capacitance		ALL		200	250	pF
C _{rss}	Reverse Transfer Capacitance		ALL		60	90	pF

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
t _{D(ON)}	Turn - On Delay Time	V _{DD} = 40 V, I _D = 19 A, V _{GS} = 10 V, R _{GEN} = 15 Ω	ALL		8.5	20	nS
t _r	Turn - On Rise Time		ALL		66	110	nS
t _{D(OFF)}	Turn - Off Delay Time		ALL		31	50	nS
t _f	Turn - Off Fall Time		ALL		48	80	nS
Q _g	Total Gate Charge	V _{DS} = 64 V, I _D = 19 A, V _{GS} = 10 V	ALL		23.5	34	nC
Q _{gs}	Gate-Source Charge		ALL		4.5		nC
Q _{gd}	Gate-Drain Charge		ALL		11.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
I _S	Maximum Continuous Drain-Source Diode Forward Current	NDP508A NDP508AE NDB508A NDB508AE				19	A
		NDP508B NDP508BE NDB508B NDB508BE				17	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	NDP508A NDP508AE NDB508A NDB508AE				57	A
		NDP508B NDP508BE NDB508B NDB508BE				51	A
V _{SD} (Note 2)	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9.5 A T_J = 125°C	ALL		0.87	1.3	V
					0.79	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 19 A, di _S /dt = 100 A/μs	ALL		78	110	ns
I _{rr}	Reverse Recovery Current		ALL		5.2	75	A
THERMAL CHARACTERISTICS							
R _{θJC}	Thermal Resistance, Junction-to-Case		ALL			2	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient		ALL			62.5	°C/W

Notes:

1. NDP508A/508B and NDB508A/508B are not rated for operation in avalanche mode.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

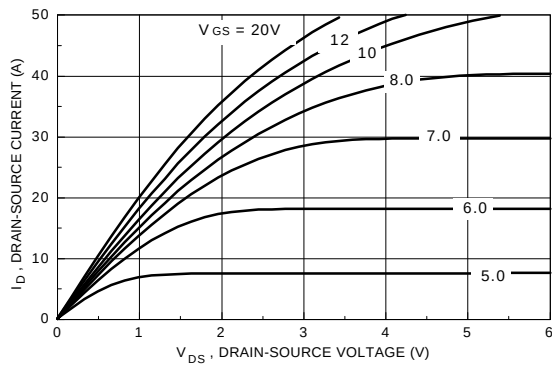


Figure 1. On-Region Characteristics.

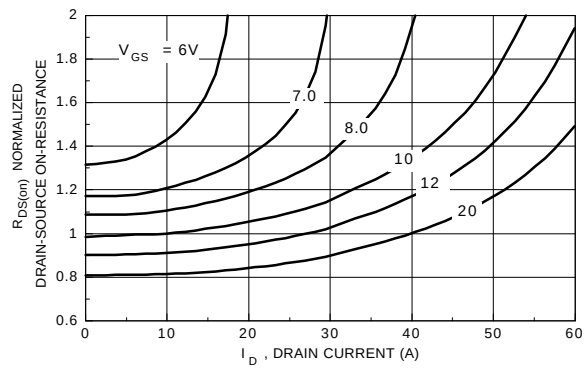


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

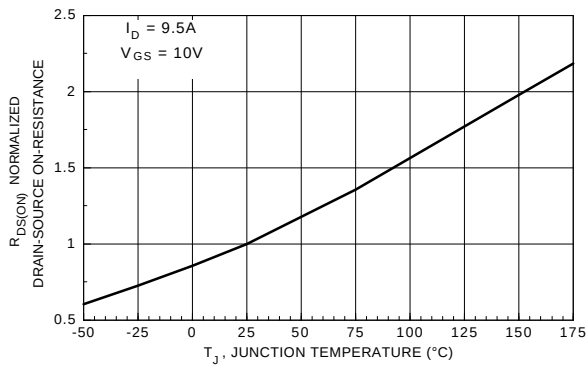


Figure 3. On-Resistance Variation with Temperature.

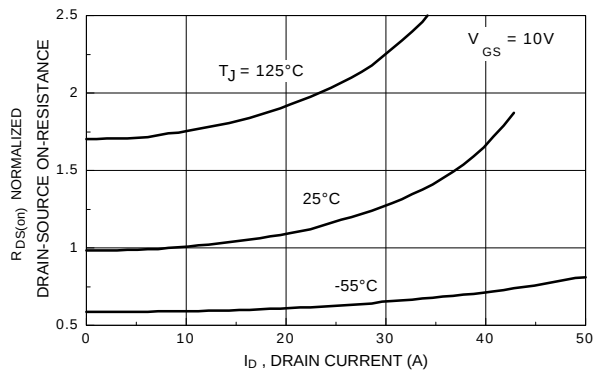


Figure 4. On-Resistance Variation with Drain Current and Temperature.

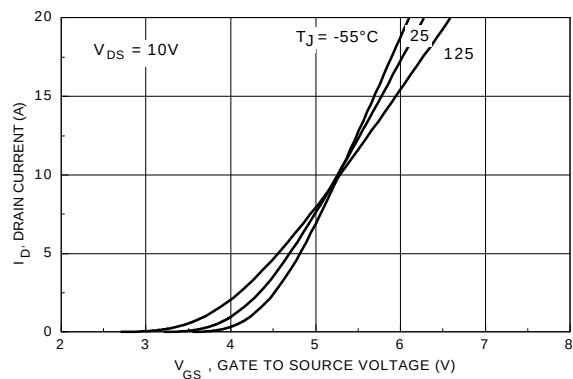


Figure 5. Transfer Characteristics.

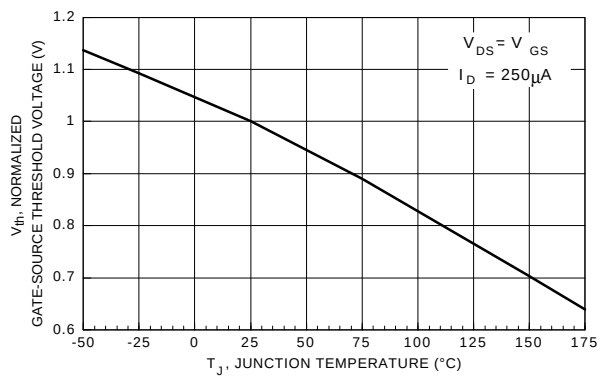


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

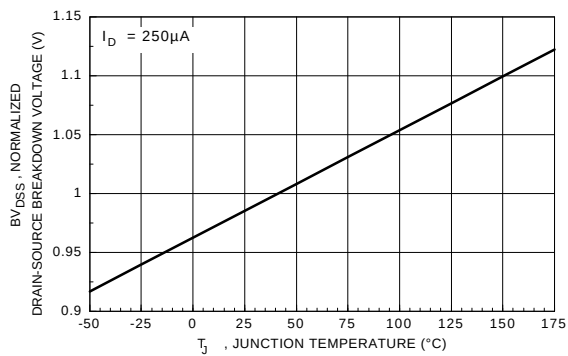


Figure 7. Breakdown Voltage Variation with Temperature.

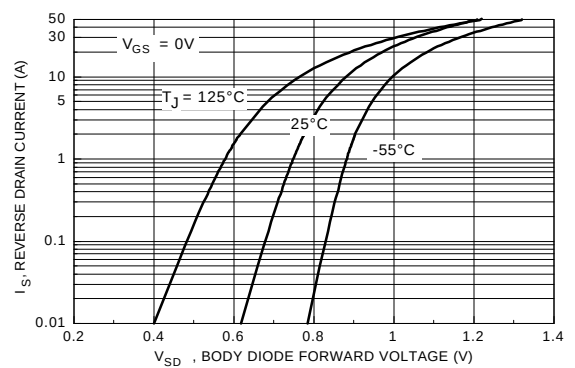


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

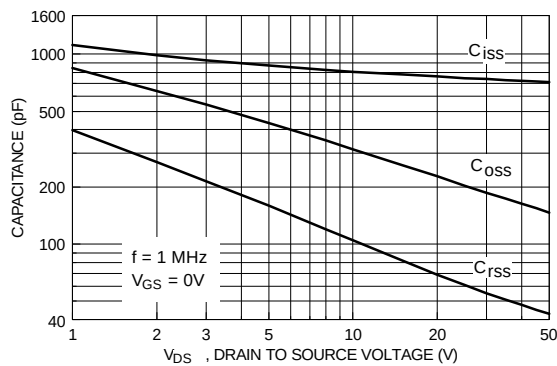


Figure 9. Capacitance Characteristics.

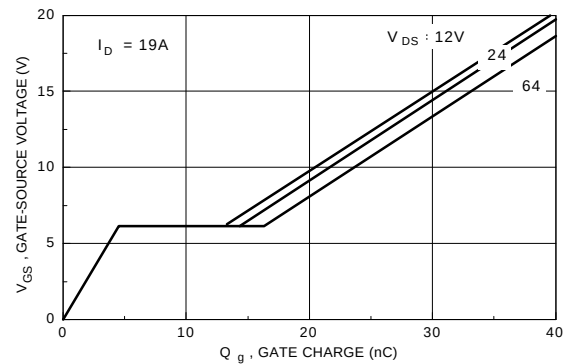


Figure 10. Gate Charge Characteristics.

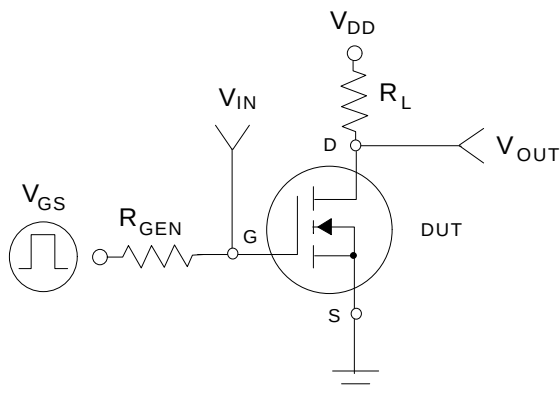


Figure 11. Switching Test Circuit.

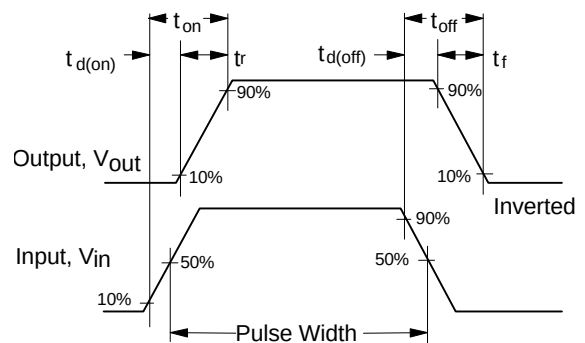


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

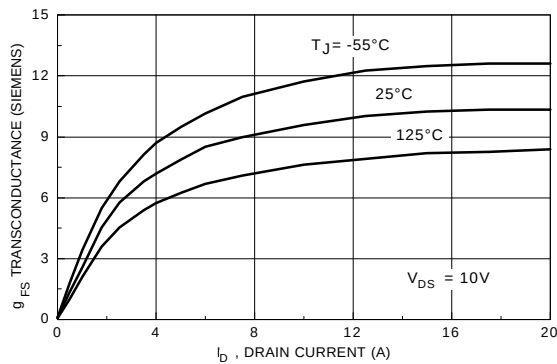


Figure 13. Transconductance Variation with Drain Current and Temperature.

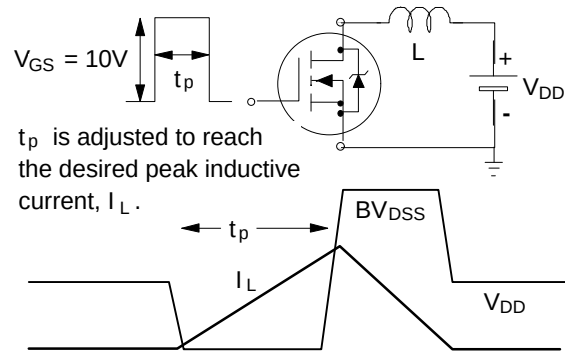


Figure 14. Unclamped Inductive Load Circuit and Waveforms.

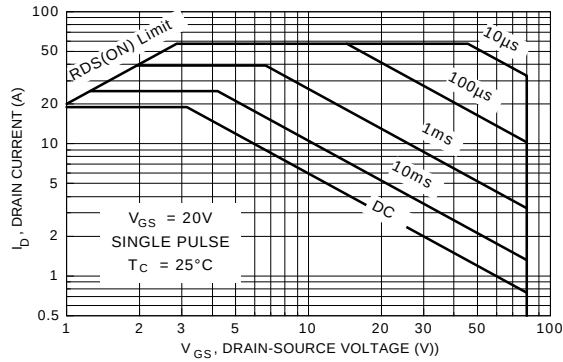


Figure 15. Maximum Safe Operating Area.

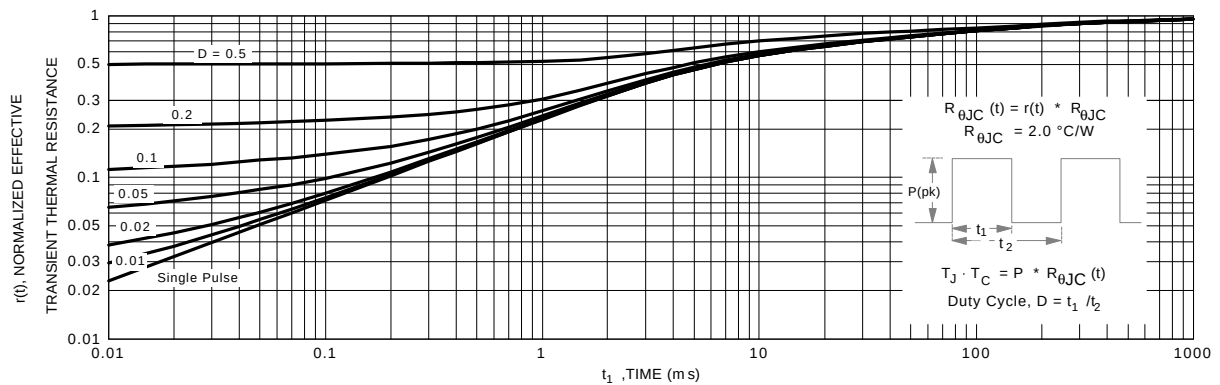


Figure 16. Transient Thermal Response Curve.