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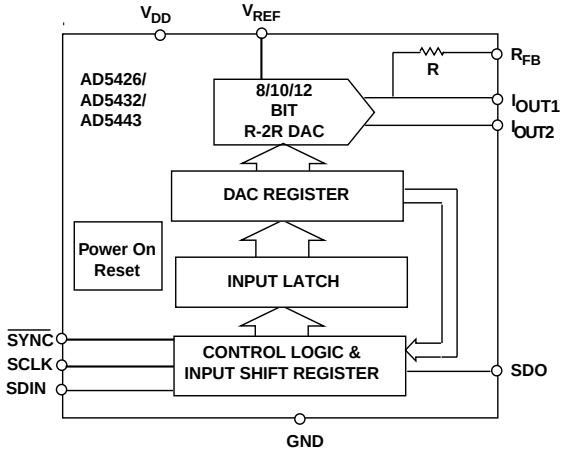
# High Bandwidth CMOS 8/10/12-Bit Serial Interface Multiplying DACs

## Preliminary Technical Data — AD5426/AD5432/AD5443*

**FEATURES**
**+2.5 V to +5.5 V Supply Operation**
**50MHz Serial Interface**
**10MHz Multiplying Bandwidth**
**±10V Reference Input**
**10-Lead µSOIC Package**
**Pin Compatible 8, 10 and 12 Bit Current Output DACs**
**Guaranteed Monotonic**
**Four Quadrant Multiplication**
**Power On Reset**
**Daisy Chain Mode**
**Readback Function**
**5µA typical Power Consumption**

**APPLICATIONS**
**Portable Battery Powered Applications**
**Waveform Generators**
**Analog Processing**
**Instrumentation Applications**
**Programmable Amplifiers and Attenuators**
**Digitally-Controlled Calibration**
**Programmable Filters and Oscillators**
**Composite Video**
**Ultrasound**
**Gain, offset and Voltage Trimming**

**FUNCTIONAL BLOCK DIAGRAM**




**GENERAL DESCRIPTION**

The AD5426/AD5432/AD5443 are CMOS 8, 10 and 12-bit Current Output digital-to-analog converters respectively.

These devices operate from a +2.5 V to 5.5 V power supply, making them suited to battery powered applications and many other applications.

These DACs utilize double buffered 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE™ and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS sub micron process, they offer excellent four quadrant multiplication characteristics, with large signal multiplying bandwidths of 10MHz.

The applied external reference input voltage ($V_{REF}$) determines the full scale output current. An integrated feedback resistor ($R_{FB}$) provides temperature tracking and full scale voltage output when combined with an external Current to Voltage precision amplifier.

The AD5426/AD5432/AD5443 DACs are available in small 10-lead µSOIC packages.

**PRODUCT HIGHLIGHTS**

1. 10MHz Multiplying Bandwidth
2. 3mm x 5mm 10-lead µSOIC package
3. Low Voltage, Low Power Current Output DACs.

*US Patent Number 5,689,257
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

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# AD5426/AD5432/AD5443–SPECIFICATIONS[1]

($V_{DD}$ = 2.5 V to 5.5 V, $V_{REF}$ = +10 V, $I_{OUT}x$ = 0 V. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. DC performance measured with OP1177, AC performance with AD811 unless otherwise noted.)

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| AD5426 | | | | | |
| Resolution | | | 8 | Bits | |
| Relative Accuracy | | | ±0.5 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| AD5432 | | | | | |
| Resolution | | | 10 | Bits | |
| Relative Accuracy | | | ±1 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| AD5443 | | | | | |
| Resolution | | | 12 | Bits | |
| Relative Accuracy | | | ±2 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| Gain Error | | | ±2 | mV | |
| Gain Error Temp Coefficient[2] | | ±5 | | ppm FSR/°C | |
| Output Leakage Current | | | ±10 | nA | Data = $0000_H$, $T_A$ = 25°C, $I_{OUT1}$ |
| | | | ±50 | nA | Data = $0000_H$, $I_{OUT1}$ |
| Output Voltage Compliance Range | | TBD | | V | |
| REFERENCE INPUT[2] | | | | | |
| Reference Input Range | | ±10 | | V | |
| $V_{REF}$ Input Resistance | 8 | 10 | 12 | kΩ | Input resistance TC = -50ppm/°C |
| DIGITAL INPUTS/OUTPUT[2] | | | | | |
| Input High Voltage, $V_{IH}$ | 1.7 | | | V | $V_{DD}$ = 2.5 V to 5.5 V |
| Input Low Voltage, $V_{IL}$ | | | 0.8 | V | $V_{DD}$ = 2.7 V to 5.5 V |
| | | | 0.7 | V | $V_{DD}$ = 2.5 V to 2.7 V |
| Input Leakage Current, $I_{IL}$ | | | 1 | µA | |
| Input Capacitance | | | 10 | pF | |
| $V_{DD}$ = 4.5 V to 5.5 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ - 1 | | | V | $I_{SOURCE}$ = 200 µA |
| $V_{DD}$ = 2.5 V to 3.6 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ - 0.5 | | | V | $I_{SOURCE}$ = 200 µA |
| DYNAMIC PERFORMANCE[2] | | | | | |
| Reference Multiplying BW | 10 | | | MHz | $V_{REF}$ = 100 mV rms, DAC loaded all 1s |
| | TBD | | | MHz | $V_{REF}$ = 6 V rms, DAC loaded all 1s |
| Output Voltage Settling Time | | | | | |
| AD5426 | | 30 | TBD | ns | Measured to ½ LSB. $R_{LOAD}$ = 100Ω, $C_{LOAD}$ = 15pF. |
| AD5432 | | 35 | TBD | ns | DAC latch alternately loaded with 0s and 1s. |
| AD5443 | | 40 | TBD | ns | |
| Slew Rate | | 100 | | V/µs | |
| Digital to Analog Glitch Impulse | | 3 | | nV-s | 1 LSB change around Major Carry |
| Multiplying Feedthrough Error | | | -75 | dB | DAC latch loaded with all 0s. Reference = 10kHz. |
| Output Capacitance | | | 2 | pF | DAC Latches Loaded with all 0s |
| | | | 4 | pF | DAC Latches Loaded with all 1s |
| Digital Feedthrough | | 5 | | nV-s | Feedthrough to DAC output with *SYNC* high and Alternate Loading of all 0s and all 1s. |
| Total Harmonic Distortion | | -85 | | dB | $V_{REF}$ = 6 V rms, All 1s loaded, f = 1kHz |
| | | -85 | | dB | $V_{REF}$ = 5 V, Sinewave generated from digital code. |
| Output Noise Spectral Density | | 25 | | nV/√Hz | @ 1kHz |
| SFDR performance | | 72 | | dB | |
| Intermodulation Distortion | | TBD | | dB | |
| POWER REQUIREMENTS | | | | | |
| Power Supply Range | 2.5 | | 5.5 | V | |
| $I_{DD}$ | | | 10 | µA | Logic Inputs = 0 V or $V_{DD}$ |
| Power Supply Sensitivity[2] | | | 0.001 | %/% | $\Delta V_{DD}$ = ±5% |

NOTES

[1]Temperature range is as follows: B Version: –40°C to +105°C.

[2]Guaranteed by design and characterisation, not subject to production test.

Specifications subject to change without notice.

# Single Supply Operation (Biased Mode)



($V_{DD}$ = 2.5 V to 5.5 V, $V_{REF}$ = + 2V, $I_{OUT}2$ = +1 V. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. DC performance measured with OP1177, AC performance with AD811 unless otherwise noted.)

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| AD5426 | | | | | |
| Resolution | | | 8 | Bits | |
| Relative Accuracy | | | ±0.5 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| AD5432 | | | | | |
| Resolution | | | 10 | Bits | |
| Relative Accuracy | | | ±1 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| AD5443 | | | | | |
| Resolution | | | 12 | Bits | |
| Relative Accuracy | | | ±2 | LSB | |
| Differential Nonlinearity | | | ±1 | LSB | Guaranteed Monotonic |
| Gain Error | | | ±2 | mV | |
| Gain Error Temp Coefficient[2] | | ±5 | | ppm FSR/°C | |
| Output Leakage Current | | | ±10 | nA | Data = $0000_H$, $T_A$ = 25°C, $I_{OUT1}$ |
| | | | ±50 | nA | Data = $0000_H$, $I_{OUT1}$ |
| Output Voltage Compliance Range | | TBD | | V | |
| REFERENCE INPUT[2] | | | | | |
| Reference Input Range | | tbd | | V | |
| $V_{REF}$ Input Resistance | 8 | 10 | 12 | kΩ | Input resistance TC = -50ppm/°C |
| DIGITAL INPUTS/OUTPUT[2] | | | | | |
| Input High Voltage, $V_{IH}$ | 1.7 | | | V | $V_{DD}$ = 2.5 V to 5.5 V |
| Input Low Voltage, $V_{IL}$ | | | 0.8 | V | $V_{DD}$ = 2.7 V to 5.5 V |
| | | | 0.7 | V | $V_{DD}$ = 2.5 V to 2.7 V |
| Input Leakage Current, $I_{IL}$ | | | 1 | µA | |
| Input Capacitance | | | 10 | pF | |
| $V_{DD}$ = 4.5 V to 5.5 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ - 1 | | | V | $I_{SOURCE}$ = 200 µA |
| $V_{DD}$ = 2.5 V to 3.6 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ - 0.5 | | | V | $I_{SOURCE}$ = 200 µA |
| DYNAMIC PERFORMANCE[2] | | | | | |
| Reference Multiplying BW | 10 | | | MHz | $V_{REF}$ = 100 mV rms, DAC loaded all 1s |
| | TBD | | | MHz | $V_{REF}$ = 1 V, DAC loaded all 1s |
| Output Voltage Settling Time | | | | | |
| AD5426 | | 30 | TBD | ns | Measured to ½ LSB. $R_{LOAD}$ = 100Ω, $C_{LOAD}$ = 15pF. |
| AD5432 | | 35 | TBD | ns | $V_{REF}$ = 0V,DAC latch alternately loaded with 0s & 1s. |
| AD5443 | | 40 | TBD | ns | |
| Slew Rate | | 100 | | V/µs | |
| Digital to Analog Glitch Impulse | | 3 | | nV-s | 1 LSB change around Major Carry |
| Multiplying Feedthrough Error | | | -75 | dB | DAC latch loaded with all 0s. Reference = 10kHz. |
| Output Capacitance | | | 2 | pF | DAC Latches Loaded with all 0s |
| | | | 4 | pF | DAC Latches Loaded with all 1s |
| Digital Feedthrough | | 5 | | nV-s | Feedthrough to DAC output with *SYNC* high and Alternate Loading of all 0s and all 1s. |
| Total Harmonic Distortion | | -85 | | dB | $V_{REF}$ = 2 Vp-p, 1V Bias, All 1s loaded, f = 1kHz |
| | | -85 | | dB | $V_{REF}$ = 2 V, Sinewave generated from digital code. |
| Output Noise Spectral Density | | 25 | | nV/√Hz | @ 1kHz |
| SFDR performance | | 72 | | dB | |
| Intermodulation Distortion | | TBD | | dB | |
| POWER REQUIREMENTS | | | | | |
| Power Supply Range | 2.5 | | 5.5 | V | |
| $I_{DD}$ | | | 10 | µA | Logic Inputs = 0 V or $V_{DD}$ |
| Power Supply Sensitivity[2] | | | 0.001 | %/% | $\Delta V_{DD}$ = ±5% |

NOTES

[1]Temperature range is as follows: B Version: –40°C to +105°C.

[2]Guaranteed by design and characterisation, not subject to production test.

Specifications subject to change without notice.

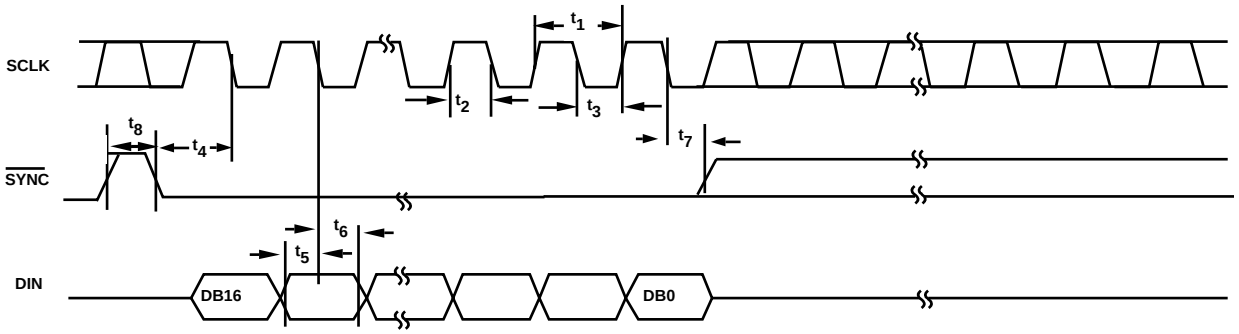
# AD5426/AD5432/AD5443–SPECIFICATIONS[1]

## TIMING CHARACTERISTICS[1] ($V_{DD}$ = 2.5 V to 5.5 V, $V_{REF}$ = +5 V, $I_{OUT}2$ = 0 V. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Units | Conditions/Comments |
|---|---|---|---|
| $f_{SCLK}$ | 50 | MHz max | Max Clock frequency |
| $t_1$ | 20 | ns min | SCLK Cycle time |
| $t_2$ | 8 | ns min | SCLK High Time |
| $t_3$ | 8 | ns min | SCLK Low Time |
| $t_4$[2] | 13 | ns min | *SYNC* falling edge to SCLK active edge setup time |
| $t_5$ | 5 | ns min | Data Setup Time |
| $t_6$ | 4.5 | ns min | Data Hold Time |
| $t_7$ | 5 | ns min | *SYNC* rising edge to SCLK active edge |
| $t_8$ | 30 | ns min | Minimum *SYNC* high time |
| $t_9$[3] | 25 | ns min | SCLK Active edge to SDO valid |

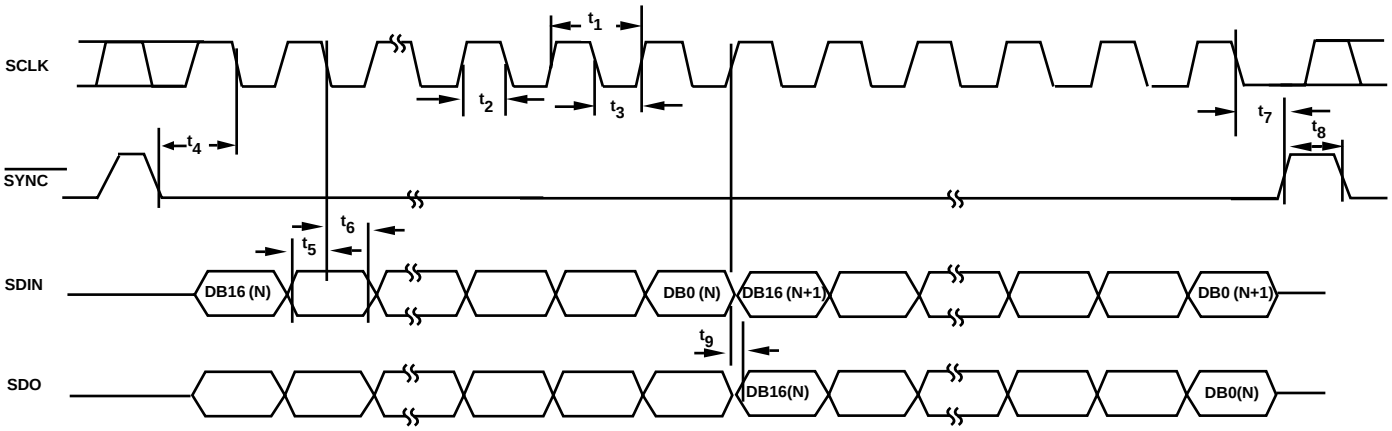
NOTES
[1]See Figures 1 & 2. Temperature range is as follows: B Version: –40°C to +105°C. Guaranteed by design and characterisation, not subject to production test. All input signals are specified with tr =tf = 5ns (10% to 90% of $V_{DD}$) and timed from a voltage level of ($V_{IL}$ + $V_{IH}$)/2.
[2]Falling or Rising edge as determined by control bits of Serial word.
[3]Daisychain and Readback modes cannot operate at max clock frequency. SDO timing specifications measured with load circuit as shown in Figure 3.

Specifications subject to change without notice.




ALTERNATIVELY, DATA MAY BE CLOCKED INTO INPUT SHIFT REGISTER ON RISING EDGE OF SCLK AS DETERMINED BY CONTROL BITS. TIMING AS PER ABOVE, WITH SCLK INVERTED.

*Figure 1. Stand Alone Mode Timing Diagram.*




ALTERNATIVELY, DATA MAY BE CLOCKED INTO INPUT SHIFT REGISTER ON RISING EDGE OF SCLK AS DETERMINED BY CONTROL BITS. IN THIS CASE, DATA WOULD BE CLOCKED OUT OF SDO ON FALLING EDGE OF SCLK. TIMING AS PER ABOVE, WITH SCLK INVERTED.

*Figure 2. Daisy Chain and Readback Modes Timing Diagram*

**ABSOLUTE MAXIMUM RATINGS**[1, 2]

($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{DD}$ to GND | –0.3 V to +7 V |
| $V_{REF}$, $R_{FB}$ to GND | –12 V to +12 V |
| $I_{OUT}1$, $I_{OUT}2$ to GND | –0.3 V to +7 V |
| Input Current to any pin except supplies | ±10 mA |
| Logic Inputs & Output[3] | -0.3V to $V_{DD}$ +0.3 V |
| Operating Temperature Range | |
| Industrial (B Version) | –40°C to +105°C |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | +150°C |
| 10 lead µSOIC $\theta_{JA}$ Thermal Impedance | 206°C/W |
| Lead Temperature, Soldering (10seconds) | 300°C |
| IR Reflow, Peak Temperature (<20 seconds) | +235°C |

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Transient currents of up to 100mA will not cause SCR latchup.

[3]Overvoltages at SCLK, *SYNC*, DIN, will be clamped by internal diodes. Current should be limited to the maximum ratings given.

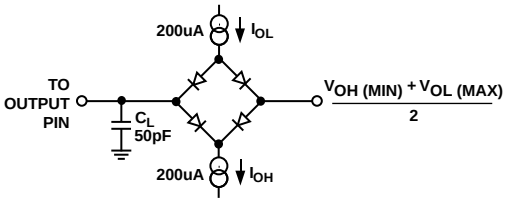



*Figure 3. Load Circuit for SDO Timing Specifications*

**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Branding | Package Option |
|---|---|---|---|---|
| AD5426BRM | -40 °C to +105 °C | µSOIC | D01 | RM-10 |
| AD5432BRM | -40 °C to +105 °C | µSOIC | D02 | RM-10 |
| AD5443BRM | -40 °C to +105 °C | µSOIC | D03 | RM-10 |

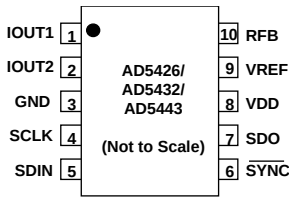
**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5426/AD5432/AD5443 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**PIN FUNCTION DESCRIPTION**

| Pin | Mnemonic | Function |
|---|---|---|
| 1 | $I_{OUT}1$ | DAC Current Output. |
| 2 | $I_{OUT}2$ | DAC Analog Ground. This pin should normally be tied to the analog ground of the system. |
| 3 | GND | Ground Pin. |
| 4 | SCLK | Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK. |
| 5 | SDIN | Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to rising edge. |
| 6 | *SYNC* | Active Low Control Input. This is the frame synchronization signal for the input data. When *SYNC* goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks. In stand alone mode, the serial interface counts clocks and data is latched to the shift register on the 16th active clock edge. |
| 7 | SDO | Serial Data Output. This allows a number of parts to be daisychained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data will always be clocked out on the alternate edge to loading data to the shift register. Writing the Readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge. |
| 8 | $V_{DD}$ | Positive power supply input. These parts can be operated from a supply of +2.5 V to +5.5 V. |
| 9 | $V_{REF}$ | DAC reference voltage input pin. |
| 10 | $R_{FB}$ | DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output. |

**PIN CONFIGURATION**
**µSOIC**



## TERMINOLOGY

**Relative Accuracy**
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

**Differential Nonlinearity**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

**Gain Error**
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is $V_{REF}$ – 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

**Output Leakage Current**
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the $I_{OUT1}$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT1}$ current. Minimum current will flow in the $I_{OUT2}$ line when the DAC is loaded with all 1s

**Output Capacitance**
Capacitance from $I_{OUT1}$ or $I_{OUT2}$ to AGND.

**Output Current Settling Time**
This is the amount of time it takes for the output to settle to a specified level for a full scale input change. For these devices, it is specifed with a 100 Ω resistor to ground.

**Digital to Analog Glitch Impulse**
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

**Digital Feedthrough**
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the $I_{OUT}$ pins and subsequently into the following circuitry. This noise is digital feedthrough.

**Multiplying Feedthrough Error**
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT1}$ terminal, when all 0s are loaded to the DAC.

**Harmonic Distortion**
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonices are included, such as second to fifth.

$$THD = 20\log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}$$

**Intermodulation Distortion**
The DAC is driven by two combinded sine waves references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa±nfb where m, n = 0, 1, 2, 3... Intermodulation terms are those for which m or n is not equal to zero. The second order terms include (fa +fb) and (fa - fb) and the third order terms are (2fa + fb), (2fa -fb), (f+2fa + 2fb) and (fa - 2fb). IMD is defined as

$$IMD = 20\log \frac{\text{(rms sum of the sum and diff distortion products)}}{\text{rms amplitude of the fundamental}}$$

**Compliance Voltage Range**
The maximum range of (output) terminal voltage for which the device will provide the specified characteristics.

## GENERAL DESCRIPTION

### DAC SECTION

The AD5426, AD5432 and AD5443 are 8, 10 and 12 bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-Bit AD54246 is shown in Figure 4. The feedback resistor $R_{FB}$ has a value of R. The value of R is typically 10kΩ (minimum 8kΩ and maximum 12kΩ). If $I_{OUT1}$ and $I_{OUT2}$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at $V_{REF}$ is always constant.

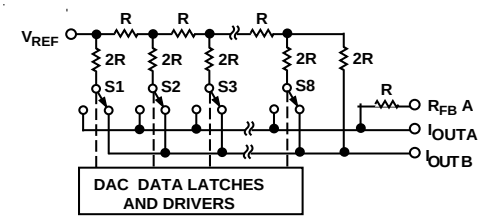



*Figure 4. Simplified Ladder*

Access is provided to the $V_{REF}$, $R_{FB}$, $I_{OUT1}$ and $I_{OUT2}$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, bipolar output or in single supply modes of operation. in unipolar mode or four quadrant multiplication in bipolar mode.

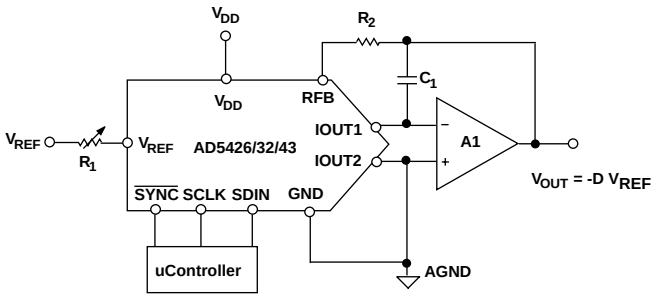
**Unipolar Mode**
Using a single op amp, these devices can easily be configured to provide 2 quadrant multiplying operation or a unipolar output voltage swing as shown in Figure 5.

When an output amplifier is connected in unipolar mode, the output voltage is given by:

$$V_{OUT} = -D \times V_{REF}$$

Where D is the fractional representation of the digital word loaded to the DAC.

D = 0 to 256 (8-Bit AD5426)
= 0 to 1024 (10-Bit AD5432)
= 0 to 4096 (12-Bit AD5443)




NOTES:
[1]R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
[2]C1 PHASE COMPENSATION (10pF-15pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

*Figure 5. Unipolar Operation*

With a fixed 10 V reference, the circuit shown above will give an unipolar 0V to -10V output voltage swing. When $V_{IN}$ is an ac signal, the circuit performs two-quadrant multiplication.

The following table shows the relationship between digital code and expected output voltage for unipolar operation. (AD5426, 8-Bit device).

**Table I. Unipolar Code Table**

| Digital Input | Analog Output (V) |
|---|---|
| 1111 1111 | $-V_{REF}$ (255/256) |
| 1000 0000 | $-V_{REF}$ (128/256) = $-V_{REF}/2$ |
| 0000 0001 | $-V_{REF}$ (1/256) |
| 0000 0000 | $-V_{REF}$ (0/256) = 0 |

**Bipolar Operation**
In some applications, it may be necessary to generate full 4-Quadrant multplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors as shown in Figure 6.

When $V_{IN}$ is an ac signal, the circuit performs four-quadrant multiplication.

Table II. shows the relationship between digital code and the expected output voltage for bipolar operation (AD5426, 8-Bit device).

**Table II. Bipolar Code Table**

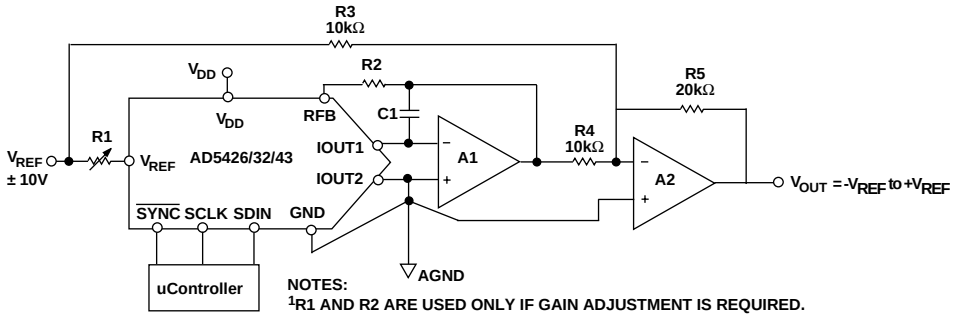
| Digital Input | Analog Output (V) |
|---|---|
| 1111 1111 | $+V_{REF}$ (127/128) |
| 1000 0000 | 0 |
| 0000 0001 | $-V_{REF}$ (127/128) |
| 0000 0000 | $-V_{REF}$ (128/128) |

**SERIAL INTERFACE**

The AD5426/AD5432/AD5443 have an easy to use 3-wire interface which is compatible with SPI/QSPI/MicroWire and DSP interface standards. Data is written to the device in 16 bit words. This 16-bit word consists of 4 control bits and either 8, 10 or 12 data bits as shown in Figure 6.The AD5443 uses all 12 bits of DAC data. The AD5432 uses ten bits and ignores the two LSBs, while the AD5443 uses eight bits and ignores the last four bits. As good programming practice, these ignored LSB's should be set to '0'.

**Low Power Serial Interface**
To minimize the power consumption of the device, the interface only powers up fully when the device is being written to, i.e., on the falling edge of *SYNC*. The SCLK and DIN input buffers are powered down on the rising edge of *SYNC*.

**DAC Control Bits C3 - C0**
Control bits C3 to C0 allow control of various functions of the DAC as can be seen in Table 3. Default settings of the DAC on power on are as follows :
Data clocked into shift register on falling clock edges;
Daisy chain mode is enabled. Device powers on with zeroscale load to the DAC register and $I_{OUT}$ lines.
The DAC control bits allow the user to adjust certain features on power on, for example, Daisy chaining may be disabled if not in use, active clock edge may be changed to rising edge and DAC output may be cleared to either zero




NOTES:
[1]R1 AND R2 ARE USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR $V_{OUT}$ = 0V WITH CODE 10000000 LOADED TO DAC.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R3 AND R4.
[3]C1 PHASE COMPENSATION (10pF-15pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER.

*Figure 6. Bipolar Operation (4 Quadrant Multiplication)*

or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

**TABLE 3. DAC CONTROL BITS**

| C3 | C2 | C1 | C0 | Funtion Implemented |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No Operation (Power On Default) |
| 0 | 0 | 0 | 1 | Load and Update |
| 0 | 0 | 1 | 0 | Initiate Readback |
| 0 | 0 | 1 | 1 | Reserved |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Reserved |
| 1 | 0 | 0 | 1 | Daisy Chain Disable |
| 1 | 0 | 1 | 0 | Clock Data to shift register On Rising Edge |
| 1 | 0 | 1 | 1 | Clear DAC output to Zero |
| 1 | 1 | 0 | 0 | Clear DAC output to Midscale |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

### *SYNC* Function

*SYNC* is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while *SYNC* is low. To start the serial data transfer, *SYNC* should be taken low observing the minimum *SYNC* falling to SCLK falling edge setup time, $t_4$.

### Daisy Chain Mode

Daisy Chain is the default power on mode. To disable the daisy chain function, write "1001" to control word. In Daisy-Chain Mode the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when *SYNC* is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK (this is the default, use the control word to change the active edge) and is valid for the next device on the falling edge (default). By connecting this line to the DIN input on the next device in the chain, a multidevice interface is constructed. 16 clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. See the timing diagram in Figure 3.

When the serial transfer to all devices is complete, *SYNC* should be taken high. This prevents any further data being clocked into the input shift register. A burst clock containing the exact number of clock cycles may be used and *SYNC* taken high some time later. After the rising edge of *SYNC*, data is automatically transferred from each device's input shift register to the addressed DAC. When control bits = "0000", the device is in No Operation mode. This may be useful in daisy-chain applications where the user does not wish to change the settings of a particular DAC in the chain. Simply write "0000" to the Control bits for that DAC and the following data bits will be ignored.

### Stand alone Mode

After power on, write "1001" to control word to disable Daisy Chain Mode. The first falling edge of *SYNC* resets a counter that counts the number of serial clocks to ensure the correct number of bits are shited in and out of the serial shift registers. Any further edges on *SYNC* are ignored until the correct number of bits are shifted in or out.

After the falling edge of the 16th SCLK pulse, data will automatically be transferred from the input shift register to the DAC. In order for another serial transfer to take place the counter must be reset by the falling edge of *SYNC*.

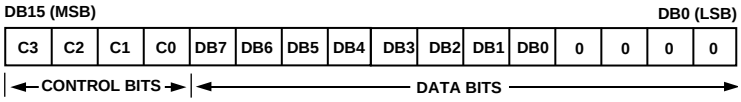



*Figure 6a. AD5426 8 bit Input Shift Register Contents*

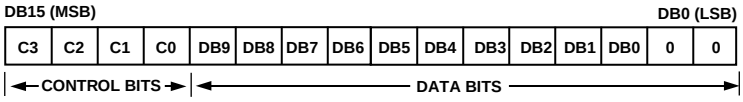



*Figure 6b. AD5432 10 bit Input Shift Register Contents*

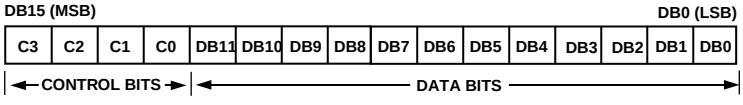



*Figure 6c. AD5443 12 bit Input Shift Register Contents*

**Overview of AD54xx devices**

| Part No | Resolution | #DACs | INL | Settling Time | Interface | Package | Features |
|---|---|---|---|---|---|---|---|
| AD5424 | 8 | 1 | ±0.5 | 20ns | Parallel | RU-16, CP-20 | 10 MHz, 10 ns *CS* Pulse Width |
| AD5425 | 8 | 1 | ±0.5 | 20ns | Serial | RM-10 | Byte Load,10 MHz BW, 50 MHz Serial |
| AD5426 | 8 | 1 | ±0.5 | 20ns | Serial | RM-10 | 10 MHz BW, 50 MHz Serial |
| AD5432 | 10 | 1 | ±1 | 25ns | Serial | RM-10 | 10 MHz BW, 50 MHz Serial |
| AD5433 | 10 | 1 | ±1 | 25ns | Parallel | RU-20, CP-20 | 10 MHz, 10 ns *CS* Pulse Width |
| AD5443 | 12 | 1 | ±2 | 30ns | Serial | RM-10 | 10 MHz BW, 50 MHz Serial |
| AD5445 | 12 | 1 | ±2 | 30ns | Parallel | RU-20, CP-20 | 10 MHz, 10 ns CS Pulse Width |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**10 Lead µSOIC**
**(RM-10)**