AN6080FHN

Modulator IC for CDMA system cellular telephone

■ Overview

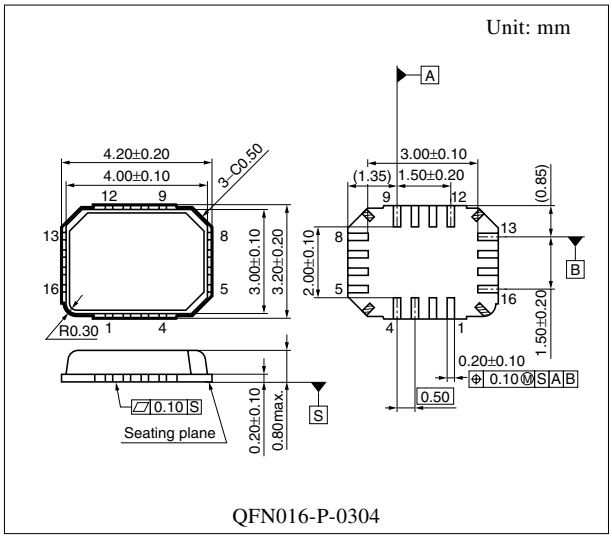
The AN6080FHN is a modulator IC for a cellular telephone, integrating a quadrature modulator for transmitting of CDMA system for the domestic market and a gain control amplifier on a single chip.

■ Features

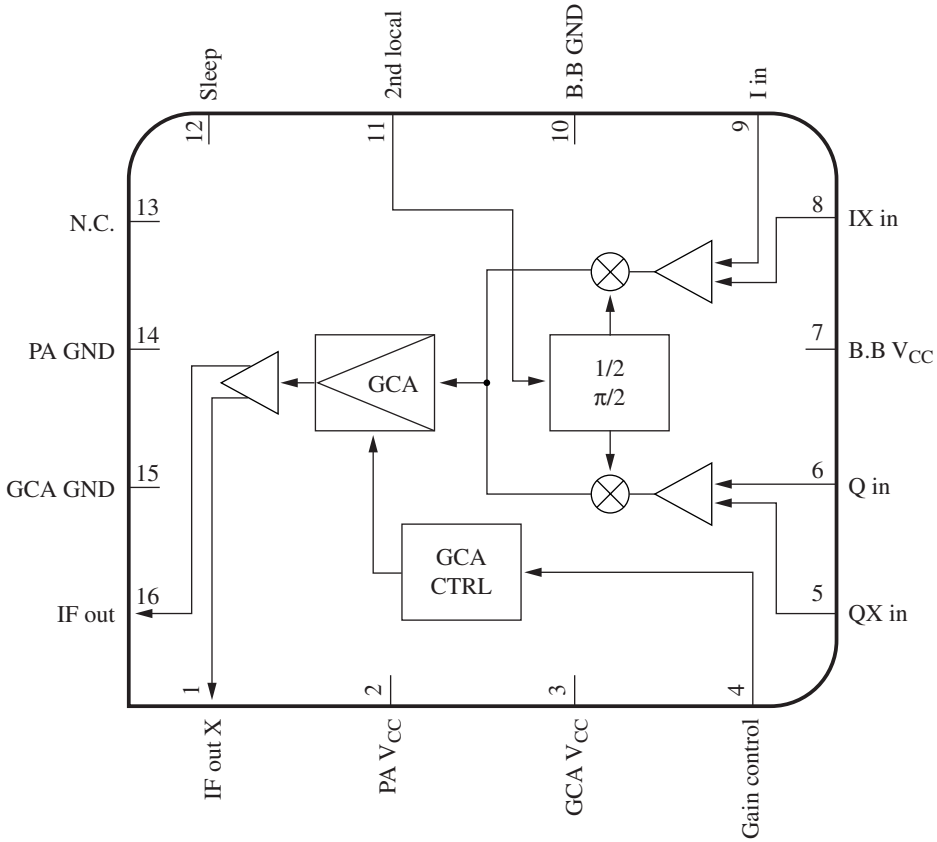
- Current consumption: 26 mA typ.
- Wide output power control range: −8 dBm to −90 dBm
- Good linearity of output power and control voltage
- Small temperature dependency: ±3 dB

■ Applications

- Cellular telephone (CDMA system)



■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Signal output (−)	9	I input
2	Power supply (output)	10	GND (base band)
3	Power supply (GCA)	11	Local signal input
4	Gain adjustment	12	Sleep mode changeover
5	$\overline{Q}$ input	13	N.C.
6	Q input	14	GND (GCA)
7	Power supply (base band)	15	GND (output)
8	$\overline{I}$ input	16	Signal output (+)

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.2	V
Supply current	I_{CC}	40	mA
Power dissipation *2	P_D	100	mW
Operating ambient temperature *1	T_{opr}	−30 to +85	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2: P_D is the value at T_a = 85°C without a heatsink. Use this device within the range of allowable power dissipation referring to "■ Technical Data • P_D — T_a curves of QFN016-P-0304".

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	2.55 to 4.00	V

■ Electrical Characteristics at T_a = 25°C

Unless otherwise specified, V_{CC} = 2.8 V, V_{SLP} = 2.8 V, SW1 = a (refer to "■ Application Circuit Examples"), V_{LO} = −7.5 dBm: f = 333.7 MHz, V_I , V_{IX} , V_Q , V_{QX} (DC operating point voltage for each input) = 1.5 V, input signal is 700 kHz sine wave, amplitude 900 mV[p-p] (single phase), phase I: 0°, IX: 180°, Q: 90° and QX: 270°.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current consumption	I_{TOT}	No input	17	26	33	mA
Current consumption (sleep)	I_{SLP}	No input, SW1 = b Refer to "■ Application Circuit Examples"	—	0	10	µA
Output level 1	$P_{O(1)}$	V_{GC} = 1.85 V IQ input is OQPSK (based on IS-95)	−13	−11	—	dBm
Output level 2	$P_{O(2)}$	V_{GC} = 1.3 V IQ input is OQPSK (based on IS-95)	−47	−42	−37	dBm
Output level 3	$P_{O(3)}$	V_{GC} = 0.5 V IQ input is OQPSK (based on IS-95)	—	−90	−83	dBm

■ Electrical Characteristics at T_a = 25°C (continued)

Unless otherwise specified, V_{CC} = 2.8 V, V_{SLP} = 2.8 V, SW1 = a (refer to "■ Application Circuit Examples"), V_{LO} = −7.5 dBm: f = 333.7 MHz, V_I , V_{IX} , V_Q , V_{QX} (DC operating point voltage for each input) = 1.5 V, input signal is 700 kHz sine wave, amplitude 900 mV[p-p] (single phase), phase I: 0°, IX: 180°, Q: 90° and QX: 270°.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output level dependency on supply voltage	dP_O	V_{GC} = 1.85 V, output level variation from V_{CC} = 2.7 V to 2.9 V	−1.2	0	1.2	dB
In-band output deviation	ΔP_O	Level deviation at output over 1.23 MHz inband	− 0.5	0	0.5	dB
Carrier leak 1	ΔCL1	V_{GC} = 1.8 V, IQ input operating point (DC) is no adjustment	—	−35	−25	dBc
Image leak 1	ΔIL1	V_{GC} = 1.8 V, IQ input operating point (DC) is no adjustment	—	−35	−25	dBc
Gain adjustment sensitivity	β_{GCA}	Gain variation amount from V_{GC} = 0.5 V to 1.85 V	55	60	65	dB/V
Gain variation range	ΔG	Gain variation amount from V_{GC} = 0.5 V to 1.85 V	73	80	—	dB
Local signal input level	V_{LO}		−17	−7.5	−4	dBm
Sleep control (low)	$V_{SLP(1)}$	Voltage when I_{TOT} becomes 10 µA or less	—	—	0.2	V
Sleep control (high)	$V_{SLP(2)}$	Voltage at which IC comes to operate	2.3	—	—	V
Gain adjustment voltage	V_{GC}		0.1	—	2.6	V

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Carrier leak 2	ΔCL2	V_{GC} = 1.8 V, −20°C to 90°C, When IQ input operating point (DC) is adjusted, adjustment range is within ±15 mV	—	−35	−30	dBc
Image leak 2	ΔIL2	V_{GC} = 1.8 V, −20°C to 90°C, When IQ input operating point (DC) is adjusted, adjustment range is within ±15 mV	—	−35	−25	dBc
Adjacent channel leak power suppression 1 (900 kHz detuning)	ACP(1)	Input is OQPSK (based on IS-95) at −13.5 dBm output (single phase) and −20°C to 90°C	—	−58	−50	dBc
Adjacent channel leak power suppression 2 (1.98 MHz detuning)	ACP(2)	Input is OQPSK (based on IS-95) at −13.5 dBm output (single phase) and −20°C to 90°C	—	−66	−60	dBc
In-band noise 1	N(1)	Noise level in center frequency ±630 kHz at −28 dBm output(single phase) and −20°C to 90°C	—	−141	−135	dBm/Hz
In-band noise 2	N(2)	Noise level in center frequency ±630 kHz at −76.5 dBm output(single phase) and −20°C to 90°C	—	−165	−160	dBm/Hz

■ Electrical Characteristics at T_a = 25°C (continued)

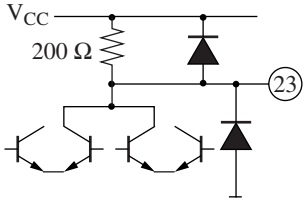
Unless otherwise specified, V_{CC} = 2.8 V, V_{SLP} = 2.8 V, SW1 = a (refer to "■ Application Circuit Examples"), V_{LO} = −7.5 dBm: f = 333.7 MHz, V_I , V_{IX} , V_Q , V_{QX} (DC operating point voltage for each input) = 1.5 V, input signal is 700 kHz sine wave, amplitude 900 mV[p-p] (single phase), phase I: 0°, IX: 180°, Q: 90° and QX: 270°.

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

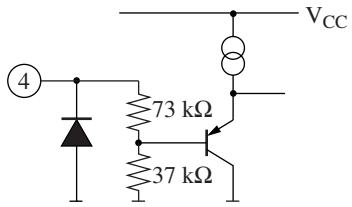
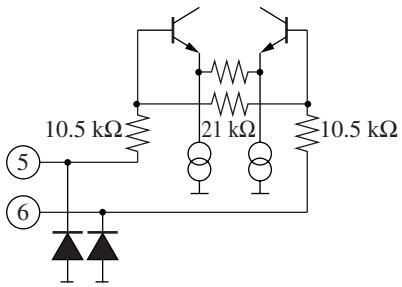
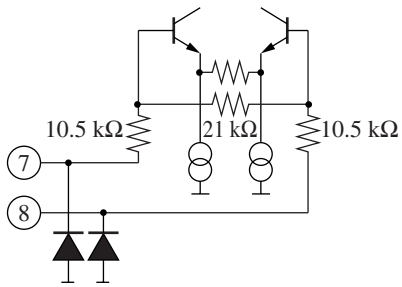
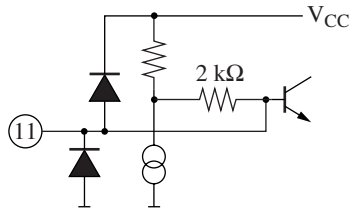
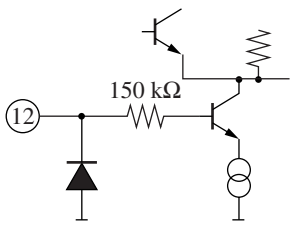
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain deviation	ΔGerr	Output level deviation at 27°C as reference, −20°C to 90°C, V_{GC} = 0.5 V to 1.85 V	−3	0	+3	dB
Rise time 1	t_{r1}	Time so as to get 90% or more output when V_{CC} , V_{SLP} are from 0 V to 2.8 V	—	50	100	µs
Rise time 2	t_{r2}	V_{CC} is fixed at 2.8 V Time so as to get 90% or more output when V_{SLP} are from 0 V to 2.8 V	—	30	80	µs
Fall time 1	t_{d1}	Time so as to get 10% or less output when V_{CC} , V_{SLP} are from 2.8V to 0V	—	20	70	µs
Fall time 2	t_{d2}	V_{CC} is fixed at 2.8 V Time so as to get 10% or less output when V_{SLP} are from 2.8 V to 0 V	—	50	100	µs
Gain adjustment pin Input impedance	Z_{GC}	Impedance between pin 4 and GND	65	110	—	kΩ
IQ input pin Input impedance	Z_{IQ}	Impedance between each pin of pin 5, pin 6, pin 8 and 9 pin and GND	15	21	—	kΩ
Output level 4	$P_{O(4)}$	V_{GC} = 1.85 V Single phase output level at pin 16 IQ input is OQPSK (based on IS-95)	−10	−8	—	dBm
Output level 5	$P_{O(5)}$	V_{GC} = 1.3 V Single phase output level at pin 16 IQ input is OQPSK (based on IS-95)	−44	−39	−34	dBm
Output level 6	$P_{O(6)}$	V_{GC} = 0.5 V Single phase output level at pin 16 IQ input is OQPSK (based on IS-95)	—	−87	−80	dBm

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	DC voltage (V)
1		Signal output (−): Output pin (reverse) of IF signal.	—
2	—	Power supply (output): Power supply pin of output amplifier.	—

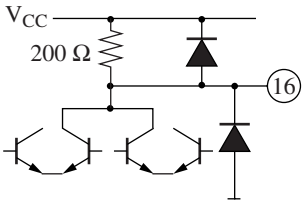
Note) The characteristics listed above are theoretical values based on the IC design and are not guaranteed.

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC voltage (V)
3	—	Power supply (GCA): Power supply pin of GCA system.	—
4		Gain adjustment : Adjust the gain. The voltage from 0 V to supply voltage can be applied.	0
5, 6		Pin 5: $\overline{Q}$ input; Pin 6: Q input: Pin to input the Q signal (differential). Apply DC bias voltage (1.5 V) to each pin.	—
7	—	Power supply (base band): Supply voltage pin of base band system.	—
8, 9		Pin 8: $\overline{I}$ input; Pin 9: I input: Pin to input the I signal (differential). Apply DC bias voltage (1.5 V) to each pin.	—
10	—	GND (base band): Ground pin of base band system.	—
11		Local signal input: Input pin of local signal for IQ modulation.	2.7
12		Sleep: Operating mode: Connect this pin to supply voltage pin. Sleep mode: Connect to GND.	—

Note) The characteristics listed above are theoretical values based on the IC design and are not guaranteed.

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	DC voltage (V)
13	—	N.C.	—
14	—	GND (GCA): Ground pin of GCA system.	—
15	—	GND (output): Ground pin of output amplifier.	—
16		Signal output (+): Output pin of IF signal.	—

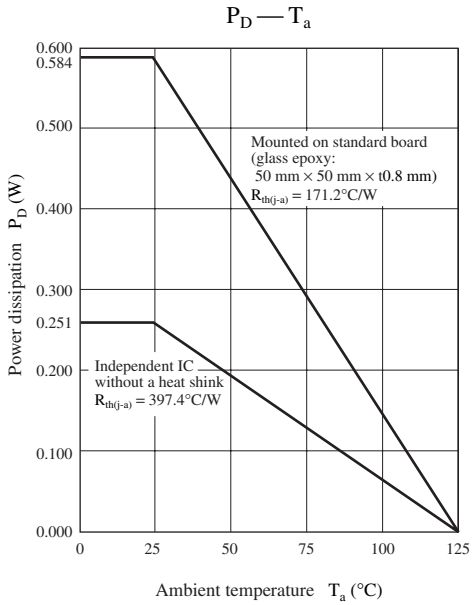
Note) The characteristics listed above are theoretical values based on the IC design and are not guaranteed.

■ Usage Note

There are three systems (pin 2, pin 3 and pin 7) of supply voltage pins in this product. Apply the same voltage at the same time to these three pins on use. (When power supply is switched to on or off, it must be done at the same time for these three pins. Never use with off for any pins.)

■ Technical Data

1. P_D — T_a curves of QFN016-P-0304



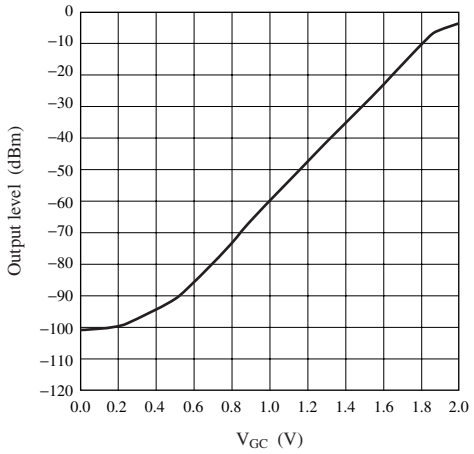
■ Technical Data (continued)

2. Main characteristics

(Gain control characteristics in the "■ Application Circuit Example 1. Bi-phase output circuit")

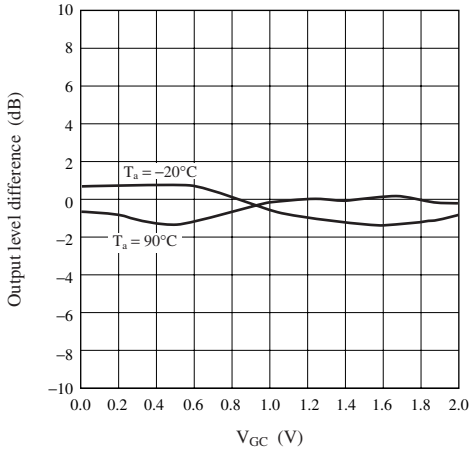
Output level — GC characteristics

(T_a = −20°C, 27°C, 90°C)



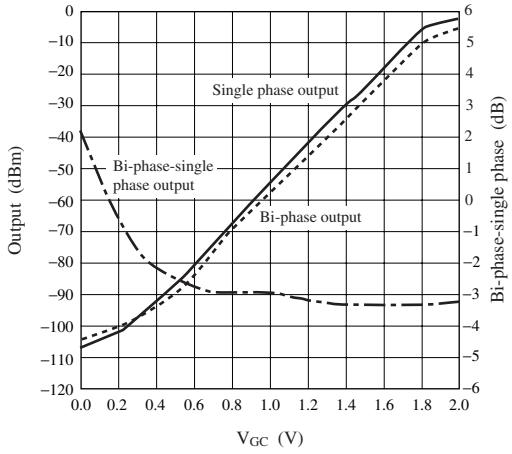
Output level — GC temperature characteristics

(27°C as reference)

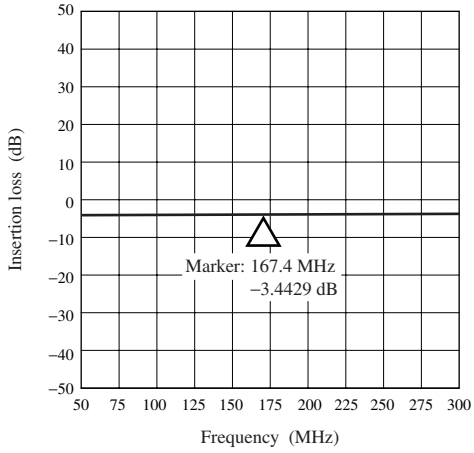


Output level — GC characteristic

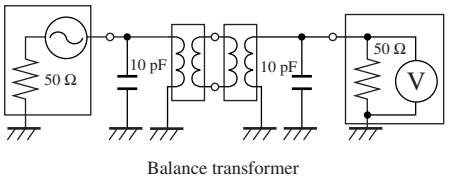
(Bi-phase — single phase output)



Balance transformer insertion loss (S21)

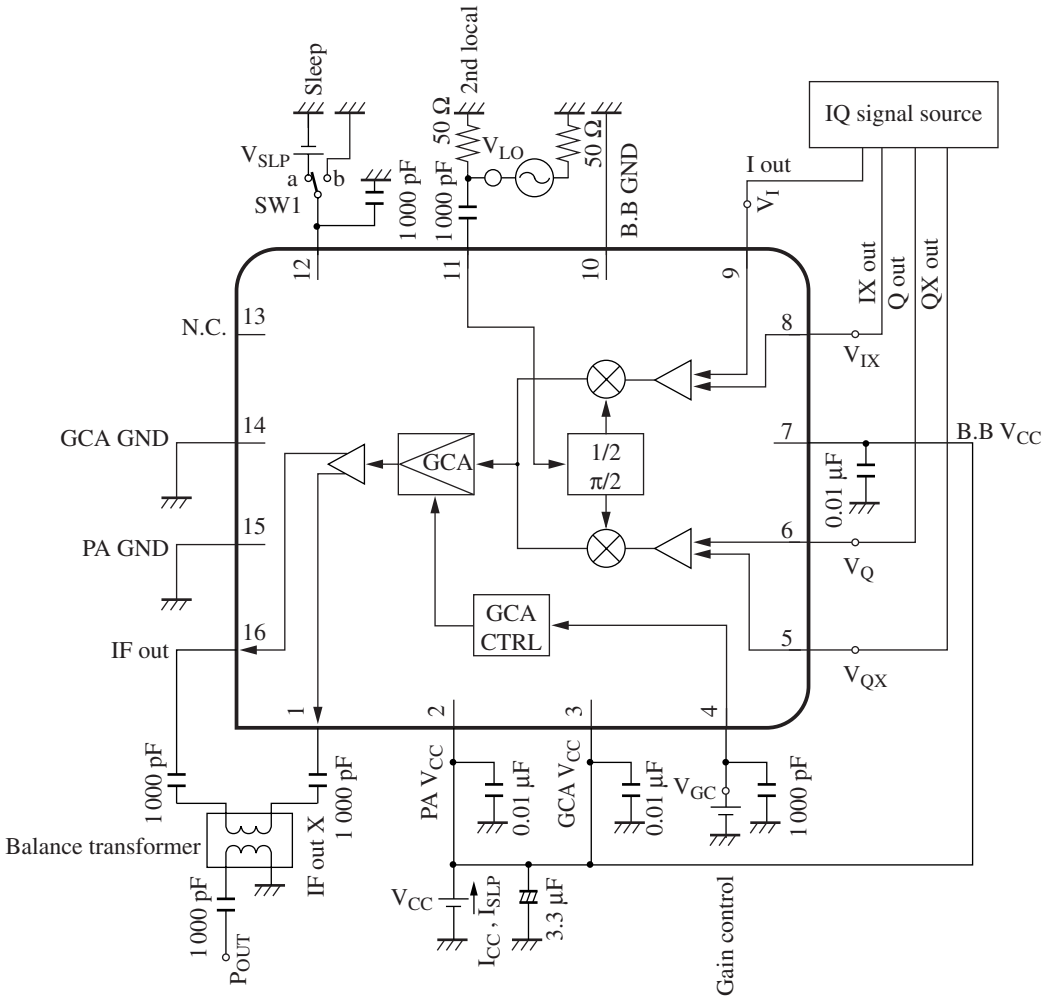


[Balance transformer insertion loss measuring circuit]



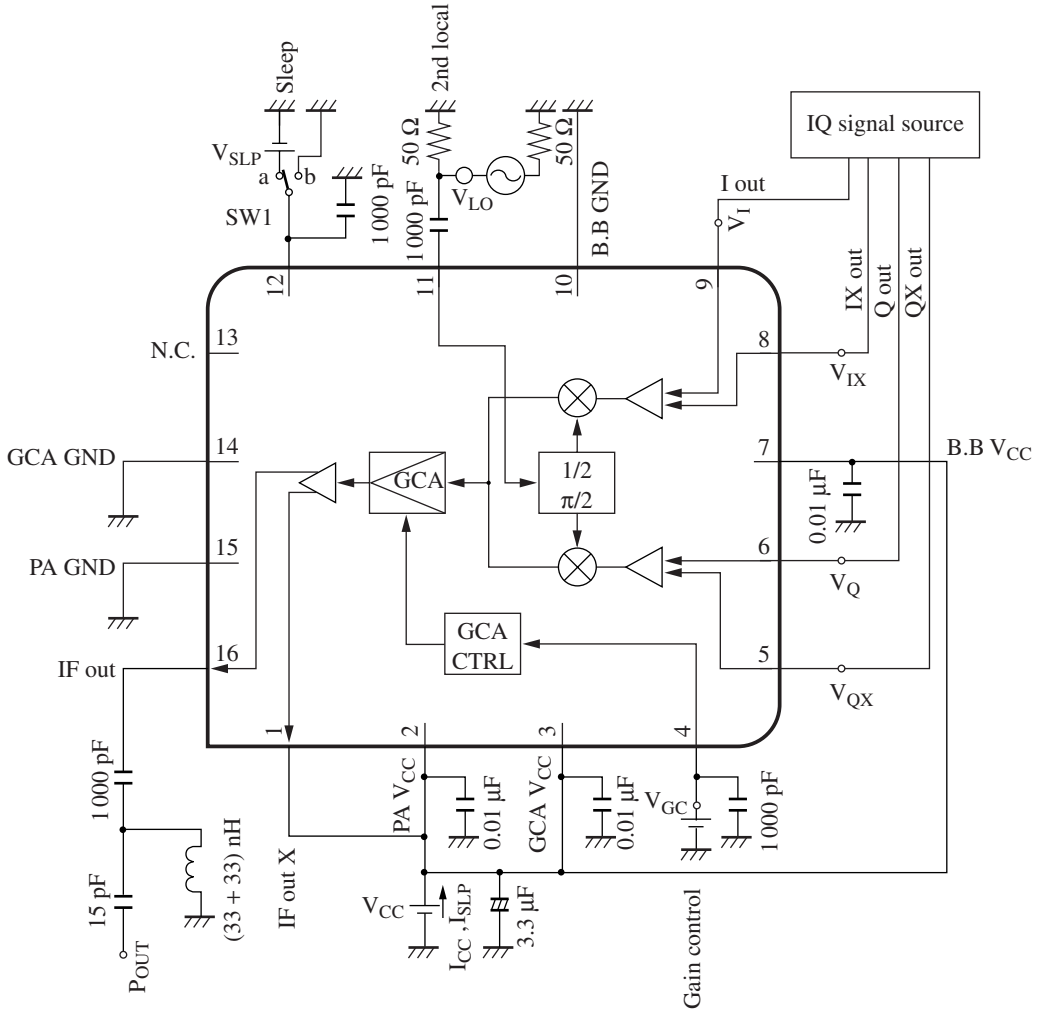
■ Application Circuit Examples

1. Bi-phase output circuit



■ Application Circuit Examples (continued)

2. Single phase output circuit



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