

STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT SERIES Voltage Detector IC

TYPE **BD48XXFVE Series**

- FEATURES
- Detection voltage lineup : 2.3V~6.0V
 - High precision detection voltage: $\pm 1.0\%$

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|-----------------------------------------|----------------------|----------------|------|
| Supply Voltage ※1 | V _{DD} -GND | -0.3 to +10 | V |
| Output Voltage ※1 Nch Open Drain Output | V _{OUT} | GND-0.3 to +10 | V |
| Power Dissipation ※2 | P _d | 210 | mW |
| Operating Temperature Range ※1 | T _{opr} | -40 to +105 | °C |
| Storage Temperature Range | T _{stg} | -55 to +125 | °C |

※1 Do not exceed P_d.

※2 Mounted on 70mm × 70mm × 1.6mm Glass Epoxy PCB, P_d derated at 2.1mW/°C for temperature above Ta=25°C

NOTE : The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

NOTE : This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

OELECTRICAL CHARACTERISTICS (Unless Otherwise Specified Ta=-40 to 105°C)

| Parameter | Symbol | Condition | Limit | | | Unit | |
|-------------------------------------------|--------|-------------------------------------------|-----------------|-----------|-----------------|--------|-----|
| | | | Min. | Typ. | Max. | | |
| Detection Voltage | Vs | RL=470kΩ, VDD=H→L ※3 | Vs(T) × 0.99 | Vs(T) | Vs(T) × 1.01 | V | |
| Output Delay Time "L→H" | tPLH | CL=100pF RL=100kΩ Vout=GND→50% ※4 | - | - | 100 | μ sec | |
| Circuit Current when ON | Icc1 | VDD=Vs-0.2V, ※3 | Vs=2.3-3.1V | - | 0.51 | 1.53 | μ A |
| | | | Vs=3.2-4.2V | - | 0.56 | 1.68 | |
| | | | Vs=4.3-5.2V | - | 0.60 | 1.80 | |
| | | | Vs=5.3-6.0V | - | 0.66 | 1.98 | |
| Circuit Current when OFF | Icc2 | VDD=Vs+2.0V, ※3 | Vs=2.3-3.1V | - | 0.75 | 2.25 | μ A |
| | | | Vs=3.2-4.2V | - | 0.80 | 2.40 | |
| | | | Vs=4.3-5.2V | - | 0.85 | 2.55 | |
| | | | Vs=5.3-6.0V | - | 0.90 | 2.70 | |
| Minimum Operating Voltage | VOPL | VOL≤0.4V, RL=470kΩ, Ta=-25~-105°C | 0.95 | - | - | V | |
| | | VOL≤0.4V, RL=470kΩ, Ta=-40~-25°C | 1.20 | - | - | | |
| 'Low'Output Current (Nch) | IoL | VDS=0.5V, VDD=1.5V, Vs=2.3-6.0V | 0.4 | 1.0 | - | mA | |
| | | VDS=0.5V, VDD=2.4V, Vs=2.7-6.0V | 2.0 | 4.0 | - | | |
| Leak Current when OFF | Ileak | VDD=VDS=10V ※3 | - | - | 0.1 | μ A | |
| Detection Voltage Temperature coefficient | Vs/ΔT | Ta=-40°C to 105°C (Designed Guarantee) | - | ± 100 | ± 360 | ppm/°C | |
| Hysteresis Voltage | ΔVs | VDD=L→H→L | Vs × 0.03 | Vs × 0.05 | Vs × 0.08 | V | |

Vs(T) : Standard Detection Voltage (2.3V to 6.0V, 0.1V step)

RL: Pull-up resistor to be connected between VOUT and power supply.

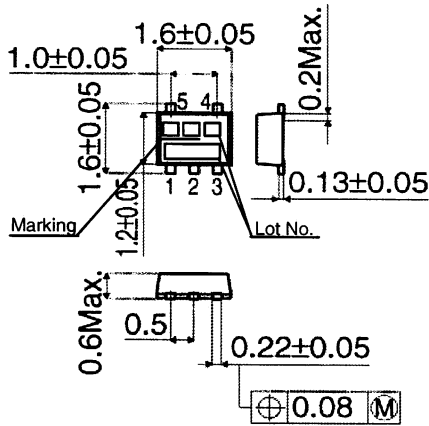
CL: Capacitor to be connected between VOUT and GND.

Designed Guarantee.(Outgoing inspection is not done on all products.)

※3 Guarantee is Ta=25°C.

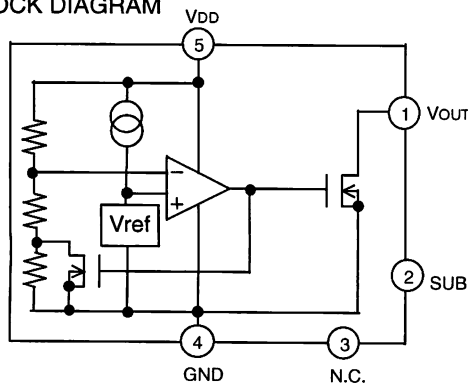
※4 tPLH: VDD=(Vs typ.-0.5V)→(Vs typ.+0.5V)

OPHYSICAL DIMENSIONS, MARKING



VSO5F5 (UNIT:mm)

OBLOCK DIAGRAM



OPIN NO. , PIN NAME

| Pin Number | Pin Name |
|------------|----------|
| 1 | VOUT |
| 2 | SUB |
| 3 | N.C. |
| 4 | GND |
| 5 | VDD |

NOTE : Substrate Pin should be connected with GND

* Please refer to Technical note concerning application circuit, and etc.

○STANDARD DETECTION VOLTAGE AND MARKING

| Type | Standard Detection Voltage[V] | Marking | Type | Standard Detection Voltage[V] | Marking |
|--------|-------------------------------|---------|--------|-------------------------------|---------|
| BD4860 | 6.000 | EW | BD4841 | 4.100 | EB |
| BD4859 | 5.900 | EV | BD4840 | 4.000 | EA |
| BD4858 | 5.800 | EU | BD4839 | 3.900 | DV |
| BD4857 | 5.700 | ET | BD4838 | 3.800 | DU |
| BD4856 | 5.600 | ES | BD4837 | 3.700 | DT |
| BD4855 | 5.500 | ER | BD4836 | 3.600 | DS |
| BD4854 | 5.400 | EQ | BD4835 | 3.500 | DR |
| BD4853 | 5.300 | EP | BD4834 | 3.400 | DQ |
| BD4852 | 5.200 | EN | BD4833 | 3.300 | DP |
| BD4851 | 5.100 | EM | BD4832 | 3.200 | DN |
| BD4850 | 5.000 | EL | BD4831 | 3.100 | DM |
| BD4849 | 4.900 | EK | BD4830 | 3.000 | DL |
| BD4848 | 4.800 | EJ | BD4829 | 2.900 | DK |
| BD4847 | 4.700 | EH | BD4828 | 2.800 | DJ |
| BD4846 | 4.600 | EG | BD4827 | 2.700 | DH |
| BD4845 | 4.500 | EF | BD4826 | 2.600 | DG |
| BD4844 | 4.400 | EE | BD4825 | 2.500 | DF |
| BD4843 | 4.300 | ED | BD4824 | 2.400 | DE |
| BD4842 | 4.200 | EC | BD4823 | 2.300 | DD |

ONOTES FOR USE

- 1 . Absolute maximum range
Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.
- 2 . GND potential
GND terminal should be a lowest voltage potential every state.
Please make sure all pins which are over ground even if include transient feature.
- 3 . Electrical Characteristics
Be sure to check the electrical characteristics, that is one the tentative specification will be changed by temperature, supply voltage, and external circuit.
- 4 . Bypass capacitor for noise rejection
Please put into capacitor to reject noise between VDD pin and GND.
If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point
- 5 . Short Circuit between Terminals and Soldering
Don't short-circuit between Output pin and VDD pin, Output pin and GND pin, or VDD pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.
- 6 . Electromagnetic field
Mal-function may happen when the device is used in the strong electromagnetic field.
- 7 . When using high VDD pin impedance, the through current may cause oscillation.
- 8 . When using high VDD pin impedance, set capacitor between VDD-GND.
- 9 . When VDD drops and goes below the minimum operating voltage, output is uncertain; when the output is pulled up, output becomes the voltage is the same as VDD.
10. BD48XFVE has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. Also, If the leakage is assumed between the VOUT terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.
11. External parameters
The recommended parameter range for R_L is $50k\Omega \sim 1M\Omega$. When attempting to operate beyond these parameters, be sure to verify the actual operation before continuing use.
12. Power on reset operation
Please note that the power on reset output varies with the Vcc rise up time.
Please verify the actual operation.

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