Ordering number : ENN6497A

Monolithic Digital IC

LB11975

High-Speed CD-ROM Spindle Motor Driver IC

Overview

The LB11975 is a monolithic bipolar IC developed for uses as a spindle motor driver for high-speed CD-ROM and DVD-ROM drives. To minimize heat generation during high-speed rotation and braking, the LB11975 adopts direct PWM drive in the output stage. During reverse braking the upper and lower side output transistors are both driven in PWM mode to implement dual PWM controlled braking. The device thus controls the current to remain under a limit value and prevent rapid heat generation. This prevents device destruction due to rapid heating. The absolute maximum voltage rating is 27 V, and the maximum current is 2.5 A.

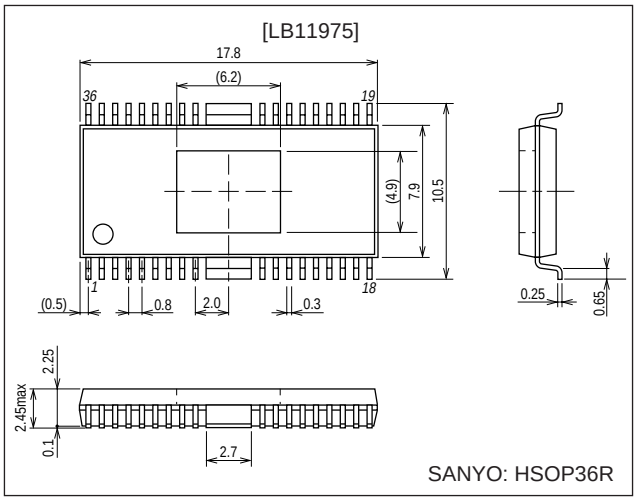
Functions and Features

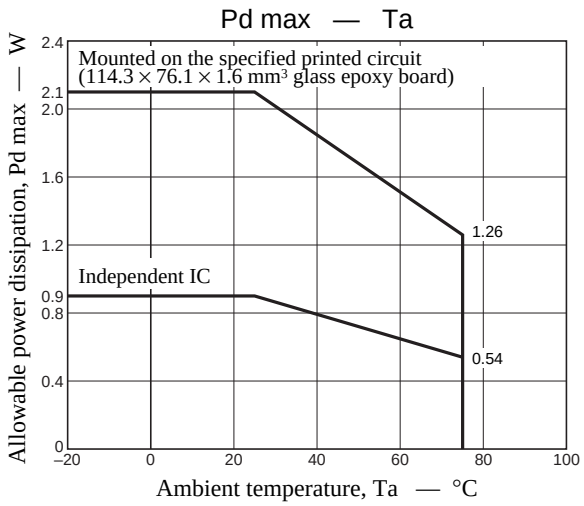
- Direct PWM drive (lower side control)
- Built-in upper and lower side output diodes
- Supports the use 3.3 V DSP devices.
- Power saving function for standby mode
- Hall FG output (1 or 3 Hall device operation)
- Built-in Hall device power supply
- Reverse rotation detection output and drive cutoff circuit
- Voltage control amplifier
- Current limiter circuit
- Thermal protection circuit

Package Dimensions

unit: mm

3251-HSOP36R





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11201RM (OT) No. 6497-1/12

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$ max		7	V
Supply voltage 2	$V_{CC}2$ max		27	V
Supply voltage 3	$V_{CC}3$ max		27	V
Output current	I_O max		2.5	A
Output applied voltage	V_{IN} max		30	V
Allowable power dissipation 1	Pd max1	Independent IC	0.9	W
Allowable power dissipation 2	Pd max2	Mounted on the specified circuit board ($114.3 \times 76.1 \times 1.6$ mm^3 glass epoxy board)	2.1	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power-supply voltage range 1	$V_{CC}1$		4 to 6	V
Power-supply voltage range 2	$V_{CC}2$	$V_{CC}2 \geq V_{CC}1$	4 to 16	V
Power-supply voltage range 3	$V_{CC}3$		4 to 16	V
FG pin applied voltage	VFG		0 to $V_{CC}1$	V
FG pin output current	IFG		0 to 4.0	mA

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 5 V, $V_{CC}2 = V_S$ = 12 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$-1	$V_{CTL} = V_{CREF}$	5.0	8.0	11.0	mA
	$I_{CC}1$-2	VS/S = 0 V		0	200	µA
Supply current 2	$I_{CC}2$-1	$V_{CTL} = V_{CREF}$	5.0	6.5	8.0	mA
	$I_{CC}2$-2	VS/S = 0 V		0	200	µA
Supply current 3	$I_{CC}3$-1	$V_{CTL} = V_{CREF}$		0.3	0.7	mA
	$I_{CC}3$-2	VS/S = 0 V		0	200	µA
[Output Block]						
Output saturation voltage 1	$V_O$sat1(L)	I_O = 0.5 A, V_O(sink), $V_{CC}1$ = 5 V, $V_{CC}2 = V_{CC}3$ = 12 V		0.15	0.25	V
	$V_O$sat1(H)	I_O = 0.5 A, V_O(source), $V_{CC}1$ = 5 V, $V_{CC}2 = V_{CC}3$ = 12 V		0.80	0.95	V
Output saturation voltage 2	$V_O$sat2(L)	I_O = 1.5 A, V_O(sink), $V_{CC}1$ = 5 V, $V_{CC}2 = V_{CC}3$ = 12 V		0.40	0.60	V
	$V_O$sat2(H)	I_O = 1.5 A, V_O(source), $V_{CC}1$ = 5 V, $V_{CC}2 = V_{CC}3$ = 12 V		1.10	1.30	V
Output leakage current	$I_O$leak(L)				100	µA
	$I_O$leak(H)		–100			µA
Diode forward voltage	V_FH	Upper side diode, I_O = 2.0 A		1.50	2.00	V
	V_FL	Lower side diode, I_O = 2.0 A		1.50	2.00	V
[Hall Amplifier Block]						
Input bias current	I_{HB}		–4	–1		µA
Common-mode input voltage range	V_{ICM}		1.5		V_{CC} – 1.5	V
Hall input sensitivity	V_{HIN}		60			mVp-p
Hysteresis	ΔV_{IN}(HA)		23	32	39	mV
Input voltage: low → high	V_{SL}H		6	16	25	mV
Input voltage: high → low	V_{SL}L		–25	–16	–6	mV
[Thermal Protection Circuit]						
Operating temperature	T-TSD	Design target value (junction temperature) *	150	180	210	°C
Hysteresis	ΔTSD	Design target value (junction temperature) *		40		°C

Note: * These are design target values and are not tested.

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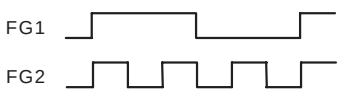
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PWM Oscillator]						
High-level output voltage	V_OH(OSC)		3.1	3.3	3.5	V
Low-level output voltage	V_OL(OSC)		1.4	1.6	1.8	V
Amplitude	V(OSC)		1.5	1.7	1.9	Vp-p
Oscillator frequency	f(OSC)	C = 2200 pF		23.0		kHz
Charge current	I_{CHG}		–110	–94	–83	µA
Charge resistor value	R_{DCHG}		1.6	2.1	2.6	kΩ
[CTL Amplifier]						
VCTL pin input current	I_{VCTL}	V_{CTL} = V_{CREF} = 1.65 V	–2			µA
VCREF pin input current	I_{VCREF}	V_{CTL} = V_{CREF} = 1.65 V	–2			µA
Forward rotation gain	GDF^+	Design target value *	0.20	0.25	0.30	times
Reverse rotation gain	GDF^-	Design target value *	–0.30	–0.25	–0.20	times
Forward rotation limiter voltage	$V_{RF}1$		0.26	0.29	0.32	V
Reverse rotation limiter voltage	$V_{RF}2$		0.26	0.29	0.32	V
Startup voltage	V_{CTH}	V_{CREF} = 1.65 V. Design target value *	1.50		1.80	V
Dead zone	V_{DZ}	V_{CREF} = 1.65 V. Design target value *	35	80	140	mV
[FG Pin] (speed pulse output)						
Low-level output voltage	V_{FGL}	I_{FG} = 2 mA			0.4	V
Pull-up resistor value	R_{FG}		7.5	10	12.5	kΩ
[RS Pin]						
Low-level output voltage	V_{RSL}	I_{RS} = 2 mA			0.4	V
Pull-up resistor value	R_{RS}		7.5	10	12.5	kΩ
[Stop/Start Pin]						
Low-level input voltage	V_{SS}L			0	0.7	V
High-level input voltage	V_{SS}H		2.0		$V_{CC}1$	V
Low-level input current	I_{SS}L	V_{SS} = 0 V	–1	0		µA
High-level input current	I_{SS}H	V_{SS} = 5.0 V		50	200	µA
[Hall Device Power Supply]						
Hall device supply voltage	V_H	I_H = 5 mA	0.65	0.85	1.05	V
Allowable current	I_H				20	mA

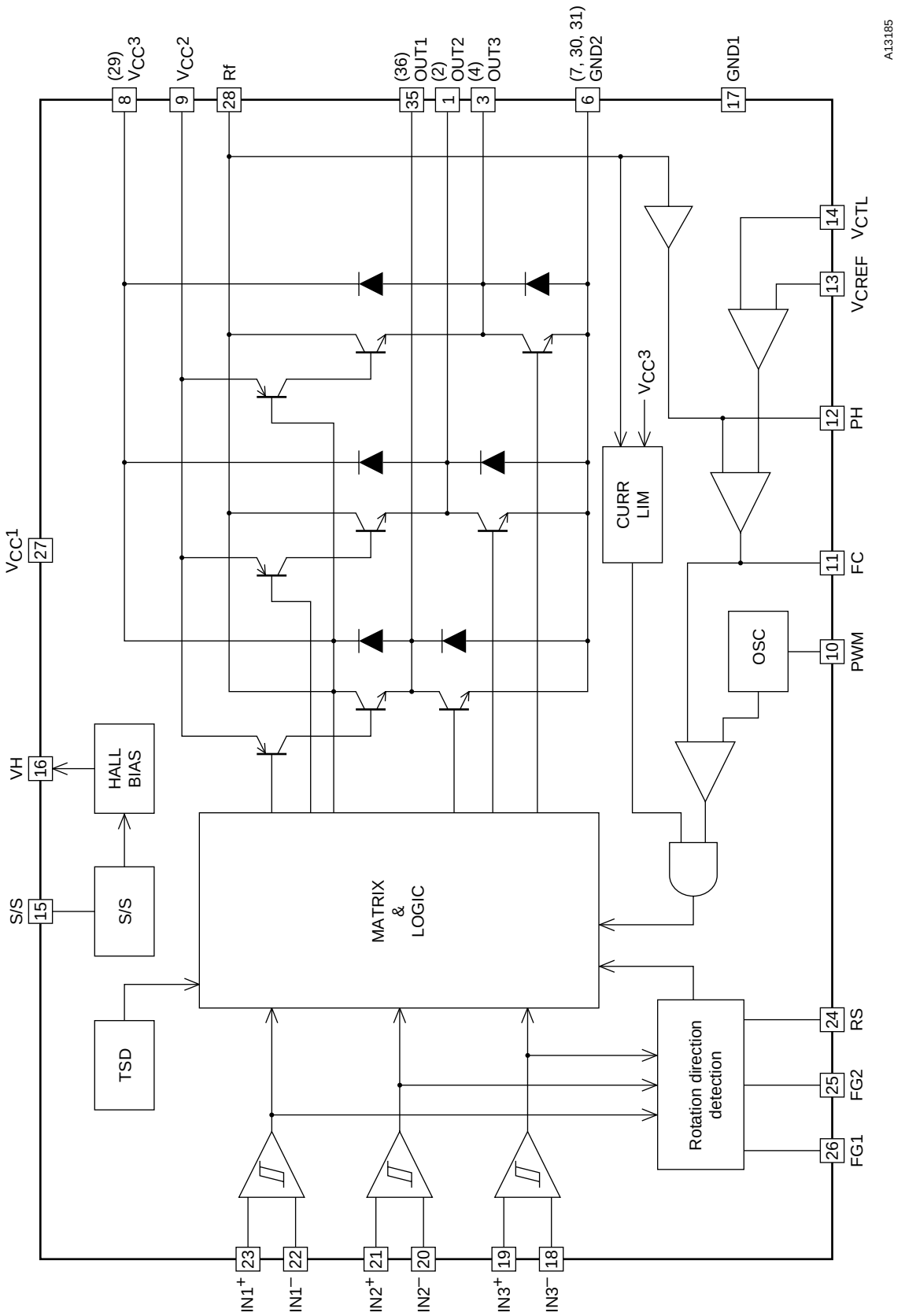
Note: * These are design target values and are not tested.

Truth Table

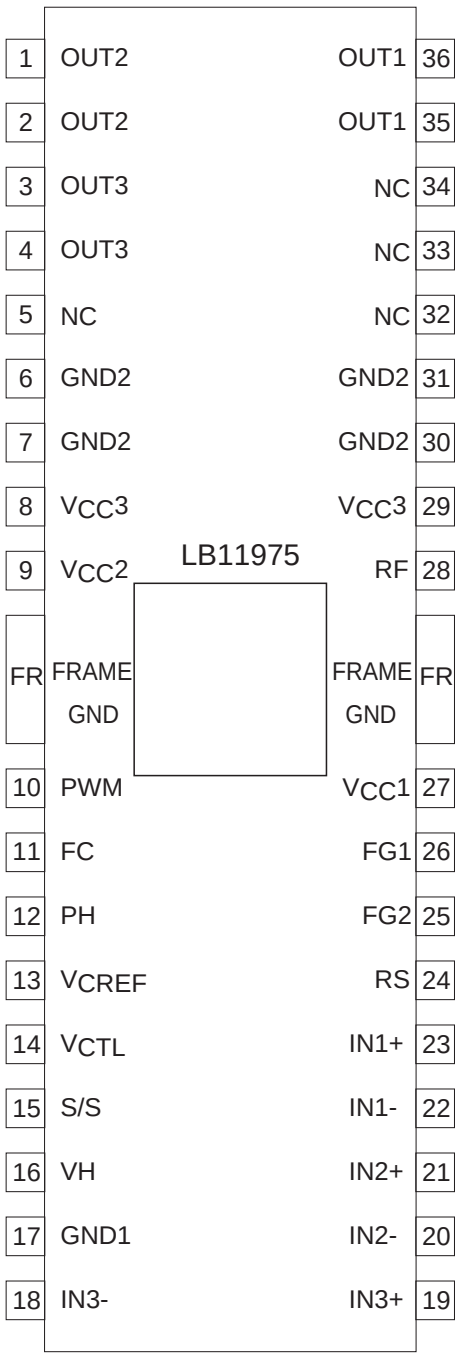
	Input			Control voltage V_{CTL}	Output	FG output	
	IN1	IN2	IN3		Source → Sink	FG1	FG2
1	H	L	H	H	OUT2 → OUT1	L	H
				L	OUT1 → OUT2		
2	H	L	L	H	OUT3 → OUT1	L	L
				L	OUT1 → OUT3		
3	H	H	L	H	OUT3 → OUT2	L	H
				L	OUT2 → OUT3		
4	L	H	L	H	OUT1 → OUT2	H	L
				L	OUT2 → OUT1		
5	L	H	H	H	OUT1 → OUT3	H	H
				L	OUT3 → OUT1		
6	L	L	H	H	OUT2 → OUT3	H	L
				L	OUT3 → OUT2		



Block Diagram

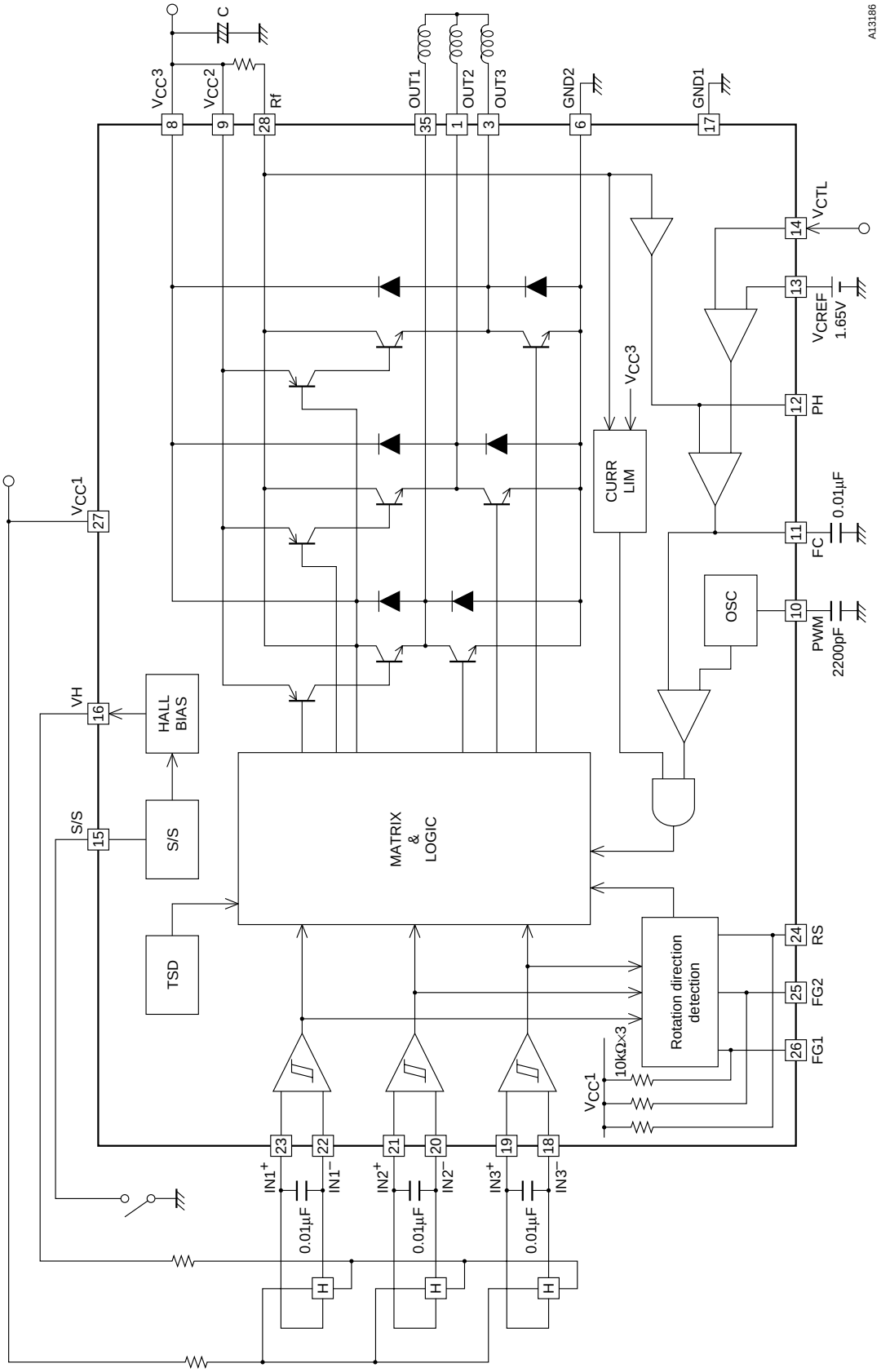


Pin Assignment

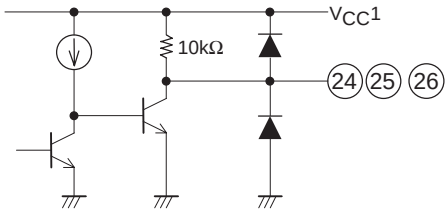
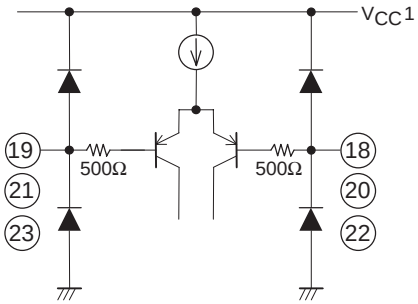
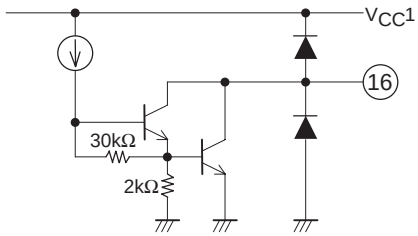
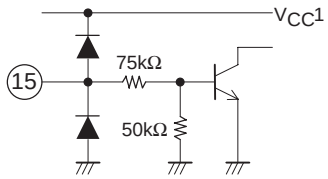


Top view

Sample Application Circuit



Pin Functions

Pin No.	Pin	Pin voltage	Function	Equivalent circuit
9	$V_{CC}2$	4 V to 16 V	Supplies the source side pre-drive voltage.	
8 29	$V_{CC}3$	4 V to 16 V	Supplies the motor drive voltage.	
27	$V_{CC}1$	4 V to 16 V	Supply voltage for all circuits other than the output transistors and the source side pre-drive voltage	
24	RS		Reverse rotation detection High-level output: Forward rotation Low-level output: Reverse rotation	
26	FG1		Single Hall device waveform Schmitt comparator synthesized output	
25	FG2		Three Hall device waveform Schmitt comparator synthesized output	
23	$IN1^+$	1.5 V to $V_{CC}1$ – 1.5 V	U phase Hall device input. Logic high refers to the state where $IN1^+ > IN1^-$.	
22	$IN1^-$			
21	$IN2^+$		V phase Hall device input. Logic high refers to the state where $IN2^+ > IN2^-$.	
20	$IN2^-$			
19	$IN3^+$		W phase Hall device input. Logic high refers to the state where $IN3^+ > IN3^-$.	
18	$IN3^-$			
16	VH		Provides the Hall device lower side bias voltage.	
15	S/S	0 V to $V_{CC}1$	All circuits can be set to the non-operating state by setting this pin to 0.7 V or under, or by setting it to the open state. This pin must be held at 2 V or higher.	
17	GND1		Ground for all circuits except the output	

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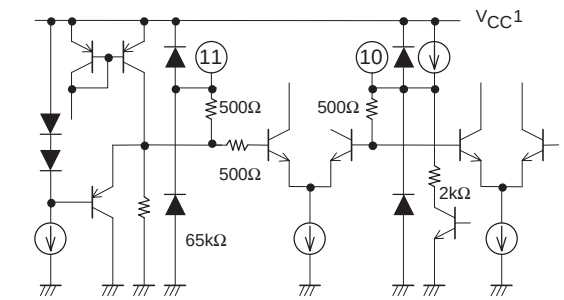
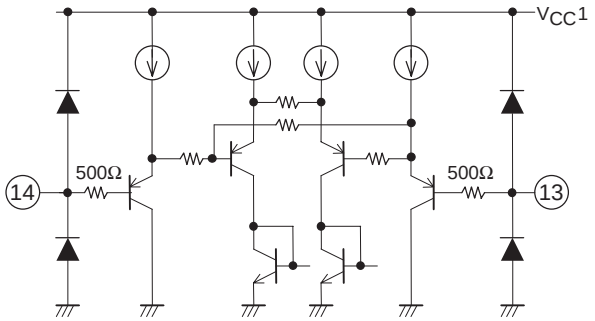
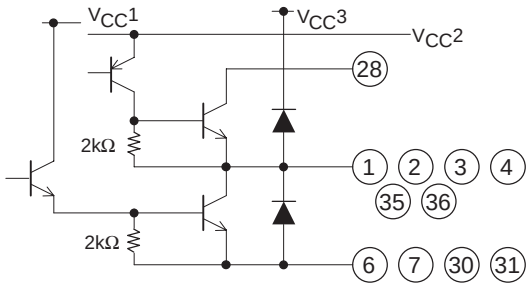
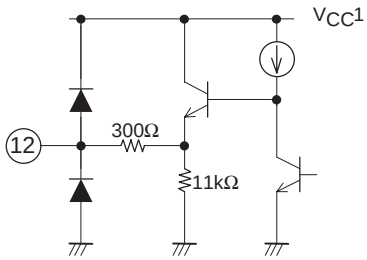
Pin No.	Pin	Pin voltage	Function	Equivalent circuit
11	FC		Control loop frequency characteristics correction Closed loop oscillation in the current control system can be stopped by connecting a capacitor between this pin and ground.	
10	PWM		PWM oscillator capacitor connection	
13	V_{CREF}	0 V to $V_{CC}1$ – 1.5 V	Control reference voltage input The control start voltage is determined by this voltage.	
14	V_{CTL}	0 V to $V_{CC}1$ – 1.5 V	Speed control voltage input This IC implements a voltage control system in which VC > V_{CREF} means forward rotation and VC < V_{CREF} means slow foward rotation. (This IC includes reverse rotation prevention circuit, so reverse rotation will not occur.)	
3, 4	OUT3		W phase output	
6, 7 30, 31	GND2		Ground for the output transistors	
1, 2	OUT2		V phase output	
35, 36	OUT1		U phase output	
28	RF		Upper side npn transistor collector (shared by all three phases) Connect a resistor between $V_{CC}3$ and the RF pin for current detection. The fixed current control system and the current limiter operate by detecting this voltage.	
12	PH		Peak hold circuit capacitor connection. Connect a capacitor to this pin to smooth the voltage detected by the resistor RF.	

Torque Command

Figure 1 shows the relationship between the control voltage (V_{CTL}) and the RF voltage.

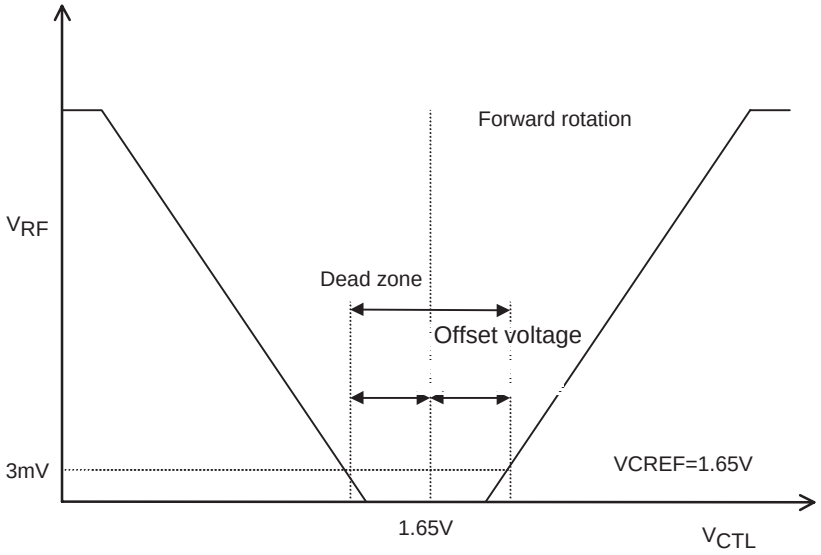


Figure 1

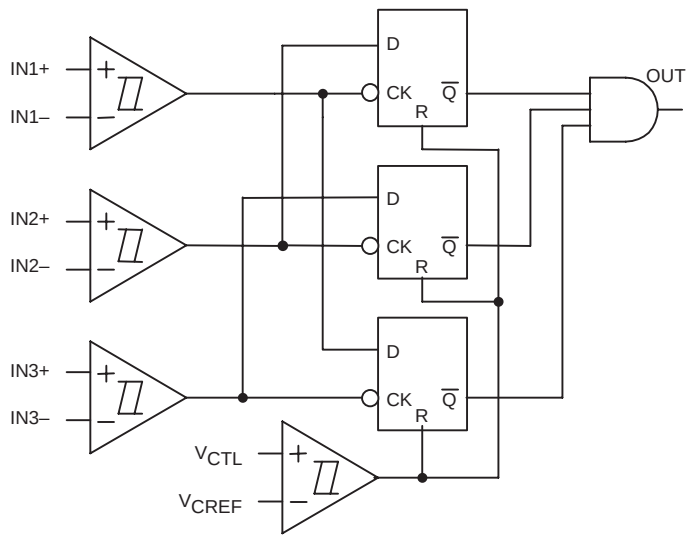
Truth Table

	Operation
$V_{CTL} > V_{CREF}$	Forward rotation
$V_{CREF} > V_{CTL}$	Reverse torque braking *

Note: * Since this IC includes a reverse rotation prevention circuit, although the IC will brake the motor if the motor is rotating and $V_{CTL} < V_{CREF}$, when reverse rotation is detected, the IC will turn the output off, thus stopping motor rotation.

Reverse Rotation Detection Circuit Truth Table

	RS pin
Forward rotation	HIGH
Reverse rotation	LOW



During forward rotation:

The OUT signal is set high to reset DFF.

During reverse rotation:

Reverse rotation is detected when the Hall comparator output falls.

At that point the OUT signal is set to the low level.

Figure 2 Reverse Rotation Detection Circuit Block Diagram

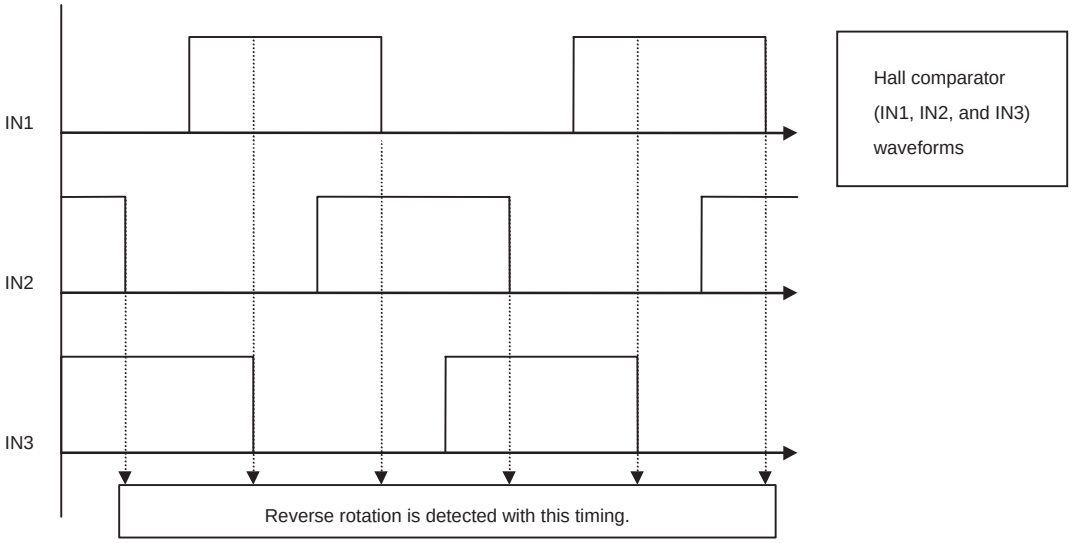


Figure 3 Reverse Rotation Timing Chart

Overview of Reverse Torque Braking

(This circuit uses a direct PWM drive technique and allows the current limiter to operate during reverse torque braking.)

In earlier direct PWM motor drivers, speed control was implemented by applying PWM to only one (either the upper or lower) output transistor. With this type of driver, the regenerative current formed during reverse torque braking operated as a short-circuit braking. As a result problems such as the coil current exceeding the limit value and $I_O$max being exceeded, would occur. To prevent these problems, the LB11975 switches both the upper and lower side output transistors during reverse torque braking to suppress the generation of overcurrents due to regenerative currents when the PWM is off and allows the optimal design of drive currents.

Supplementary Documentation

Coil current during reverse torque braking

(1) Earlier ICs, with the lower side transistor was switched and the upper side transistor used for current detection (RF)
During reverse torque braking, when the coil current increases and the limit is reached, the lower side output transistor is turned off. At this time the regenerative current flows through the upper side transistor. The circuit path is as follows:
Coil → upper side diode → V_{CC} → RF → upper side transistor → coil
During regeneration, the upper side transistor is on and the back EMF that occurs at the upper side transistor's emitter pin has a low potential, and since the upper side transistor is fully on at that point, the circuit functions as short-circuit braking.
Even if the regenerative current results in the RF voltage reaching the limit voltage, since the upper side transistor cannot be turned off, the limit circuit will not operate and a coil current in excess of $I_O$max may occur.

(2) Earlier ICs, with the upper side transistor was switched and the upper side transistor used for current detection (RF)
During reverse torque braking, when the coil current increases and the limit is reached, the upper side output transistor is turned off. At this time the regenerative current flows through the lower side transistor. The circuit path is as follows:
Coil → lower side transistor → ground → lower side diode → coil
During regeneration, the lower side transistor is on and the back EMF that occurs at the lower side transistor's collector pin has a high potential, and since the lower side transistor is fully on at that point, the circuit functions as short-circuit braking.
Since the regenerative current does not flow through the RF pin, the current limiter circuit does not operate, and a current in excess of $I_O$max may occur in the lower side transistor.

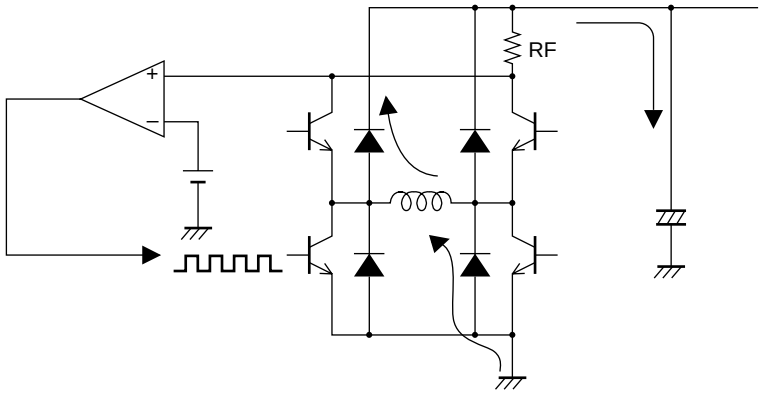
(3) When both the upper and lower side transistors are switched and current detection (RF) is performed in the upper side transistor

During reverse torque braking, when the coil current increases and the limit is reached, both the upper and lower side transistors are turned off. The motor current circuit path at this point is as follows:

Coil → upper side diode → V_{CC} → power supply line capacitor → ground → lower side diode → coil

When the limiter circuit operates, both the upper and lower side transistors are turned off, so short-circuit breaking does not occur, and coil current attenuation is all that occurs. Thus this technique allows current control at the set (limiter) current to be performed even during reverse torque braking.

Regenerative Current Path



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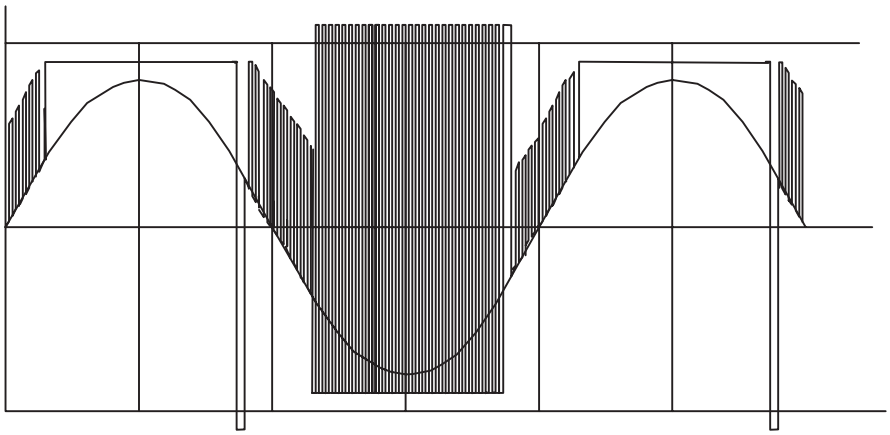
Drive Mode



Braking Mode