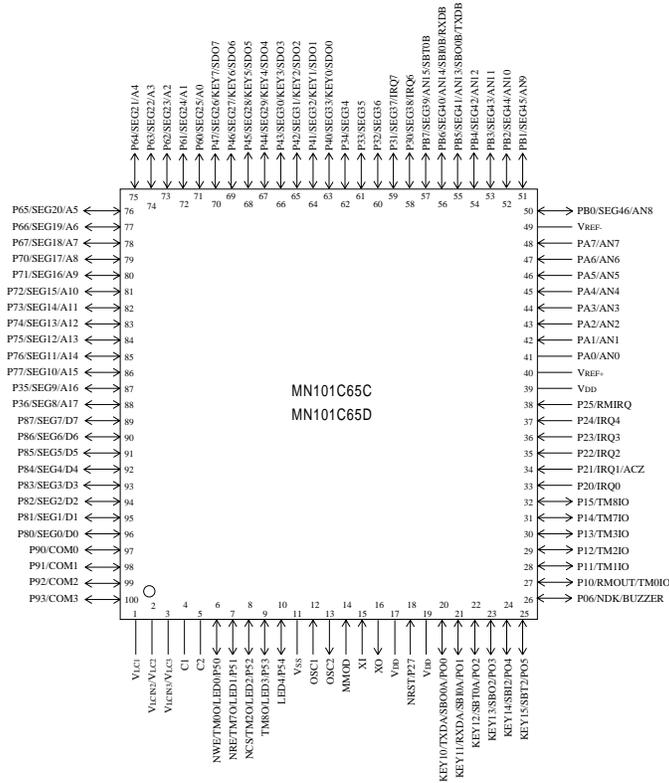


# □ MN101C65C , MN101C65D

<b>Type</b>	MN101C65C (under planning)	MN101C65D (under planning)
<b>ROM (×8-bit)</b>	48 K	64 K
<b>RAM (×8-bit)</b>	2 K	2 K
<b>Package</b>	QFP100-P-1818B *Lead-free (under planning), LQFP100-P-1414 *Lead-free (under planning)	
<b>Minimum Instruction Execution Time</b>	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)*	
	* The lower limit for operation guarantee for flash memory built-in type is 2.5 V.	
<b>Interrupts</b>	<ul style="list-style-type: none"> <li>• RESET • Watchdog • External 0 • External 1 • External 2 • External 3</li> <li>• External 4 (key interrupt selectable) • External 5 (key interrupt dedicated) • External 6 • External 7</li> <li>• Remote control • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6</li> <li>• Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish</li> </ul>	
<b>Timer Counter</b>	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible)</p> <p>Clock source ..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source ..... coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event)</p> <p>Clock source ..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source ..... coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible)</p> <p>Clock source ..... 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source ..... coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer)</p> <p>Clock source ..... 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source ..... coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source ..... 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source ..... coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible)</p> <p>Clock source ..... 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency</p> <p>Interrupt source ..... coincidence with compare register 7 (2 lines)</p>	



## Pin Assignment



QFP100-P-1818B \*Lead-free (under planning)

LQFP100-P-1414 \*Lead-free (under planning)

## Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C65-QFP100-P-1818B (under planning)
Flash Memory Built-in Type	Type MN101CF65D (under planning)
	ROM (× 8-bit) 64 K
	RAM (× 8-bit) 2 K
	Minimum instruction execution time 0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.5 V to 5.5 V, 32 kHz)
	Package QFP100-P-1818B *Lead-free (under planning), LQFP100-P-1414 *Lead-free (under planning)



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