

# MN673274

## Signal-Processing IC for Multipurpose Cameras

### ■ Overview

The MN673274 is designed for surveillance and PC input cameras. In addition to the basic functions of luminance signal and chrominance signal processing, it also integrates microcontroller functions (ALC, AWB, and AGC) and SSG, CG, and I<sup>2</sup>C-bus circuits on a single chip.

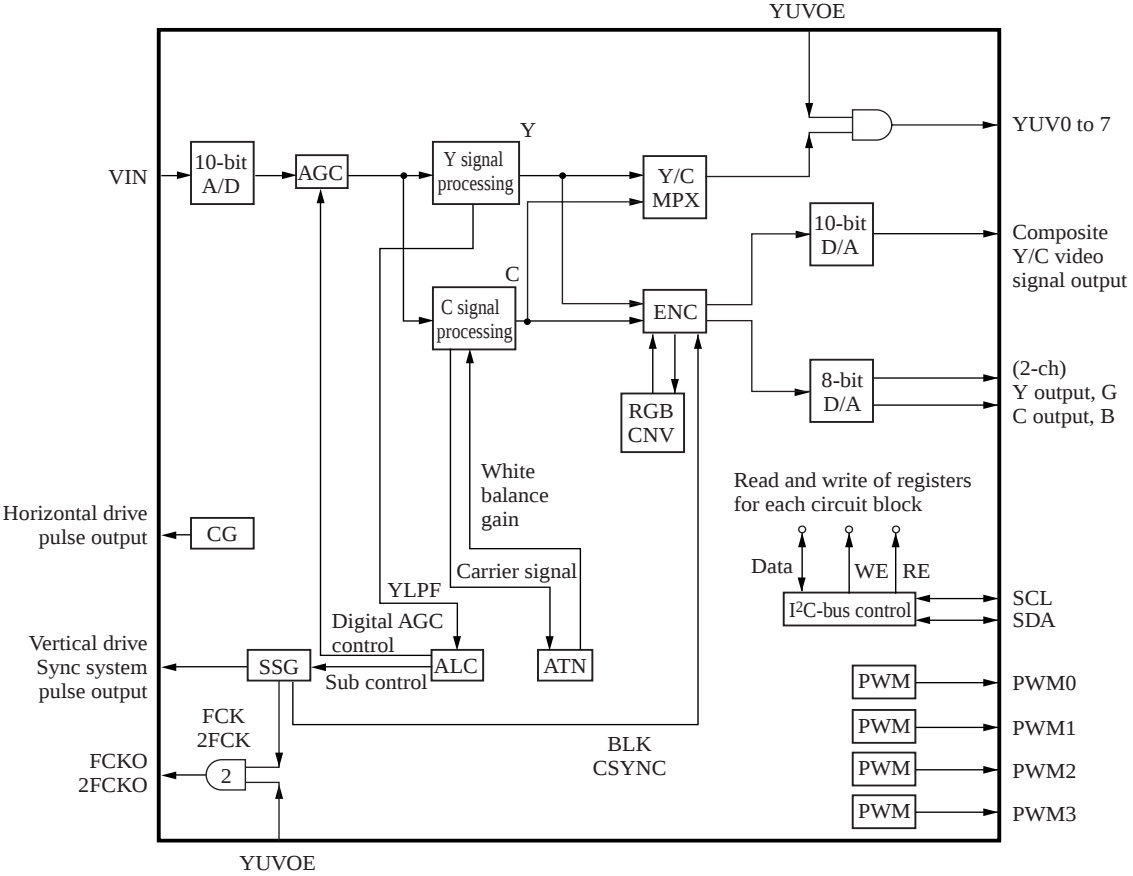
### ■ Features

- Input: Analog signal (A/D converter input)
- Output: Digital output
  - YUV signal: 8 bits
- Analog outputs
  - Y signal
  - C signal
  - Composite video output
  - RGB outputs
- Operating supply voltage: 3.3 V  $\pm$  0.3 V
- Operating frequency: 9.5 MHz to 28.7 MHz
- Main functions
  - 10-bit A/D converter
  - 10-bit D/A converter
  - 2-channel 8-bit D/A converter
  - Support for analog AGC (NN2038, NN2039)
  - CG and SSG functions
  - 510H and 768H (Supports NTSC and PAL )
  - Supports progressive scan readout CCDs with complementary color filters for VGA
  - Supports black-and-white CCD signal processing
  - CCD white defect/black defect correction circuit
  - Maximum digital AGC gain: 24 dB
  - Left/right reversing function
  - Variable gamma correction ( $\gamma = 0.3$  to 1)
  - ZV port conforming mode, BT656 conforming mode
  - External synchronization support: HD/VD, VD2, Sync., LL mode
  - On-chip I<sup>2</sup>C-bus circuit
  - ELC/AGC (Also supports external AGC)
  - Two-mode white balance (manual/ATW) with ATW lock function
  - Automatic OB correction function

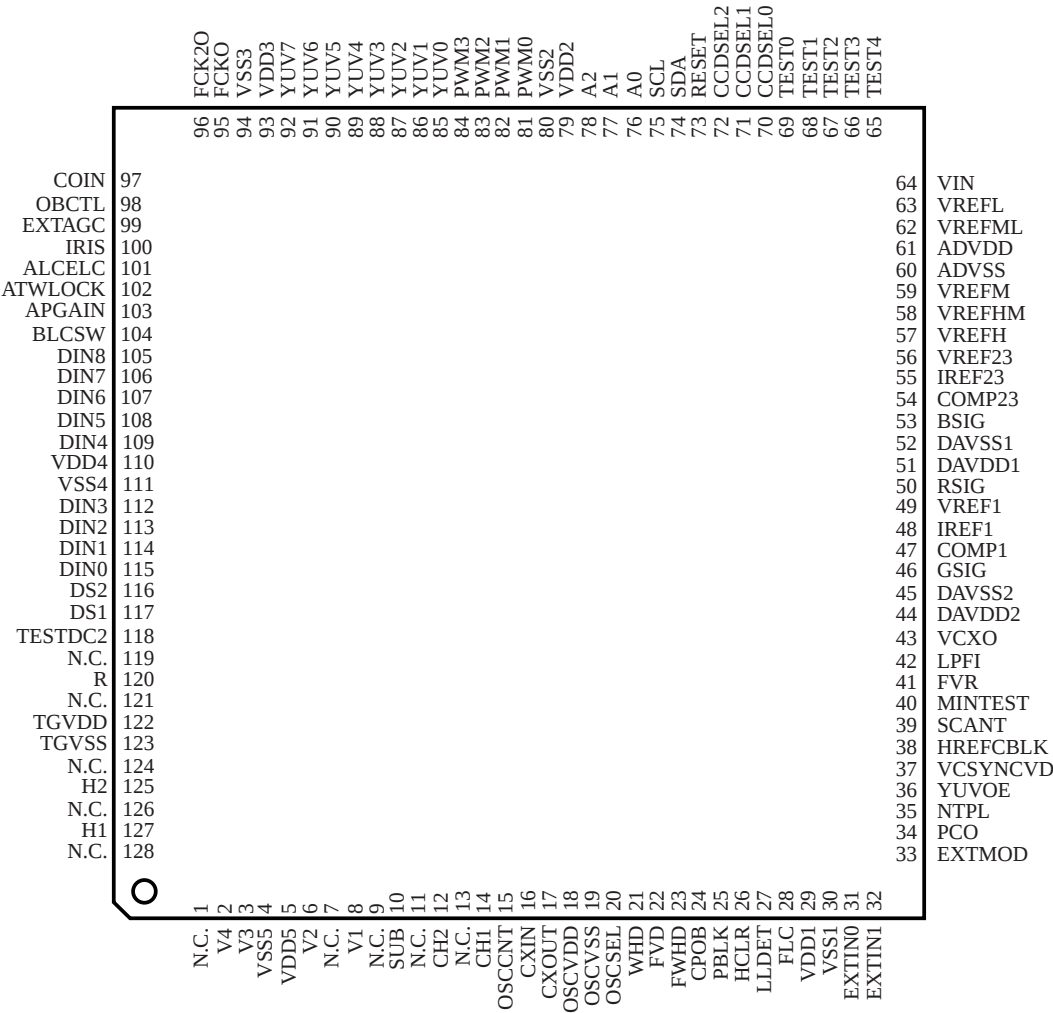
### ■ Applications

- Surveillance cameras, PC cameras

■ Block Diagram



■ Pin Arrangement



(TOP VIEW)

## ■ Pin Descriptions

| Pin No. | Pin Name | I/O | Description                                                                                                     |
|---------|----------|-----|-----------------------------------------------------------------------------------------------------------------|
| 1       | N.C.     | —   | —                                                                                                               |
| 2       | V4       | O   | $\phi$ V4 charge pulse                                                                                          |
| 3       | V3       | O   | $\phi$ V3 charge pulse                                                                                          |
| 4       | VSS5     | VSS | Digital system ground                                                                                           |
| 5       | VDD5     | VDD | Digital system power supply (3.3 V)                                                                             |
| 6       | V2       | O   | $\phi$ V2 charge pulse                                                                                          |
| 7       | N.C.     | —   | —                                                                                                               |
| 8       | V1       | O   | $\phi$ V1 charge pulse                                                                                          |
| 9       | N.C.     | —   | —                                                                                                               |
| 10      | SUB      | O   | Vertical exclusion pulse                                                                                        |
| 11      | N.C.     | —   | —                                                                                                               |
| 12      | CH2      | O   | V3 charge pulse                                                                                                 |
| 13      | N.C.     | —   | —                                                                                                               |
| 14      | CH1      | O   | V1 charge pulse                                                                                                 |
| 15      | OSCCNT   | O   | Oscillator control test                                                                                         |
| 16      | CXIN     | I   | Synchronization oscillator connection (crystal oscillator)                                                      |
| 17      | CXOUT    | O   | Synchronization oscillator connection (crystal oscillator)                                                      |
| 18      | OSCVDD   | VDD | Oscillator cell power supply                                                                                    |
| 19      | OSCVSS   | VSS | Oscillator cell ground                                                                                          |
| 20      | OSCSEL   | I   | Source oscillator 2FCK/4FCK switching                                                                           |
| 21      | WHD      | O   | WHD signal with a normal phase to Sync                                                                          |
| 22      | FVD      | O   | VD signal with a normal phase to Sync                                                                           |
| 23      | FWHD     | O   | WHD for CG drive                                                                                                |
| 24      | CPOB     | O   | A/D converter input signal clamping pulse/ D/A converter output clamping pulse                                  |
| 25      | PBLK     | O   | Pre-blanking pulse                                                                                              |
| 26      | HCLR     | O   | Horizontal reference signal                                                                                     |
| 27      | LLDET    | I   | Power supply synchronization switching Low: internal synchronization, high: LL synchronization                  |
| 28      | FLC      | I   | Flicker correction (pulled-up input) High: flicker correction on                                                |
| 29      | VDD1     | VDD | Digital system power supply (3.3 V)                                                                             |
| 30      | VSS1     | VSS | Digital system ground                                                                                           |
| 31      | EXTIN0   | I   | External synchronization input 1                                                                                |
| 32      | EXTIN1   | I   | External synchronization input 2                                                                                |
| 33      | EXTMOD   | I   | Surveillance/automotive mode switching (pulled-up input) High: automotive mode (HDVD/Sync synchronization mode) |
| 34      | PCO      | O   | Phase comparator output                                                                                         |
| 35      | NTPL     | I   | NTSC/PAL switching Low: NTSC, high: PAL (pulled-down input)                                                     |

## ■ Pin Descriptions (continued)

| Pin No. | Pin Name | I/O | Description                                                                                  |
|---------|----------|-----|----------------------------------------------------------------------------------------------|
| 36      | YUVOE    | I   | Digital output system output enable                                                          |
| 37      | VCSYNCVD | O   | VCSYNC output/VD output (VGA mode: CSYNC, IT mode: register switching)                       |
| 38      | HREFCBLK | O   | HREF output/CBLK output (VGA mode: HREF, IT mode: register switching)                        |
| 39      | SCANT    | I   | Test input (Normally connect low)                                                            |
| 40      | MINTEST  | I   | Test input (Normally connect low)                                                            |
| 41      | FVR      | I   | DC level input used for frequency control                                                    |
| 42      | LPFI     | I   | Low-pass filter analog switch input                                                          |
| 43      | VCXO     | O   | Analog switch output - LC oscillator                                                         |
| 44      | DAVDD2   | VDD | D/A converter power supply                                                                   |
| 45      | DAVSS2   | VSS | D/A converter ground                                                                         |
| 46      | GSIG     | O   | Video output (composite/G signal) Connect the resistor $R_L$ between GSIG and DAVSS2         |
| 47      | COMP1    | I   | Phase compensation Connect a 1 $\mu$ F capacitor between COMP1 and DAVDD2                    |
| 48      | IREF1    | I   | Bias current resistor connection Connect the resistor $R_{IREF}$ between IREF1 and DAVSS2    |
| 49      | VREF1    | I   | Reference voltage input                                                                      |
| 50      | RSIG     | O   | Video output (luminance/R signal) Connect the resistor $R_L$ between RSIG and DAVSS1         |
| 51      | DAVDD1   | VDD | D/A converter power supply                                                                   |
| 52      | DAVSS1   | VSS | D/A converter ground                                                                         |
| 53      | BSIG     | O   | Video output (chrominance/B signal) Connect the resistor $R_L$ between BSIG and DAVSS1       |
| 54      | COMP23   | I   | Phase compensation Connect a 1 $\mu$ F capacitor between this pin and DAVDD1                 |
| 55      | IREF23   | I   | Bias current resistor connection Connect the resistor $R_{IREF}$ between this pin and DAVSS1 |
| 56      | VREF23   | I   | Reference voltage input                                                                      |
| 57      | VREFH    | I   | High-level reference voltage input                                                           |
| 58      | VREFHM   | I   | Intermediate reference potential Connect a capacitor between this pin and ADVSS              |
| 59      | VREFM    | I   | Intermediate reference potential Connect a capacitor between this pin and ADVSS              |
| 60      | ADVSS    | VSS | A/D converter power supply                                                                   |
| 61      | ADVDD    | VDD | A/D converter ground                                                                         |
| 62      | VREFML   | I   | Intermediate reference potential Connect a capacitor between this pin and ADVSS              |
| 63      | VREFL    | I   | Low-level reference voltage input                                                            |
| 64      | VIN      | I   | Analog signal input                                                                          |
| 65      | TEST4    | I   | Test input (Normally connect low)                                                            |
| 66      | TEST3    | I   | Test input (Normally connect low)                                                            |
| 67      | TEST2    | I   | Test input (Normally connect low)                                                            |
| 68      | TEST1    | I   | Test input (Normally connect low)                                                            |
| 69      | TEST0    | I   | Test input (Normally connect low)                                                            |
| 70      | CCDSEL0  | I   | CCD switching                                                                                |
| 71      | CCDSEL1  | I   | CCD switching                                                                                |
| 72      | CCDSEL2  | I   | CCD switching                                                                                |

# **■ Pin Descriptions (continued)**

| Pin No. | Pin Name | I/O | Description                                                                    |
|---------|----------|-----|--------------------------------------------------------------------------------|
| 73      | RESET    | I   | Logic system initialization                                                    |
| 74      | SDA      | I/O | I <sup>2</sup> C-bus (data)                                                    |
| 75      | SCL      | I/O | I <sup>2</sup> C-bus (clock)                                                   |
| 76      | A0       | I   | EEPROM address (pulled-down input)                                             |
| 77      | A1       | I   | EEPROM address (pulled-down input)                                             |
| 78      | A2       | I   | EEPROM address (pulled-down input)                                             |
| 79      | VDD2     | VDD | Digital system power supply (3.3 V)                                            |
| 80      | VSS2     | VSS | Digital system ground                                                          |
| 81      | PWM0     | O   | PWM signal output                                                              |
| 82      | PWM1     | O   | PWM signal output                                                              |
| 83      | PWM2     | O   | PWM signal output                                                              |
| 84      | PWM3     | O   | PWM signal output                                                              |
| 85      | YUV0     | O   | Digital Y/U/V output (LSB)                                                     |
| 86      | YUV1     | O   | Digital Y/U/V output                                                           |
| 87      | YUV2     | O   | Digital Y/U/V output                                                           |
| 88      | YUV3     | O   | Digital Y/U/V output                                                           |
| 89      | YUV4     | O   | Digital Y/U/V output                                                           |
| 90      | YUV5     | O   | Digital Y/U/V output                                                           |
| 91      | YUV6     | O   | Digital Y/U/V output                                                           |
| 92      | YUV7     | O   | Digital Y/U/V output (MSB)                                                     |
| 93      | VDD3     | VDD | Digital system power supply (3.3 V)                                            |
| 94      | VSS3     | VSS | Digital system ground                                                          |
| 95      | FCKO     | O   | FCK output                                                                     |
| 96      | FCK2O    | O   | 2FCK output                                                                    |
| 97      | COIN     | I   | Synchronization oscillator cell (LC oscillator)                                |
| 98      | OBCTL    | O   | Automatic OB correction output                                                 |
| 99      | EXTAGC   | O   | External AGC control                                                           |
| 100     | IRIS     | O   | Mechanical iris locking (PWM output)                                           |
| 101     | ALCELC   | I   | Locked/ELC switching Low: ELC, high: locked                                    |
| 102     | ATWLOCK  | I   | ATW stop. Low: normal, high: ATWLOCK                                           |
| 103     | APGAIN   | I   | Aperture gain switching Low: register value, high: register value divided by 2 |
| 104     | BLCSW    | I   | Backlighting correction Low: normal, high: ATWLOCK                             |
| 105     | DIN8     | I   | Digital signal input (MSB)                                                     |
| 106     | DIN7     | I   | Digital signal input                                                           |
| 107     | DIN6     | I   | Digital signal input                                                           |
| 108     | DIN5     | I   | Digital signal input                                                           |
| 109     | DIN4     | I   | Digital signal input                                                           |

## ■ Pin Descriptions (continued)

| Pin No. | Pin Name | I/O | Description                         |
|---------|----------|-----|-------------------------------------|
| 110     | VDD4     | VDD | Digital system power supply (3.3 V) |
| 111     | VSS4     | VSS | Digital system ground               |
| 112     | DIN3     | I   | Digital signal input                |
| 113     | DIN2     | I   | Digital signal input                |
| 114     | DIN1     | I   | Digital signal input                |
| 115     | DIN0     | I   | Digital signal input (LSB)          |
| 116     | DS2      | O   | CDS pulse 2                         |
| 117     | DS1      | O   | CDS pulse 1                         |
| 118     | TESTDC2  | I   | Test input (Normally connect low)   |
| 119     | N.C.     | —   | —                                   |
| 120     | R        | O   | $\phi$ R pulse                      |
| 121     | N.C.     | —   | —                                   |
| 122     | TGVDD    | VDD | CG power supply                     |
| 123     | TGVSS    | VSS | CG ground                           |
| 124     | N.C.     | —   | —                                   |
| 125     | H2       | O   | $\phi$ H1 transfer pulse            |
| 126     | N.C.     | —   | —                                   |
| 127     | H1       | O   | $\phi$ H2 transfer pulse            |
| 128     | N.C.     | —   | —                                   |

## ■ Electrical Characteristics

### 1. Absolute Maximum Ratings

| Item                            | Symbol    | Rating                  | Unit |
|---------------------------------|-----------|-------------------------|------|
| Supply voltage (digital system) | $V_{DD}$  | – 0.3 to +4.6           | V    |
| Supply voltage (analog system)  | $AV_{DD}$ | – 0.3 to +4.6           | V    |
| Input voltage                   | $V_I$     | – 0.3 to $V_{DD} + 0.3$ | V    |
| Output voltage                  | $V_O$     | – 0.3 to $V_{DD} + 0.3$ | V    |
| Output current                  | $I_O$     | $\pm 48$                | mA   |
| Power dissipation               | $P_D$     | 750                     | mW   |
| Operating temperature           | $T_{opr}$ | –20 to +70              | °C   |
| Storage temperature             | $T_{stg}$ | –55 to +150             | °C   |

Notes: 1. The absolute maximum ratings are the limiting values for which chip destruction will not occur if that level is applied. Operation is not guaranteed at these levels.

2. The VDD1, VDD2, VDD3, VDD4, VDD5, VDDTG, ADVDD, and DAVDD pins must always be held at the same potential. The VSS1, VSS2, VSS3, VSS4, VSS5, VSSTG, ADVSS, and DAVSS pins must always be held at the same potential.

## ■ Electrical Characteristics (continued)

### 2. Recommended Operating Conditions

$$V_{SS} = TGV_{SS} = OSCV_{SS} = ADV_{SS} = DAV_{SS} = 0 \text{ V}$$

| Item                     | Symbol      | Condition                   | Min | Typ | Max  | Unit |
|--------------------------|-------------|-----------------------------|-----|-----|------|------|
| Supply voltage (digital) | $V_{DD}$    | Digital system power supply | 3.0 | 3.3 | 3.6  | V    |
| Supply voltage (digital) | $OSCV_{DD}$ | Oscillator pin power supply | 3.0 | 3.3 | 3.6  | V    |
| Supply voltage (analog)  | $ADV_{DD}$  | A/D converter power supply  | —   | 3.3 | —    | V    |
| Supply voltage (analog)  | $DAV_{DD}$  | D/A converter power supply  | —   | 3.3 | —    | V    |
| Operating frequency      | $F_{OSC}$   | Duty 50%                    | 9.5 | —   | 28.7 | MHz  |

### 3. DC Characteristics

$$V_{DD} = TGV_{DD} = OSCV_{DD} = 3.0 \text{ V to } 3.6 \text{ V}, ADV_{DD} = DAV_{DD} = 3.0 \text{ V to } 3.6 \text{ V},$$

$$V_{SS} = TGV_{SS} = OSCV_{SS} = ADV_{SS} = DAV_{SS} = 0 \text{ V}, T_a = -20^\circ\text{C to } +70^\circ\text{C}$$

| Item                     | Symbol     | Condition                                            | Min | Typ | Max | Unit |
|--------------------------|------------|------------------------------------------------------|-----|-----|-----|------|
| Operating supply current | $I_{DD}$   | $V_{DD} = TGV_{DD} = TGV_{DD} = 3.6 \text{ V}$       | —   | 80  | 120 | mA   |
|                          | $DAI_{DD}$ | $ADV_{DD} = DAV_{DD} = 3.6 \text{ V}$                | —   | 23  | 33  |      |
|                          | $ADI_{DD}$ | $F_{CLK} = 28.7 \text{ MHz}, T_a = 25^\circ\text{C}$ | —   | 20  | 40  |      |

Input pins 1-1 Standard input pins

EXTIN0, EXTIN1, YUVOE, CCDSEL0 to CCDSEL2, RESET, COIN, ALCELC, ATWLOCK,  
APGAIN, BLCSW, DIN0 to DIN8, H12BSTP, VDDSW, LLDET

|                       |            |                                   |    |                     |   |                     |               |
|-----------------------|------------|-----------------------------------|----|---------------------|---|---------------------|---------------|
| Input voltage         | High level | $V_{IH}$                          |    | $V_{DD} \times 0.8$ | — | $V_{DD}$            | V             |
|                       | Low level  | $V_{IL}$                          |    | 0                   | — | $V_{DD} \times 0.2$ |               |
| Input leakage current | $I_{LIPD}$ | $V_I = V_{DD} \text{ or } V_{SS}$ | —5 | —                   | 5 |                     | $\mu\text{A}$ |

Input pins 1-2 Pulled-up input pins

FLC, EXTMOD

|                       |            |                                        |     |                     |    |                     |               |
|-----------------------|------------|----------------------------------------|-----|---------------------|----|---------------------|---------------|
| Input voltage         | High level | $V_{IH}$                               |     | $V_{DD} \times 0.8$ | —  | $V_{DD}$            | V             |
|                       | Low level  | $V_{IL}$                               |     | 0                   | —  | $V_{DD} \times 0.2$ |               |
| Input leakage current | $I_{LIPD}$ | $V_I = V_{DD}$                         | —10 | —                   | 10 |                     | $\mu\text{A}$ |
| Pull-up resistance    | $R_{PU1}$  | $V_{DD} = 3.3 \text{ V}, V_I = V_{SS}$ | 10  | 30                  | 90 |                     | k $\Omega$    |

Input pins 1-3 Pulled-down input pins

OSCSEL, NTPL, SCANT, A0 to A2, TEST4 to TEST0, MINTEST

|                       |            |                |     |                     |    |                     |               |
|-----------------------|------------|----------------|-----|---------------------|----|---------------------|---------------|
| Input voltage         | High level | $V_{IH}$       |     | $V_{DD} \times 0.8$ | —  | $V_{DD}$            | V             |
|                       | Low level  | $V_{IL}$       |     | 0                   | —  | $V_{DD} \times 0.2$ |               |
| Input leakage current | $I_{LIPD}$ | $V_I = V_{SS}$ | —10 | —                   | 10 |                     | $\mu\text{A}$ |
| Pull-down resistance  | $P_{PD1}$  | $V_I = V_{DD}$ | 10  | 30                  | 90 |                     | k $\Omega$    |

Output pins 1-1 V4 to V1, SUB, CH2, CH1, OSCCNT, PCO, WHD, CPOB, PBLK, HCLR, PWM0 to PWM3, OBCTL,  
EXTAGC, IRIS

|                |            |          |                       |                |   |     |   |
|----------------|------------|----------|-----------------------|----------------|---|-----|---|
| Output voltage | High level | $V_{OH}$ | $I_O = -1 \text{ mA}$ | $V_{DD} - 0.6$ | — | —   | V |
|                | Low level  | $V_{OL}$ | $I_O = 1 \text{ mA}$  | —              | — | 0.4 |   |

## ■ Electrical Characteristics (continued)

### 3. DC Characteristics (continued)

$V_{DD} = TGV_{DD} = OSCV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $ADV_{DD} = DAV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,

$V_{SS} = TGV_{SS} = OSCV_{SS} = ADV_{SS} = DAV_{SS} = 0\text{ V}$ ,  $T_a = -20^\circ\text{C to }+70^\circ\text{C}$

| Item                                   | Symbol            | Condition        | Min                                                                                              | Typ                   | Max  | Unit   |
|----------------------------------------|-------------------|------------------|--------------------------------------------------------------------------------------------------|-----------------------|------|--------|
| Output pins 1-2 YUV7 to YUV0           |                   |                  |                                                                                                  |                       |      |        |
| Output voltage                         | High level        | V <sub>OH</sub>  | I <sub>O</sub> = − 2 mA                                                                          | V <sub>DD</sub> − 0.6 | —    | V      |
|                                        | Low level         | V <sub>OL</sub>  | I <sub>O</sub> = 2 mA                                                                            | —                     | 0.4  |        |
| Output pins 1-3 VCSYNCVD, HREFCBLK     |                   |                  |                                                                                                  |                       |      |        |
| Output voltage                         | High level        | V <sub>OH</sub>  | I <sub>O</sub> = − 4 mA                                                                          | V <sub>DD</sub> − 0.6 | —    | V      |
|                                        | Low level         | V <sub>OL</sub>  | I <sub>O</sub> = 4 mA                                                                            | —                     | 0.4  |        |
| Output pins 1-4 FVD, EWHD, FCKO, FCK2O |                   |                  |                                                                                                  |                       |      |        |
| Output voltage                         | High level        | V <sub>OH</sub>  | I <sub>O</sub> = − 8 mA                                                                          | V <sub>DD</sub> − 0.6 | —    | V      |
|                                        | Low level         | V <sub>OL</sub>  | I <sub>O</sub> = 8 mA                                                                            | —                     | 0.4  |        |
| Output pins 1-5 DS1, DS2, R, H2, H1    |                   |                  |                                                                                                  |                       |      |        |
| Output voltage                         | High level        | V <sub>OH</sub>  | I <sub>O</sub> = − 16 mA                                                                         | V <sub>DD</sub> − 0.6 | —    | V      |
|                                        | Low level         | V <sub>OL</sub>  | I <sub>O</sub> = 16 mA                                                                           | —                     | 0.4  |        |
| I/O pins 1 SDA, SCL                    |                   |                  |                                                                                                  |                       |      |        |
| TTL                                    | Input             | V <sub>T+</sub>  | V <sub>DD</sub> = 3.0 V to 3.6 V                                                                 | —                     | 1.6  | V      |
| Schmitt trigger input voltage          | Threshold voltage | V <sub>T−</sub>  | V <sub>REF5</sub> = 4.75 V to 5.25 V<br>(V <sub>REF5</sub> is an external reference voltage.)    | 0.6                   | 1.2  |        |
| Output voltage                         | Low level         | V <sub>OL</sub>  | I <sub>O</sub> = 4 mA                                                                            | —                     | 0.4  | V      |
| Output leakage current                 |                   | I <sub>LO</sub>  | V <sub>O</sub> = V <sub>DD</sub> or V <sub>SS</sub>                                              | − 10                  | —    | 10 μA  |
| Oscillator pins 1 CXIN, CXOUT          |                   |                  |                                                                                                  |                       |      |        |
| Standard oscillator frequency          |                   | F <sub>OSC</sub> | V <sub>DD</sub> = 3.3 V<br>Using an external crystal                                             | 15                    | —    | 30 MHz |
| Internal feedback resistor             |                   | R <sub>FB</sub>  | V <sub>DD</sub> = 3.3 V<br>V <sub>I</sub> (X <sub>I</sub> ) = V <sub>DD</sub> or V <sub>SS</sub> | 0.73                  | 2.2  | 6.6 kΩ |
| Output voltage                         | High level        | I <sub>OH</sub>  | V <sub>DD</sub> = 3.3 V<br>V <sub>I</sub> = V <sub>SS</sub> , V <sub>O</sub> = V <sub>SS</sub>   | − 9.2                 | − 23 | mA     |
|                                        | Low level         | I <sub>OL</sub>  | V <sub>DD</sub> = 3.3 V<br>V <sub>I</sub> = V <sub>DD</sub> , V <sub>O</sub> = V <sub>DD</sub>   | 9.6                   | 24   |        |

## ■ Electrical Characteristics (continued)

### 4. AC Characteristics

| Item                | Symbol     | Condition | Min                             | Typ  | Max | Unit  |    |
|---------------------|------------|-----------|---------------------------------|------|-----|-------|----|
| Input pins 2-1 CXIN |            |           |                                 |      |     |       |    |
| Clock waveform      | Period     | tcyc      | See figure 1                    | 34.8 | —   | 105.3 | ns |
|                     | Clock duty | dclk      | See figure 1<br>dclk = thi/tcyc | —    | 50  | —     | %  |

Output pins 1 OSCCNT, PCO, PWM0 to PWM3, YUV0 to YUV7, WHD, CPOB, PBLK, HCLR, VCSYNCD, HREFCBLK, FVD, EWHD, OBCTL, EXTAGC, IRIS, FCKO, FCK2O, V1 to V4, SUB, CH1, CH2, DS1, DS2, R, H2, H1

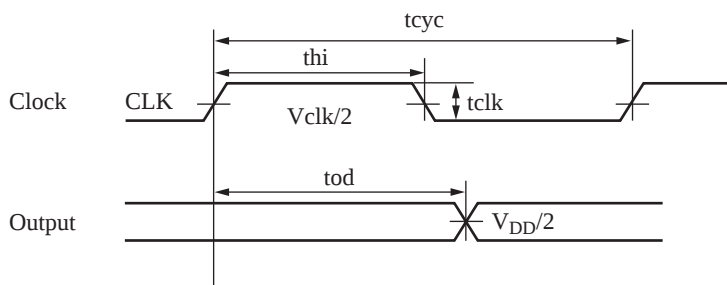


Figure 1. I/O Timing

### 5. A/D Converter

$V_{DD} = TGV_{DD} = OSCV_{DD} = 3.3\text{ V}$ ,  $ADV_{DD} = DAV_{DD} = 3.3\text{ V}$ ,  $V_{SS} = TGV_{SS} = OSCV_{SS} = ADV_{SS} = DAV_{SS} = 0\text{ V}$ ,  
 $T_a = 25^\circ\text{C}$

Pins: VIN, VREFH, VREFL, VREFM, VREFML, and VREFHM

| Item                                           | Symbol     | Condition | Min   | Typ | Max   | Unit     |
|------------------------------------------------|------------|-----------|-------|-----|-------|----------|
| A/D Converter Recommended Operating Conditions |            |           |       |     |       |          |
| Analog input voltage                           | $V_{AIN}$  | VIN       | VREFL | —   | VREFH | V        |
| Analog input pin capacitance                   | $C_{AI}$   | VIN       | —     | 330 | —     | pF       |
| Reference voltage high level                   | $V_{REFH}$ | VREFH     | —     | 2.5 | —     | V        |
| Reference voltage low level                    | $V_{REFL}$ | VREFL     | —     | 0.5 | —     | V        |
| Reference resistor (VREFL–VREFH)               | $R_{REF}$  |           | —     | 440 | —     | $\Omega$ |

#### A/D converter characteristics

|                                 |           |                                                        |   |           |                       |        |
|---------------------------------|-----------|--------------------------------------------------------|---|-----------|-----------------------|--------|
| Resolution                      | $R_{ES}$  |                                                        | — | —         | 10                    | bit    |
| Nonlinearity error              | NLE       | $F_{ADCK} = 20\text{ MHz}$                             | — | $\pm 5.0$ | $\pm 7.5$             | LSB    |
| Differential nonlinearity error | DNLE      | $V_{REFH} = 2.5\text{ V}$<br>$V_{REFL} = 0.5\text{ V}$ | — | $\pm 2.0$ | $\pm 6.5$             | LSB    |
| Analog input dynamic range      | $V_{AIN}$ |                                                        | — | —         | $V_{REFH} - V_{REFL}$ | V[p-p] |

## 6. D/A Converter

$V_{DD} = TGV_{DD} = OSCV_{DD} = 3.3\text{ V}$ ,  $ADV_{DD} = DAV_{DD} = 3.3\text{ V}$ ,  $V_{SS} = TGV_{SS} = OSCV_{SS} = ADV_{SS} = DAV_{SS} = 0\text{ V}$ ,  
 $T_a = 25^\circ\text{C}$

## 1) Pins: VREF23, IREF23, COMP23, BSIG, and RSIG

| Item                                           | Symbol     | Condition                                                                       | Min | Typ  | Max       | Unit          |
|------------------------------------------------|------------|---------------------------------------------------------------------------------|-----|------|-----------|---------------|
| D/A Converter Recommended Operating Conditions |            |                                                                                 |     |      |           |               |
| Reference voltage                              | $V_{REF}$  | $R_L = 75\ \Omega$<br>$R_{IREF23} = 820\ \Omega$                                | —   | 1.37 | —         | V             |
| External phase assurance capacitor             | $C_{COMP}$ | Connect between the COMP23 pin and $AV_{DD}$ .                                  | —   | 1.0  | —         | $\mu\text{F}$ |
| External output resistors                      | $R_L$      | Connect these between the BSIG and RSIG pins respectively, and $AV_{SS}$ .      | —   | 75   | —         | $\Omega$      |
| External bias current setting resistor         | $R_{IREF}$ | Connect between the IREF23 pin and $AV_{SS}$ .                                  | —   | 820  | —         | $\Omega$      |
| D/A converter characteristics                  |            |                                                                                 |     |      |           |               |
| Resolution                                     | $R_{ES}$   |                                                                                 | —   | —    | 8         | bit           |
| Nonlinearity error                             | INLE       | $R_L = 75\ \Omega$<br>$V_{REF23} = 1.37\text{ V}$<br>$R_{IREF23} = 820\ \Omega$ | —   | —    | $\pm 2.5$ | LSB           |
| Differential nonlinearity error                | DNLE       |                                                                                 | —   | —    | $\pm 2.5$ | LSB           |
| Full-scale voltage                             | $V_{OFS}$  |                                                                                 | —   | 1.0  | —         | V             |
| Zero-scale voltage                             | $V_{OZS}$  |                                                                                 | —   | 0    | —         | V             |

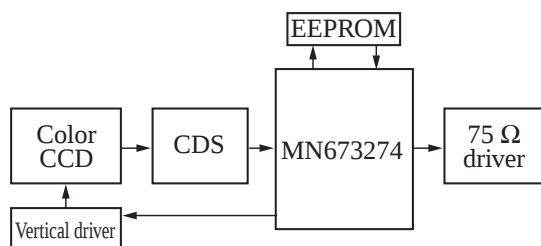
## 2) Pins: VREF1, IREF1, COMP1, and GSIG

| Item                                           | Symbol     | Condition                                                                            | Min | Typ  | Max       | Unit             |
|------------------------------------------------|------------|--------------------------------------------------------------------------------------|-----|------|-----------|------------------|
| D/A Converter Recommended Operating Conditions |            |                                                                                      |     |      |           |                  |
| Reference voltage                              | $V_{REF}$  | $R_L = 75\ \Omega$<br>$R_{IREF1} = 1.13\text{ k}\Omega$                              | —   | 1.5  | —         | V                |
| External phase assurance capacitor             | $C_{COMP}$ | Connect between the COMP1 pin and $AV_{DD}$ .                                        | —   | 1.0  | —         | $\mu\text{F}$    |
| External output resistors                      | $R_L$      | Connect between the GSIG pin and $AV_{SS}$ .                                         | —   | 75   | —         | $\Omega$         |
| External bias current setting resistor         | $R_{IREF}$ | Connect between the IREF1 pin and $AV_{SS}$ .                                        | —   | 1.13 | —         | $\text{k}\Omega$ |
| D/A converter characteristics                  |            |                                                                                      |     |      |           |                  |
| Resolution                                     | $R_{ES}$   |                                                                                      | —   | —    | 10        | bit              |
| Nonlinearity error                             | INLE       | $R_L = 75\ \Omega$<br>$V_{REF1} = 1.5\text{ V}$<br>$R_{IREF1} = 1.13\text{ k}\Omega$ | —   | —    | $\pm 2.5$ | LSB              |
| Differential nonlinearity error                | DNLE       |                                                                                      | —   | —    | $\pm 2.5$ | LSB              |
| Full-scale voltage                             | $V_{OFS}$  |                                                                                      | —   | 1.0  | —         | V                |
| Zero-scale voltage                             | $V_{OZS}$  |                                                                                      | —   | 0    | —         | V                |

## ■ Application System Examples

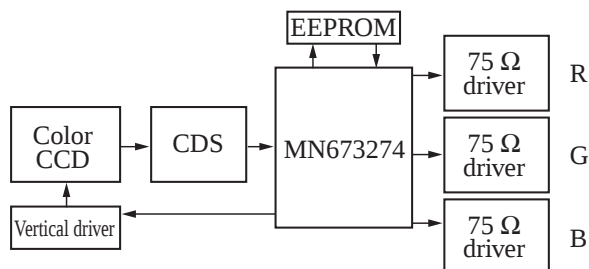
### 1. Example A (Minimum configuration)

- Internal synchronization
- Composite video output



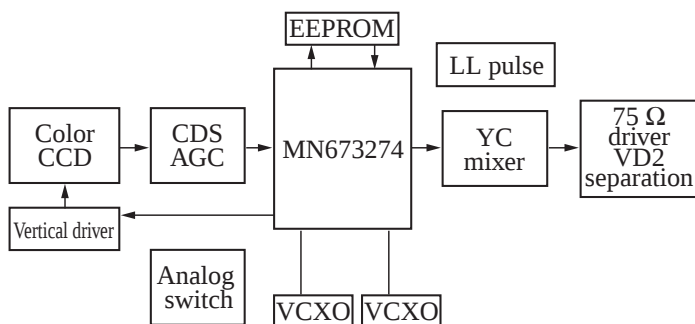
### 2. Example C

- Internal synchronization
- RGB output



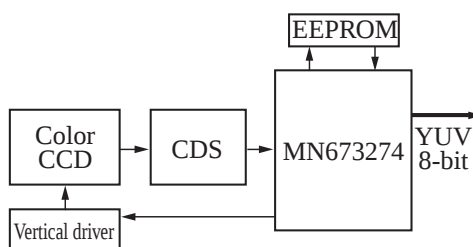
### 3. Example D (Surveillance camera)

- External synchronization
- YC output



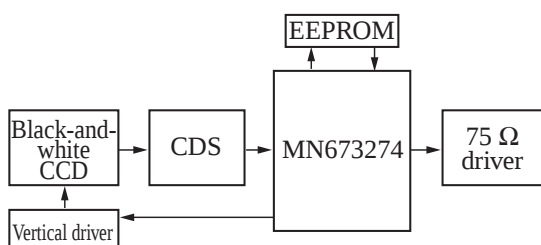
### 4. Example E (PC camera)

- Internal synchronization
- Digital output



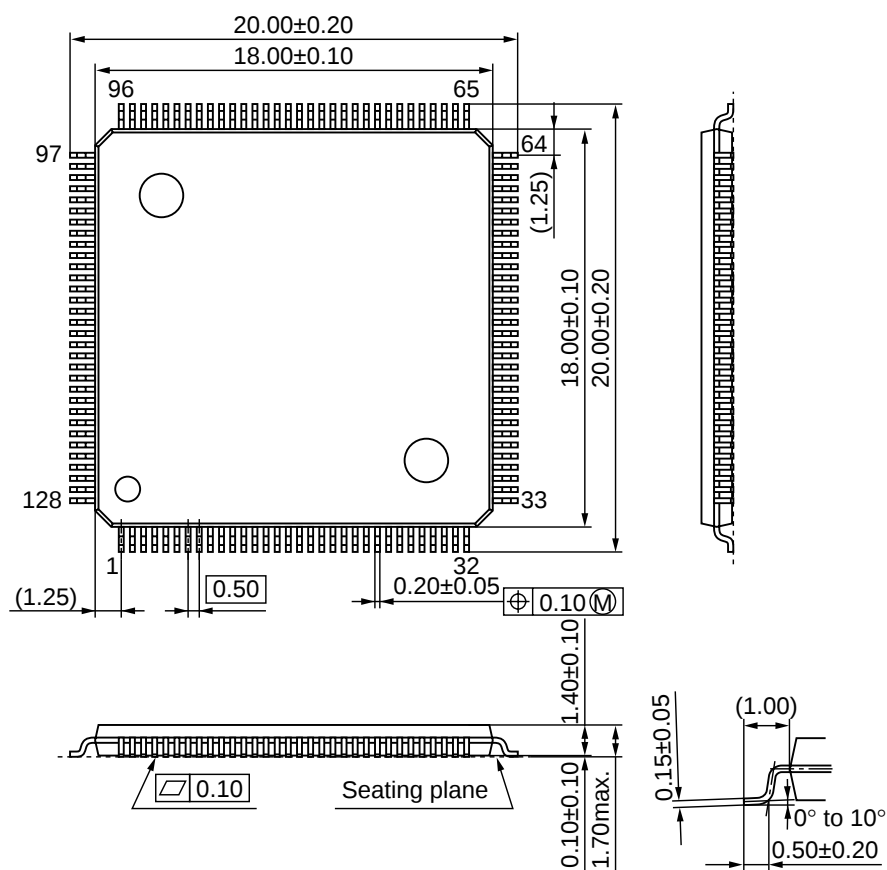
### 5. Example F

- Internal synchronization
- Y output



■ Package Dimensions (units: mm)

- LQFP128-P-1818C



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