

# HIGH SPEED COUPLER

## 6N135, 6N136 INFRARED LED + PHOTO IC

The 6N135 and 6N136 consist of a high emitting diode and a one chip photo diode-transistor. Each unit is an 8-lead DIP package.

### APPLICATIONS

- DIGITAL LOGIC ISOLATION
- LINE RECEIVER
- POWER SUPPLY CONTROL
- SWITCHING POWER SUPPLY
- TRANSISTOR INVERTER

### FEATURES

- High isolation voltage.
- High speed:  $t_{pHL}, t_{pLH} = 0.5\mu s$  (Typ.) ( $R_L = 1.9k\Omega$ ).
- TTL compatible.
- If base pin is open, output signal will be noisy by environmental condition for this case, MT5500 is suitable.
- UL recognized.

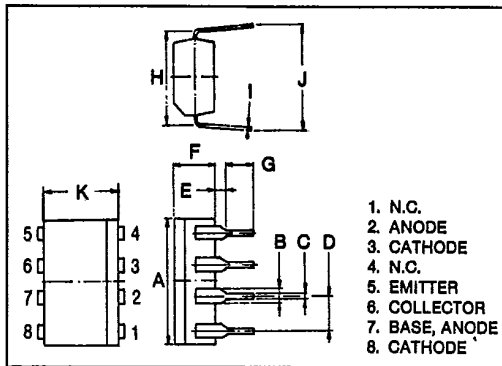
### MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Forward Current (Note 1)	$I_F$	25	mA
Pulse Forward Current (Note 2)	$I_{FP}$	50	mA
Total Pulse Forward Current (Note 3)	$I_{FPT}$	1	A
Reverse Voltage	$V_R$	5	V
Diode Power Dissipation (Note 4)	$P_D$	45	mW
Output Current	$I_O$	8	mA
Peak Output Current	$I_{OP}$	16	mA
Emitter-Base Reverse Voltage (Pin 5-7)	$V_{EB}$	5	V
Supply Voltage	$V_{CC}$	-0.5 ~ 15	V
Output Voltage	$V_O$	-0.5 ~ 15	V
Base Current (Pin 7)	$I_B$	5	mA
Output Power Dissipation (Note 5)	$P_O$	100	mW
Operating Temperature Range	$T_{opr}$	-55 ~ 100	$^\circ C$
Storage Temperature Range	$T_{stg}$	-55 ~ 125	$^\circ C$
Isolation Voltage (Note 6)	$BV_S$	2500	$V_{rms}$

Note 1: Derate 0.8mA above 70°C.  
 Note 2: 50% duty cycle, 1ms pulse width. Derate 1.6mA/°C above 70°C.  
 Note 3: Pulse width 1μs, 300pps.  
 Note 4: Derate 0.9mW/°C above 70°C.  
 Note 5: Derate 2mW/°C above 70°C.  
 Note 6: R.H.=40~60%, AC/1 min.

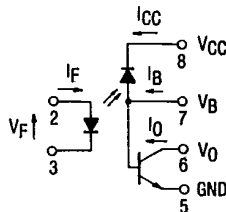
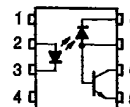
A - LED B - DETECTOR

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SYMBOL	INCHES	MM
A	0.380 ± 0.010	9.66 ± 0.25
B	0.047	1.2
C	0.020	0.5
D	0.100 ± 0.010	2.54 ± 0.25
E	0.031	0.8
F	0.144	3.65
G	0.098	2.5
H	0.300 ± 0.010	7.62 ± 0.25
I	0.010 $\begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$	0.25 $\begin{smallmatrix} +0.1 \\ -0.06 \end{smallmatrix}$
J	0.309 ~ 0.346	7.85 ~ 8.80
K	0.252	6.4

PIN CONFIGURATIONS  
(TOP VIEW)



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**OPTO-ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEMPERATURE ( $T_a = 0^\circ\text{C} - 70^\circ\text{C}$  Unless otherwise noted)**

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CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP**	MAX.	UNIT
Current Transfer Ratio	6N135	$I_F = 16\text{mA}$ , $V_O = 0.4\text{V}$	7	18	—	%
	6N136	$V_{CC} = 4.5\text{V}$ , $T_a = 25^\circ\text{C}$ (Note 1)	19	24	—	%
	6N135	$I_F = 16\text{mA}$ , $V_O = 0.5\text{V}$	5	13	—	%
	6N136	$V_{CC} = 4.5\text{V}$ (Note 1)	15	21	—	%
Logic Low Output Voltage	6N135	$I_F = 16\text{mA}$ , $I_O = 1.1\text{mA}$ , $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
	6N136	$I_F = 16\text{mA}$ , $I_O = 2.4\text{mA}$ , $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
Logic High Output Current	$I_{OH}$	$I_F = 0\text{mA}$ , $V_O = V_{CC} = 5.5\text{V}$ $T_a = 25^\circ\text{C}$	—	3	500	nA
		$I_F = 0\text{mA}$ , $V_O = V_{CC} = 15\text{V}$ $T_a = 25^\circ\text{C}$	—	0.1	100	$\mu\text{A}$
	$I_{OH}$	$I_F = 0\text{mA}$ , $V_O = V_{CC} = 15\text{V}$	—	—	250	$\mu\text{A}$
Logic Low Supply Current	$I_{CCL}$	$I_F = 16\text{mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{V}$	—	40	—	$\mu\text{A}$
Logic High Supply Current	$I_{CCH}$	$I_F = 0\text{mA}$ , $V_O = \text{Open}$ $V_{CC} = 15\text{V}$ , $T_a = 25^\circ\text{C}$	—	0.01	1	$\mu\text{A}$
	$I_{CCH}$	$I_F = 0\text{mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{V}$	—	—	2	$\mu\text{A}$
Input Forward Voltage	$V_F$	$I_F = 16\text{mA}$ , $T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_a}$	$I_F = 16\text{mA}$	—	-1.9	—	mV/°C
Input Reverse Breakdown Voltage	$BV_R$	$I_R = 10\mu\text{A}$ , $T_a = 25^\circ\text{C}$	5	—	—	V
Input Capacitance	$C_{IN}$	$f = 1\text{MHz}$ , $V_F = 0$	—	60	—	pF
Input-Output Insulation Leakage Current	$I_{I-O}$	45% Relative Humidity, $t = 5\text{s}$ , $V_{I-O} = 3000\text{Vdc}$ , $T_a = 25^\circ\text{C}$ (Note 2)	—	—	1.0	$\mu\text{A}$
Resistance (Input-Output)	$R_{I-O}$	$V_{I-O} = 500\text{Vdc}$ (Note 2)	—	$10^{12}$	—	$\Omega$
Capacitance (Input-Output)	$C_{I-O}$	$f = 1\text{MHz}$ (Note 2)	—	0.6	—	pF
Transistor DC Current Gain	$h_{FE}$	$V_O = 5\text{V}$ , $I_O = 3\text{mA}$	—	80	—	—

\*\*All typicals at  $T_a = 25^\circ\text{C}$ .

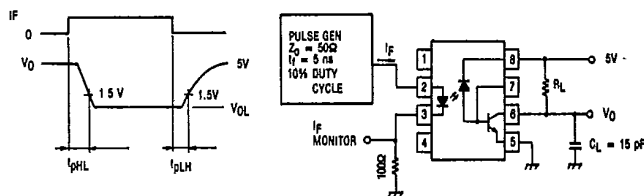
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## SWITCHING CHARACTERISTICS (Ta = 25°C, VCC = 5V, IF = 16mA Unless otherwise noted)

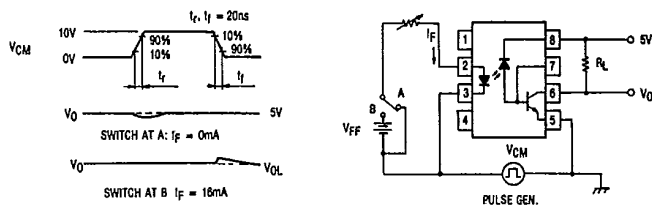
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output	6N135	1	RL = 4.1kΩ	—	0.2	1.5	μs
	6N136		RL = 1.9kΩ	—	0.2	0.8	μs
Propagation Delay Time to Logic High at Output	6N135	1	RL = 4.1kΩ	—	1.0	1.5	μs
	6N136		RL = 1.9kΩ	—	0.5	0.8	μs
Common Mode Transient Immunity at Logic High Level Output (Note 3)	6N135	2	IF = 0mA, VCM = 10Vp-p RL = 4.1kΩ	—	1000	—	V/μs
	6N136		IF = 0mA, VCM = 10Vp-p RL = 1.9kΩ	—	1000	—	V/μs
Common Mode Transient Immunity at Logic Low Level Output (Note 3)	6N135	2	IF = 16mA, VCM = 10Vp-p RL = 4.1kΩ	—	-1000	—	V/μs
	6N136		IF = 16mA, VCM = 10Vp-p RL = 1.9kΩ	—	-1000	—	V/μs
Bandwidth (Note 4)	BW	—	RL = 100Ω	—	2	—	MHz

Note 1: DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current,  $I_O$ , to the forward LED Input current,  $I_F$ , times 100%.  
 Note 2: Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.  
 Note 3: Common mode transient immunity in Logic High level is the maximum tolerable (Positive)  $dV_{cm}/dt$  on the leading edge of the common mode pulse,  $V_{cm}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 2.0V$ ). Common mode transient immunity in Logic Low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{cm}$ , to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 0.8V$ ).  
 Note 4: The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

TEST CIRCUIT 1.



TEST CIRCUIT 2



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