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# 12-Bit, 105/125 MSPS IF Sampling A/D Converter

## Preliminary Technical Data

AD9433

### FEATURES

**IF Sampling up to 400MHz**  
**IF Mode select for optimized SINAD and SFDR**  
**On Chip Clock Duty Cycle Stabilization**  
**On-chip reference and track/hold**  
**SFDR Optimization circuit**  
**Excellent Linearity:**  
 - DNL = +/- 0.25 lsb (typ)  
 - INL = +/- 0.5 lsb (typ)  
**750 MHz Full Power Analog Bandwidth**  
**SNR = 67dB @ Fin up to Nyquist**  
**SFDR = 85dBc @ Fin up to 125 MHz**  
**SFDR = 80dBc @ Fin up to 250 MHz**  
**THD = 90dBc @ Fin up to 250 MHz**  
**Power dissipation = 1.3W typical at 125MSPs**  
**Input voltage of 1Vp-p or 2Vp-p**  
**Two's complement or Offset binary data format**  
**+5.0V Analog Supply Operation**  
**+2.5V to 3.3V TTL/CMOS outputs.**

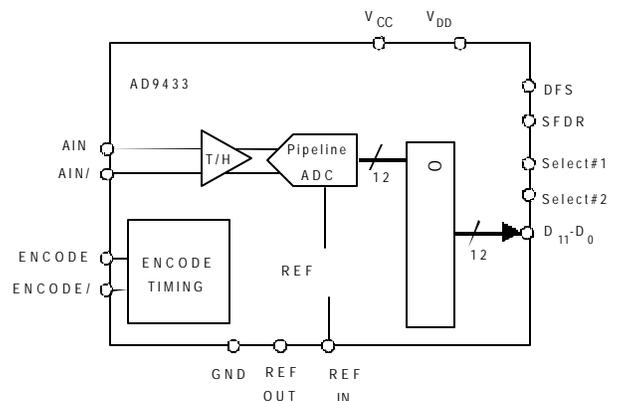
### APPLICATIONS

**Wireless and Wired Broadband Communications**  
 - Wideband carrier frequency systems  
**Communications Test Equipment**  
 "IF Sampling" schemes  
**Radar and Satellite sub-systems**

### GENERAL INTRODUCTION

The AD9433 is a 12-bit monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and is designed for ease of use. The product operates up to 125 Msp/s conversion rate and is optimized for outstanding dynamic performance in wideband and high IF carrier systems.

The ADC requires a +5V analog power supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3V or 2.5V logic.



AD9433 FUNCTIONAL BLOCK DIAGRAM

A user selectable on-chip circuit optimizes SFDR performance of 90dBc from DC to 70MHz. A user select allows optimized SINAD vs SFDR for a particular input frequency range.

The encode clock supports either differential or single-ended input and is PECL compatible and an output data format select option of two's complement or offset binary are also supported.

Fabricated on an advanced BiCMOS process, the AD9433 is available in a 52 pin surface mount plastic package (52 LQFP) specified over the industrial temperature range (-40°C to +85°C) and is pin compatible with the AD9432.

# PRELIMINARY TECHNICAL DATA

## AD9433

### DC SPECIFICATIONS (V<sub>DD</sub> = 3.3 V, V<sub>CC</sub> = 5.0 V; external reference; differential encode input, unless otherwise noted)

| Parameter   | Temp | Test Level | AD9433-105 |       |      | AD9433-125 |      |      | Unit   |
|---|------|------------|------------|-------|------|------------|------|------|--------|
|   |      |            | Min        | Typ   | Max  | Min        | Typ  | Max  |        |
| RESOLUTION  |      |            | 12         |       |      | 12         |      |      | Bits   |
| ACCURACY  |      |            | Guaranteed |       |      | Guaranteed |      |      |        |
| No Missing Codes  | Full | VI         |            |       |      |            |      |      |        |
| Offset Error  | Full | VI         | -5         | 0     | +5   | -5         | 0    | +5   | mV     |
| Gain Error <sup>1</sup>   | 25°C | I          | ±1         |       |      | ±1         |      |      | % FS   |
| Differential Nonlinearity (DNL)                                       | 25°C | I          | -0.6       | ±0.25 | +0.6 | -0.6       | ±0.3 | +0.6 | LSB    |
|   | Full | VI         |            |       |      |            |      |      |        |
| Integral Nonlinearity (INL)   | 25°C | I          | ±0.5       |       |      | ±0.5       |      |      | LSB    |
|   | Full | VI         |            |       |      |            |      |      |        |
| REFERENCE   |      |            |            |       |      |            |      |      |        |
| Internal Reference Voltage (VREFOUT)                                  | 25°C | I          | 2.4        | 2.5   | 2.6  | 2.4        | 2.5  | 2.6  | V      |
| Output Current (VREFOUT)  | Full | V          |            |       |      |            |      |      | uA     |
| Input Current (VREFIN)  | Full | V          |            |       |      |            |      |      | uA     |
| Input Resistance (VREFIN)   | Full | V          |            |       |      |            |      |      | kΩ     |
| ANALOG INPUTS   |      |            |            |       |      |            |      |      |        |
| Differential Input Voltage Range (A <sub>IN</sub> , A <sub>IN</sub> ) |      |            |            |       |      |            |      |      |        |
| Baseband, IF Sampling I Modes   | Full | V          | 2.0        |       |      | 2.0        |      |      | V      |
| IF Sampling II Mode   | Full | V          | 1.0        |       |      | 1.0        |      |      | V      |
| Common Mode Voltage   | Full | V          | 4.0        |       |      | 4.0        |      |      | V      |
| Input Resistance  | Full | V          | 2          | 3     | 4    | 3          |      |      | kΩ     |
| Input Capacitance   | Full | V          | 3          |       |      | 3          |      |      | pF     |
| Analog Bandwidth, Full Power  | Full | V          | 750        |       |      | 750        |      |      | MHz    |
| TEMPERATURE DRIFT   |      |            |            |       |      |            |      |      |        |
| Offset Error  | Full | V          |            |       |      |            |      |      | ppm/°C |
| Gain Error <sup>1</sup>   | Full | V          | 150        |       |      | 150        |      |      | ppm/°C |
| Reference   | Full | V          | 50         |       |      | 50         |      |      | ppm/°C |
| SWITCHING PERFORMANCE   |      |            |            |       |      |            |      |      |        |
| Encode Rate   | Full | VI         | 1          | 105   |      | 1          | 125  |      | MspS   |
| Encode Pulse Width High (t <sub>EH</sub> )                            | Full | VI         | 2.9        | 6.7   |      | 2.4        | 5.6  |      | ns     |
| Encode Pulse Width Low (t <sub>EL</sub> )                             | Full | VI         | 2.9        | 6.7   |      | 2.4        | 5.6  |      | ns     |
| Aperture Delay (t <sub>A</sub> )                                      | 25°C | V          |            |       |      |            |      |      | ns     |
| Aperture Uncertainty (Jitter)   | 25°C | V          | 0.25       |       |      | 0.25       |      |      | ps rms |
| Output Valid Time (t <sub>V</sub> ) <sup>2</sup>                      | Full | VI         | 4.0        |       |      | 4.0        |      |      | ns     |
| Output Propagation Delay (t <sub>PD</sub> ) <sup>2</sup>              | Full | VI         | 4.0        |       |      | 4.0        |      |      | ns     |
| Output Rise Time (t <sub>R</sub> )                                    | Full | V          | 2.1        |       |      | 2.1        |      |      | ns     |
| Output Fall Time (t <sub>F</sub> )                                    | Full | V          | 1.9        |       |      | 1.9        |      |      | ns     |
| Out of Range Recovery Time  | 25°C | V          | 2          |       |      | 2          |      |      | ns     |
| Transient Response Time   | 25°C | V          | 2          |       |      | 2          |      |      | ns     |
| Latency   | Full | IV         | 10         |       |      | 10         |      |      | Cycles |
| DIGITAL INPUTS  |      |            |            |       |      |            |      |      |        |
| Encode Input Common Mode  | Full | V          | 3.75       |       |      | 3.75       |      |      | V      |
| Differential Input (ENC – ENC)  | Full | V          | 500        |       |      | 500        |      |      | mV     |
| Input Voltage Range   | Full | IV         | -0.5       |       |      | -0.5       |      |      | V      |
| Input Resistance  | Full | VI         | 6          |       |      | 6          |      |      | kΩ     |
| Input Capacitance   | 25°C | V          | 3          |       |      | 3          |      |      | pF     |
| POWER SUPPLY  |      |            |            |       |      |            |      |      |        |
| V <sub>CC</sub>   | Full | IV         | 4.75       | 5.0   | 5.25 | 4.75       | 5.0  | 5.25 | V      |
| V <sub>DD</sub>   | Full | IV         | 2.7        | 3.3   |      | 2.7        | 3.3  |      | V      |
| Power Dissipation <sup>3</sup>  | Full | VI         | 1250       |       |      | 1350       |      |      | mW     |
| Power Supply Rejection Ratio (PSRR)                                   | 25°C | I          | ±5         |       |      |            |      |      | mV/V   |
| IV <sub>CC</sub> <sup>3</sup>   | Full | VI         | 250        |       |      | 270        |      |      | mA     |
| IV <sub>DD</sub> <sup>3</sup>   | Full | VI         | 12.5       |       |      | 16         |      |      | mA     |

# PRELIMINARY TECHNICAL DATA

## AD9433

### DC SPECIFICATIONS continued (V<sub>DD</sub> = 3.3 V, V<sub>CC</sub> = 5.0 V; external reference; differential encode input, unless otherwise noted)

| Parameter         | Temp | Test Level | AD9433-105                       |     |     | AD9433-125            |     |     | Unit |
|-------------------|------|------------|----------------------------------|-----|-----|-----------------------|-----|-----|------|
|                   |      |            | Min                              | Typ | Max | Min                   | Typ | Max |      |
| DIGITAL OUPUTS    |      |            |                                  |     |     |                       |     |     |      |
| Logic "1" Voltage | Full | VI         | V <sub>DD</sub> -0.05            |     |     | V <sub>DD</sub> -0.05 |     |     | V    |
| Logic "0" Voltage | Full | VI         | 0.05                             |     |     | 0.05                  |     |     | V    |
| Output Coding     |      |            | Twos Compliment or Offset Binary |     |     |                       |     |     |      |

### AC SPECIFICATIONS (V<sub>DD</sub> = 3.3 V, V<sub>CC</sub> = 5.0 V; internal reference; differential encode input, unless otherwise noted)

| Parameter  | Temp | Test Level | AD9433-105 |     |     | AD9433-125 |     |     | Units |
|--|------|------------|------------|-----|-----|------------|-----|-----|-------|
|  |      |            | Min        | Typ | Max | Min        | Typ | Max |       |
| DYNAMIC PERFORMANCE <sup>4</sup>   |      |            |            |     |     |            |     |     |       |
| Signal to Noise Ratio (SNR)<br>(Without Harmonics)                             |      |            | Guaranteed |     |     | Guaranteed |     |     |       |
| f <sub>IN</sub> =10.3MHz   | 25°C | I          | 68.0       |     |     | 67.5       |     |     | dB    |
| f <sub>IN</sub> =49MHz   | 25°C | I          | 66.8       |     |     | 65.0       |     |     | dB    |
| f <sub>IN</sub> =70MHz   | 25°C | I          | 67.0       |     |     | 64.5       |     |     | dB    |
| f <sub>IN</sub> =150MHz  | 25°C | V          | 65.5       |     |     | 62.0       |     |     | dB    |
| f <sub>IN</sub> =250MHz  | 25°C | V          | 63.5.5     |     |     | 60.0       |     |     | dB    |
| Signal to Noise Ratio (SINAD)<br>(With Harmonics)                              |      |            |            |     |     |            |     |     |       |
| f <sub>IN</sub> =10.3MHz   | 25°C | I          | 67.8       |     |     | 67.2       |     |     | dB    |
| f <sub>IN</sub> =49MHz   | 25°C | I          | 67.2       |     |     | 65.4       |     |     | dB    |
| f <sub>IN</sub> =70MHz   | 25°C | I          | 66.5       |     |     | 63.6       |     |     | dB    |
| f <sub>IN</sub> =150MHz  | 25°C | V          | 65.0       |     |     | 60.0       |     |     | dB    |
| f <sub>IN</sub> =250MHz  | 25°C | V          | 63.0       |     |     | 57.0       |     |     | dB    |
| Effective Number of Bits   |      |            |            |     |     |            |     |     |       |
| f <sub>IN</sub> =10.3MHz   | 25°C | I          | 11.0       |     |     | 10.4       |     |     | Bits  |
| f <sub>IN</sub> =49MHz   | 25°C | I          | 11.0       |     |     | 10.4       |     |     | Bits  |
| f <sub>IN</sub> =70MHz   | 25°C | I          | 10.8       |     |     | 10.2       |     |     | Bits  |
| f <sub>IN</sub> =150MHz  | 25°C | V          | 10.6       |     |     | 9.8        |     |     | Bits  |
| f <sub>IN</sub> =250MHz  | 25°C | V          | 10.2       |     |     | 9.5        |     |     | Bits  |
| 2 <sup>nd</sup> & 3 <sup>rd</sup> Harmonic Distortion(SNR)                     |      |            |            |     |     |            |     |     |       |
| f <sub>IN</sub> =10.3MHz   | 25°C | I          | 85         |     |     | 83         |     |     | dBc   |
| f <sub>IN</sub> =49MHz   | 25°C | I          | 85         |     |     | 80         |     |     | dBc   |
| f <sub>IN</sub> =70MHz   | 25°C | I          | 80         |     |     | 80         |     |     | dBc   |
| f <sub>IN</sub> =150MHz  | 25°C | V          | 80         |     |     | 80         |     |     | dBc   |
| f <sub>IN</sub> =250MHz  | 25°C | V          | 75         |     |     | 75         |     |     | dBc   |
| Worst other Harmonic or Spur<br>(Excluding 2 <sup>nd</sup> & 3 <sup>rd</sup> ) |      |            |            |     |     |            |     |     |       |
| f <sub>IN</sub> =10.3MHz   | 25°C | I          | 90         |     |     | 90         |     |     | dBFS  |
| f <sub>IN</sub> =49MHz   | 25°C | I          | 90         |     |     | 85         |     |     | dBFS  |
| f <sub>IN</sub> =70MHz   | 25°C | I          | 90         |     |     | 85         |     |     | dBFS  |
| f <sub>IN</sub> =150MHz  | 25°C | V          | 90         |     |     | 83         |     |     | dBFS  |
| f <sub>IN</sub> =250MHz  | 25°C | V          | 90         |     |     | 80         |     |     | dBFS  |
| Two Tone Intermod Distortion (IMD)   |      |            |            |     |     |            |     |     |       |
| f <sub>IN1</sub> =29.3MHz, f <sub>IN2</sub> =30.3MHz                           | 25°C | V          |            |     |     |            |     |     | dBc   |
| f <sub>IN1</sub> =150MHz, f <sub>IN2</sub> =151MHz                             | 25°C | V          |            |     |     |            |     |     | dBc   |
| f <sub>IN1</sub> =250MHz, f <sub>IN2</sub> =251MHz                             | 25°C | V          |            |     |     |            |     |     | dBc   |

#### NOTES

- 1 Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5 V external reference and a 2 V p-p differential analog input).
- 2 t<sub>v</sub> and t<sub>pp</sub> are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 mA. Rise and fall times measured from 10% to 90%.
- 3 Power dissipation measured with rated encode and a dc analog input (Outputs Static, I<sub>VDD</sub> = 0.). I<sub>VCC</sub> and I<sub>VDD</sub> measured with 10.3MHz analog input @ 0.5dBFS.
- Typical θ<sub>JA</sub> for LQFP package = 50C/W.
- 4 SNR/harmonics based on an analog input voltage of -0.5 dBFS referenced to a 2 V full-scale input range.

**Specifications subject to change without notice.**

# PRELIMINARY TECHNICAL DATA

## AD9433

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| Parameter                             | Min  | Max                  | Units |
|---------------------------------------|------|----------------------|-------|
| <b>ELECTRICAL</b>                     |      |                      |       |
| V <sub>DD</sub> Voltage               | -0.5 | 6.0                  | V     |
| V <sub>CC</sub> Voltage               | -0.5 | 6.0                  | V     |
| Analog Input Voltage                  | -0.5 | V <sub>CC</sub> +0.5 | V     |
| Analog Input Current                  |      | TBD                  | mA    |
| Digital Input Voltage                 | TBD  | V <sub>CC</sub> +0.5 | V     |
| Digital Output Current                |      | 20                   | mA    |
| <b>ENVIRONMENTAL<sup>6</sup></b>      |      |                      |       |
| Operating Temperature Range (Ambient) | -55  | 125                  | °C    |
| Maximum Junction Temperature          |      | 175                  | °C    |
| Lead Temperature (Soldering, 10 sec)  |      | TBD                  | °C    |
| Maximum Case Temperature              |      | 150                  | °C    |
| Storage Temperature Range (Ambient)   | -65  | 150                  | °C    |

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### EXPLANATION OF TEST LEVELS

#### Test Level

- I 100% production tested.
- II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.
- III Sample Tested Only
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9433 features proprietary protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

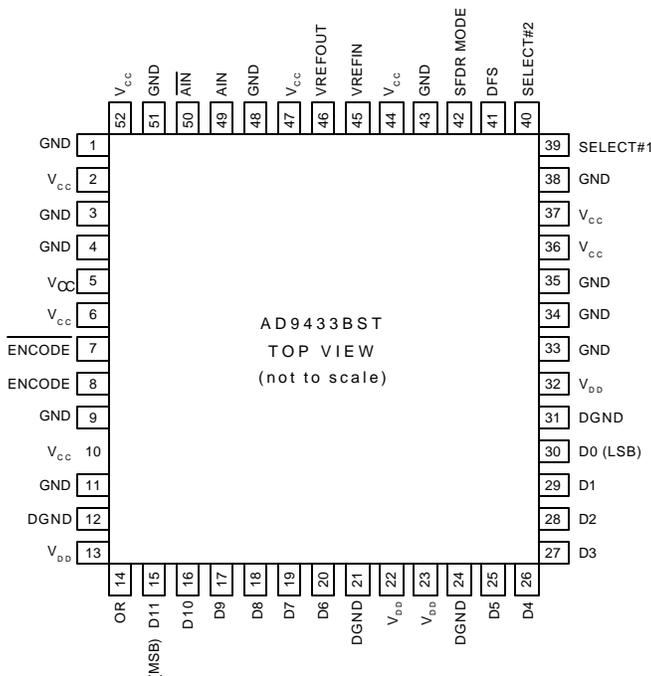


### ORDERING GUIDE

| Model          | Temperature Range        | Package Description              | Package Option |
|----------------|--------------------------|----------------------------------|----------------|
| AD9433BST -105 | -40°C to +85°C (Ambient) | 52-Lead Plastic Quad Flatpack    | ST-52          |
| AD9433BST -125 | -40°C to +85°C (Ambient) | 52-Lead Plastic Quad Flatpack    | ST-52          |
| AD9433/PCB     | +25°C                    | Evaluation Board with AD9433-125 |                |

PIN FUNCTION DESCRIPTIONS

| Pin No.                            | Name      | Function  |
|------------------------------------|-----------|---|
| 1,3,4,9,11,12,33,34,35,38,43,48,51 | GND       | Analog Ground   |
| 2,5,6,10,36,37,44,47,52            | Vcc       | Analog Supply (+5V)   |
| 7                                  | ENCODE    | Encode Clock for ADC – Complementary  |
| 8                                  | ENCODE    | Encode Clock for ADC – True - (ADC samples on rising edge of ENCODE)  |
| 14                                 | OR        | Out of Range Output.  |
| 15-20, 25-30                       | D11-0     | Digital Output  |
| 13,22,23,32                        | Vdd       | Digital Output Power Supply (+3V)   |
| 21,24,31                           | DGND      | Digital Output Ground   |
| 39                                 | SELECT#1  | User select option #1   |
| 40                                 | SELECT#2  | User select option #2   |
| 41                                 | DFS       | Data format select. Low = Two's compliment, High = Binary   |
| 42                                 | SFDR MODE | CMOS control pin that enables (SFDR MODE=1) a proprietary circuit that may improve the spurious free dynamic range (SFDR) performance of the AD9433. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by non-linearities in the ADC transfer function. SFDR MODE=0 for normal operation. |
| 45                                 | VREFIN    | Reference input for ADC (2.5V typical)  |
| 46                                 | VREFOUT   | Internal reference output (2.5V typical); bypass with 0.1uF to Ground.  |
| 49                                 | AIN       | Analog input – True   |
| 50                                 | AIN       | Analog input – Complement   |



PIN CONFIGURATION

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

**DEFINITIONS OF SPECIFICATIONS (cont'd)**

**Differential Analog Input Voltage Range**

The peak to peak differential voltage that must be applied to the converter to generate a fullscale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak to peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

**Differential Nonlinearity**

The deviation of any code width from an ideal 1 LSB step.

**Effective Number of Bits**

The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76dB + 20 \log \left( \frac{FullScale\_Amplitude}{Input\_Amplitude} \right)}{6.02}$$

**Encode Pulse Width/Duty Cycle**

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic “1” state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t<sub>ENCH</sub> in text. At a give clock rate, these specs define an acceptable Encode duty cycle.

**Fullscale Input Power**

Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10 \log \left( \frac{\frac{V_{Fullscale_{rms}}^2}{Z_{Input}}}{.001} \right)$$

**Gain**

Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

**Harmonic Distortion, 2<sup>nd</sup>**

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

**Harmonic Distortion, 3<sup>rd</sup>**

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

**Integral Nonlinearity**

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

**Minimum Conversion Rate**

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

**Maximum Conversion Rate**

The maximum encode rate at which parametric testing is performed.

**Output Propagation Delay**

The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

**Noise (for any range within the ADC)**

$$V_{noise} = \sqrt{Z * .001 * 10^{\left( \frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}}$$

Where Z is the input impedance, FS is the fullscale of the device for the frequency in question, SNR is the value for the particular input level and Signal is the signal level within the ADC reported in dB below fullscale. This value includes both thermal and quantization noise.

**Power Supply Rejection Ratio**

The ratio of a change in input offset voltage to a change in power supply voltage.

**Signal-to-Noise-and-Distortion (SINAD)**

The ratio of the rms signal amplitude (set 1dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

**Signal-to-Noise Ratio (without Harmonics)**

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

**Spurious-Free Dynamic Range (SFDR)**

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e. degrades as signal level is lowered), or dBFS (always related back to converter full scale).

**Two-Tone Intermodulation Distortion Rejection**

The ratio of the rms value of either input tone (f1, f2) to the rms value of the worst third order intermodulation product; reported in dBc. Products are located at 2f1-f2 and 2f2-f1.

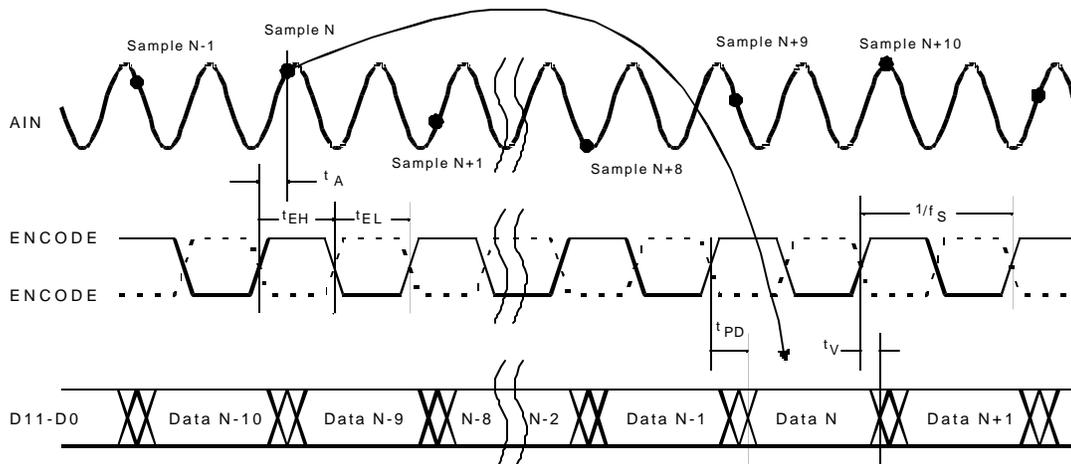
**Two-Tone SFDR**

The ratio of the rms value of either input tone (f1, f2) to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e. degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

**Worst Other Spur**

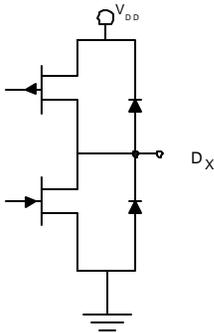
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic) reported in dBc.

**Timing Diagram**

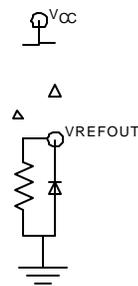


**AD9433 Timing Diagram**

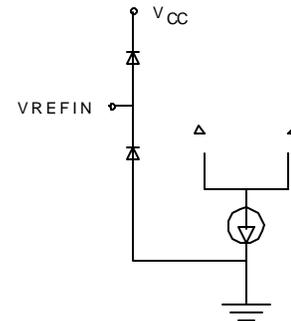
**Equivalent Circuits**



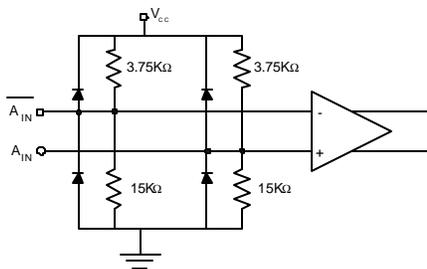
*Figure TBD. Digital Output*



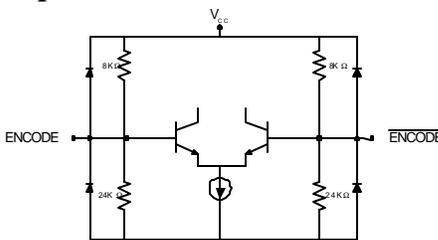
*Figure TBD. Reference Output*



*Figure TBD. Reference Input*

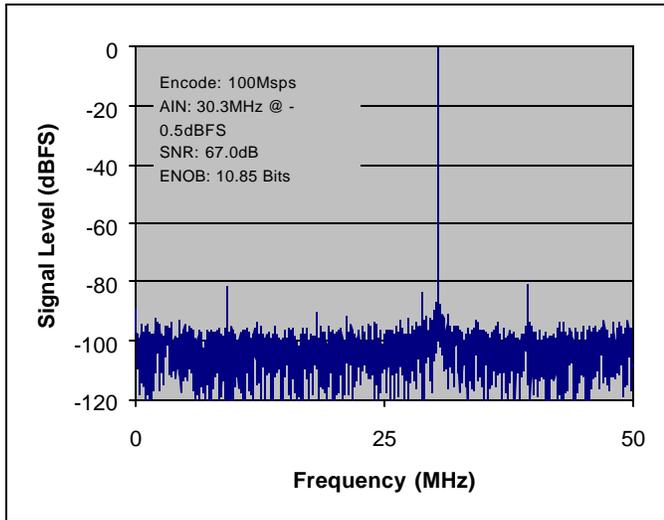


*Figure TBD. Analog Input*

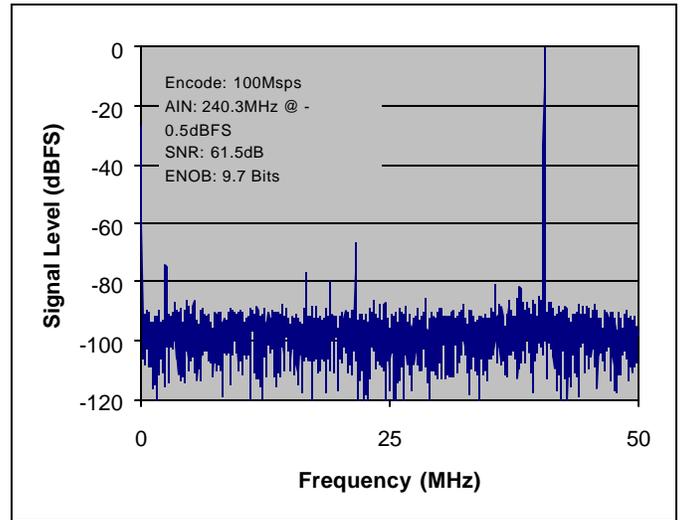


*Figure TBD. Encode Inputs*

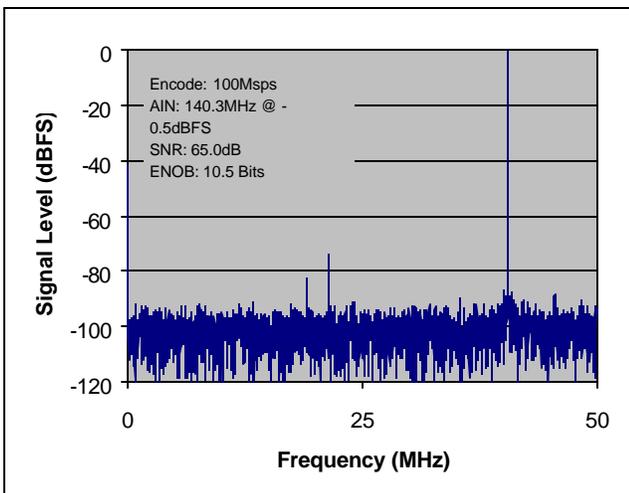
TYPICAL PERFORMANCE CURVES



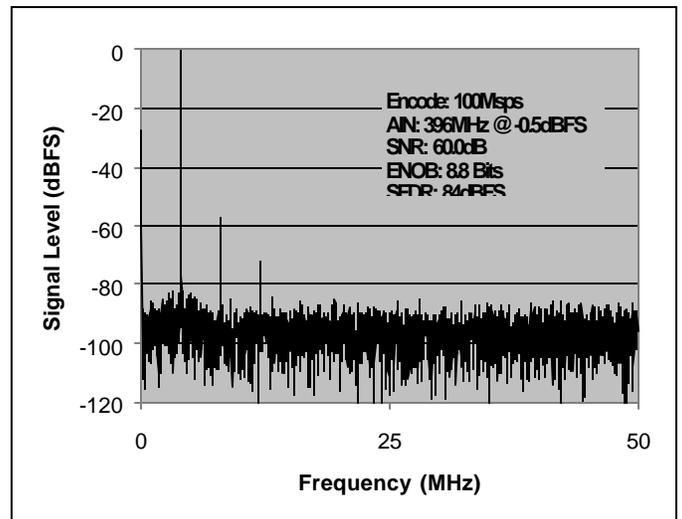
*FFT: 100MSPS, 30.3MHz @ -0.5dBFS, Baseband Mode, SFDR MODE Enabled*



*FFT: 100MSPS, 240.3MHz @ -0.5dBFS, IF II Mode, SFDR MODE Enabled*



*FFT: 100MSPS, 140.3MHz @ -0.5dBFS, IF I Mode, SFDR MODE Enabled*



*FFT: 100MSPS, 396MHz @ -0.5dBFS, IF II Mode, SFDR MODE Enabled*

**Theory of Operation**

The AD9433 is a multibit pipeline converter that uses a switched capacitor architecture. Optimized for high speed, this converter provides flat dynamic performance up to and beyond the Nyquist limit. DNL transitional errors are calibrated at final test to a typical accuracy of 0.25 LSB or less.

**USING THE AD9433**

**ENCODE Input**

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9433, and the user is advised to give commensurate thought to the clock source.

The AD9433 has an internal clock duty cycle stabilization circuit that locks to the rising edge of ENCODE (falling edge of ENCODE if driven differentially), and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern, and is not reduced by the internal stabilization circuit.

The ENCODE and ENCODE inputs are internally biased to 3.75V (nominal), and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. Good performance is obtained using an MC10EL16 in the circuit to directly drive the encode inputs, as illustrated in Fig. TBD.

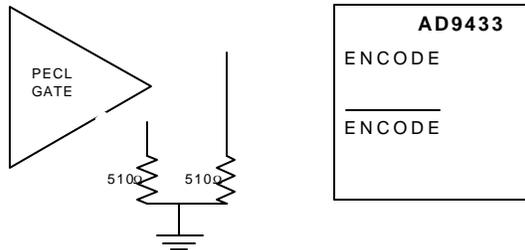


Figure TBD. Using PECL to drive the ENCODE Inputs

Often, the cleanest clock source is a crystal oscillator producing a pure, single ended sine wave. In this configuration, or with any roughly symmetrical, single ended clock source, the signal can be ac-coupled to the ENCODE input. To minimize jitter, the signal amplitude should be maximized within the input range described in Table TBD. The ENCODE input should be bypassed with a capacitor to ground to reduce noise. This ensures that the internal bias voltage is centered on the encode signal. For best dynamic performance, impedances at ENCODE and ENCODE should match.

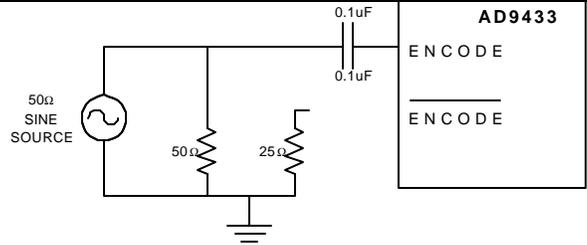


Figure TBD. Single ended 50 Sine Source Encode Circuit

**ENCODE Voltage Level Definition**

The voltage level definitions for driving ENCODE and ENCODE in single-ended and differential mode are shown in Figure TBD.

ENCODE Inputs

| Description  | Minimum | Nominal | Maximum       |
|--|---------|---------|---------------|
| Differential Signal Amplitude ( $V_{ID}$ )                   | 200mV   | 750mV   | 5.5V          |
| Input Voltage Range ( $V_{IHD}, V_{ILD}, V_{IHS}, V_{ILS}$ ) | -0.5V   |         | $V_{CC}+0.5V$ |
| Internal Common Mode Bias ( $V_{ICM}$ )                      |         | 3.75 V  |               |
| External Common Mode Bias ( $V_{ECM}$ )                      | 2.5V    |         | 4.5V          |

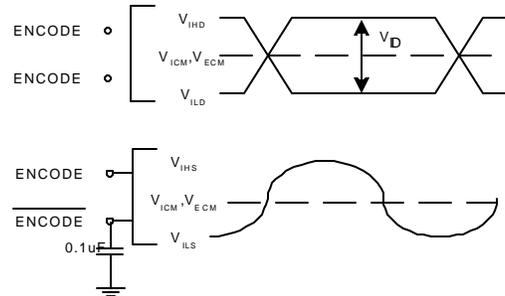


Figure TBD. Differential and Single Ended Input Levels

**Analog Input**

The dynamic performance of the AD9433 can be optimized for different signal bandwidths by configuring the mode of the analog input circuit. CMOS inputs SELECT#1 and SELECT#2 optimize performance and analog input voltage swing as defined in the table below.

Table X. Setting the Analog Input Circuit Mode

| Mode           | Differential Analog Input Range (V) | Optimized Analog Bandwidth (MHz) | SELECT #1 (Pin 39) | SELECT #2 (Pin 40) |
|----------------|-------------------------------------|----------------------------------|--------------------|--------------------|
| IF Sampling I  | 2Vp-p                               | 100 - 250                        | 0                  | 0                  |
| IF Sampling II | 1Vp-p                               | 250 - 350                        | 1                  | 1                  |
| Baseband       | 2Vp-p                               | DC to 100                        | 0                  | 1                  |

In all modes, the analog input to the AD9433 is a differential buffer. The input buffer is self-biased by an on-chip resistor divider that sets the dc common-mode voltage to a nominal 4V (see Equivalent Circuits section). Rated performance is achieved by driving the input differentially. Minimum input offset voltage is obtained when driving from a source with a low differential source impedance such as a transformer in ac applications (See figure TBD). Capacitive coupling at the inputs will increase the input offset voltage by as much as  $\pm 25$  mV.

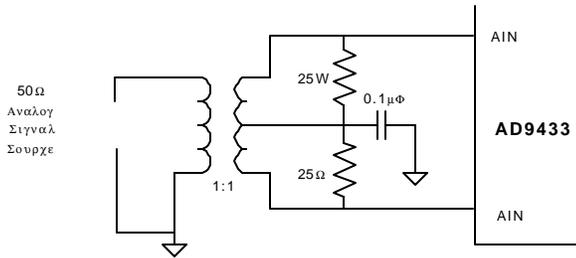


Figure TBD. Transformer-Coupled Analog Input Circuit

In the highest frequency applications, two transformers connected in series may be necessary to minimize even order harmonic distortion. The first transformer will isolate and convert the signal to a differential signal, but the grounded input on the primary side will degrade amplitude balance on the secondary winding. This imbalance is caused by capacitive coupling between the windings. Since one input to the first transformer is grounded, there is little or no capacitive coupling, resulting in an amplitude mismatch at the first transformers output. A second transformer will improve the amplitude balance, and thus improve the harmonic distortion. A wideband transformer, such as the ADT1-1WT from Mini Circuits, is recommended for these applications, as the bandwidth through the two transformers will be reduced by the  $\sqrt{2}$ .

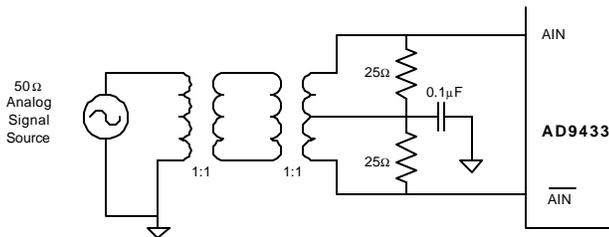


Figure TBD. Driving the Analog Input with 2 transformers for improved even order harmonics

Driving the ADC single-ended will degrade performance, particularly even order harmonics. For best dynamic performance, impedances at AIN and AIN should match. Special care was taken in the design of the analog input section of the AD9433 to prevent damage and corruption of data when the input is overdriven. When the nominal input range is set for 2.0V<sub>p-p</sub>, each analog input will be 1 V p-p when driven differentially. When set for 1.0V<sub>p-p</sub>, each analog input will be 0.5V<sub>p-p</sub> when driven differentially.

**SFDR Optimization**

The SFDR MODE pin enables (SFDR MODE=1) a proprietary circuit that may improve the spurious free dynamic range (SFDR) performance of the AD9433. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by non-linearities in the ADC transfer function.

Enabling this circuit will give the circuit a dynamic transfer function, meaning that the voltage threshold between two adjacent output codes may change from clock cycle to clock cycle. While improving spurious frequency content, this dynamic aspect of the

transfer function may be inappropriate for some time domain applications of the converter. Connecting the SFDR MODE pin to ground will disable this function. The typical performance curves section of the data sheet illustrates the improvement in the linearity of the converter and it's effect on spurious free dynamic range.

**Digital Outputs**

The digital outputs are 3V (2.7 V to 3.3 V) TTL/CMOS-compatible for lower power consumption. The output data format is selectable through the data format select (DFS) CMOS input. DFS=1 selects offset binary; DFS=0 selects two's complement coding.

**Table TBD. Offset Binary Output Coding (DFS=1, V<sub>REF</sub> = +2.5V)**

| Code | AIN-AIN (V)<br>Range=2Vp-p | AIN-AIN (V)<br>Range=1Vp-p | Digital Output |
|------|----------------------------|----------------------------|----------------|
| 4095 | 1.000                      | 0.500                      | 1111 1111 1111 |
| .    | .                          | .                          | .              |
| .    | .                          | .                          | .              |
| 2048 | 0                          | 0                          | 1000 0000 0000 |
| 2047 | -0.00049                   | -0.000245                  | 0111 1111 1111 |
| .    | .                          | .                          | .              |
| .    | .                          | .                          | .              |
| 0    | -1.000                     | -0.5000                    | 0000 0000 0000 |

**Table I. Two's Complement Output Coding (DFS=0, V<sub>REF</sub> = +2.5V)**

| Code  | AIN-AIN (V)<br>Range=2Vp-p | AIN-AIN (V)<br>Range=1Vp-p | Digital Output |
|-------|----------------------------|----------------------------|----------------|
| +2047 | 1.000                      | 0.500                      | 0111 1111 1111 |
| .     | .                          | .                          | .              |
| .     | .                          | .                          | .              |
| 0     | 0                          | 0                          | 0000 0000 0000 |
| -1    | -0.00049                   | -0.000245                  | 1111 1111 1111 |
| .     | .                          | .                          | .              |
| .     | .                          | .                          | .              |
| -2048 | -1.000                     | -0.5000                    | 1000 0000 0000 |

**Voltage Reference**

A stable and accurate 2.5 V voltage reference is built into the AD9433 (VREFOUT). In normal operation the internal reference is used by strapping Pin 45 to Pin 46 and placing a 0.1 μF decoupling capacitor at VREFIN. The input range can be adjusted by varying the reference voltage applied to the AD9433. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

**Timing**

The AD9433 provides latched data outputs, with 10 pipeline delays. Data outputs are available one propagation delay (t<sub>PD</sub>) after the rising edge of the encode command (see Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9433; these transients can detract from the converter's dynamic performance. The minimum guaranteed conversion rate of the AD9433 is 1 MSPS. At internal clock rates below 1 MSPS, dynamic performance may degrade.

### Replacing the AD9432 with the AD9433

The AD9433 is pin compatible with the AD9432, although there are 4 control pins on the AD9433 that are "do not connect (DNC), supply (V<sub>CC</sub>) or ground connections on the AD9432. They are summarized in the table below.

| Pin # | AD9432          | AD9433    |
|-------|-----------------|-----------|
| 39    | GND             | SELECT #1 |
| 40    | GND             | SELECT #2 |
| 41    | DNC             | DFS       |
| 42    | V <sub>CC</sub> | SFDR MODE |

Using the AD9433 in an AD9432 pin assignment will configure the AD9433 as follows:

- SELECT #1 and SELECT #2 will both be connected to ground, putting the device in IF Sampling I mode (2V

differential analog input range, performance optimized for 100-250MHz).

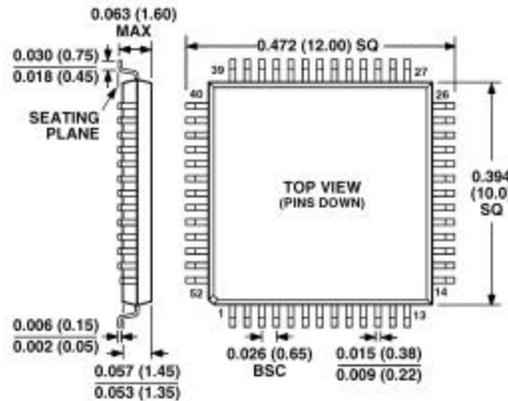
- The SFDR improvement circuit will be enabled.
- The DFS pin will float LOW, selecting Two's Complement coding for the digital outputs.

Other differences between the AD9432 and AD9433 are summarized as follows:

| Attribute                                | AD9432 | AD9433 |
|--|--------|--------|
| ENCODE / ENCODE V <sub>COMMON MODE</sub> | 1.6V   | 3.75V  |
| AIN / AIN V <sub>COMMON MODE</sub>       | 3.0V   | 4.0V   |

### AD9433BST OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



ST-52 Package