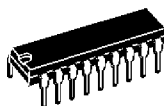


3.5A STEP DOWN SWITCHING REGULATOR

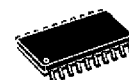
PRELIMINARY DATA

- UPTO3.5ASTEPPDOWNCONVERTER
- OPERATING INPUT VOLTAGE FROM 8V TO 55V
- 3.3V AND 5.1V (+/-2%) FIXED OUTPUT VOLTAGES
- OUTPUT VOLTAGE ADJUSTABLE FROM: 0V TO 50V (L4973V3)
5.1V TO 50V (L4973V5)
- FREQUENCY ADJUSTABLE UP TO 300KHz
- VOLTAGE FEED FORWARD
- ZERO LOAD CURRENT OPERATION (min 1mA)
- INTERNAL CURRENT LIMITING (PULSE BY PULSE AND HICCUP MODE)
- PRECISE 5.1V (1.5%) REFERENCE VOLTAGE EXTERNALLY AVAILABLE
- INPUT/OUTPUT SYNCHRONIZATION FUNCTION
- INHIBIT FOR ZERO CURRENT CONSUMPTION (100µA Typ. at V_{CC} = 24V)
- PROTECTION AGAINST FEEDBACK DISCONNECTION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (12+3+3)



SO20(12+4+4)

ORDERING NUMBERS:

L4973V3
L4973V5

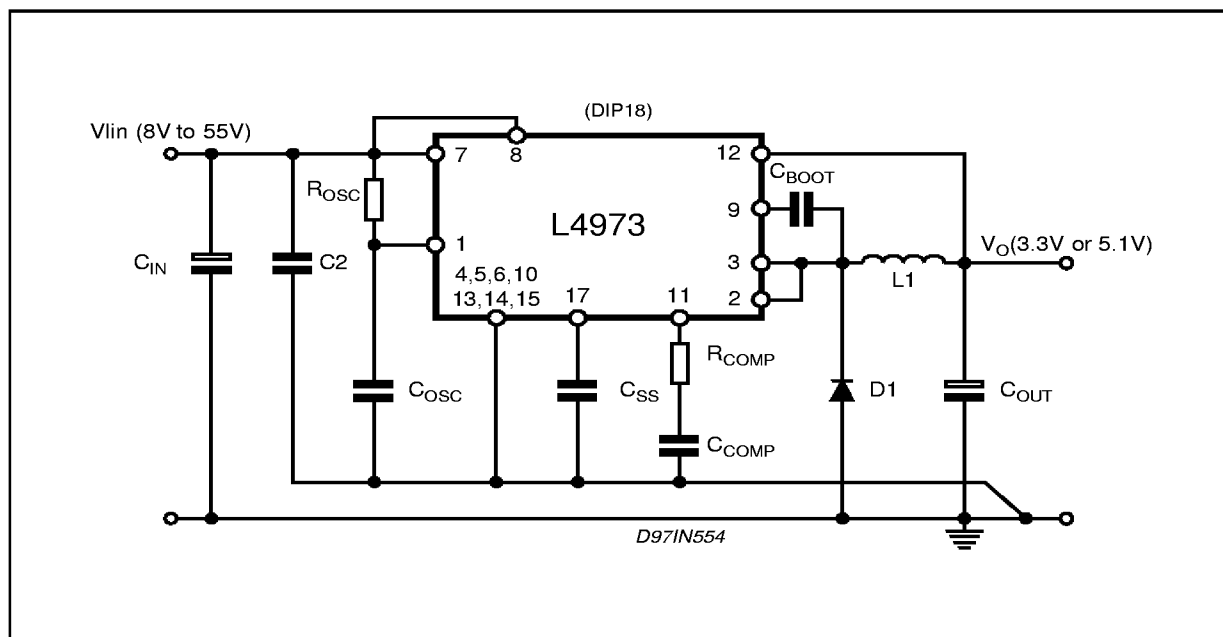
L4973D3
L4973D5

- THERMAL SHUTDOWN
- OUTPUT OVERVOLTAGE PROTECTION
- SOFT START FUNCTION

DESCRIPTION

The L4973 is a step down monolithic power switching regulator delivering 3.5A at fixed voltages of 3.3V or 5.1V and using a simple external divider output adjustable voltage up to 50V.

TYPICAL APPLICATION CIRCUIT



April 1997

1/8

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

L4973V3 - L4973V5 - L4973D3 - L4973D5

Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical $R_{ds(on)}$ of 0.15ohm) to obtain very high efficiency and very fast switching times.

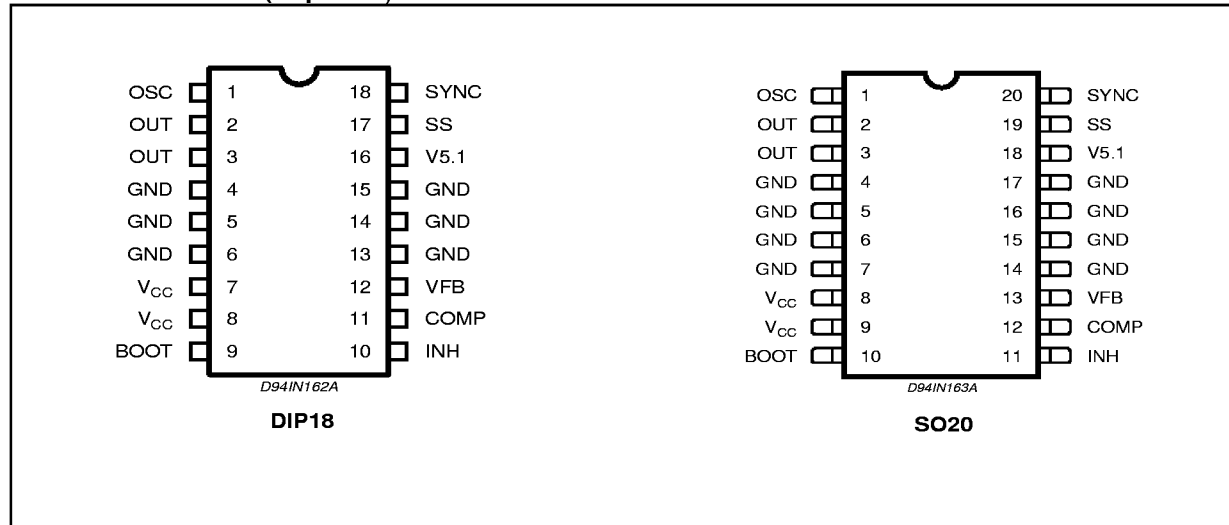
Switching frequency up to 300KHz are achievable (the maximum power dissipation of the packages must be observed).

A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 40V cover the majority of the today applications.

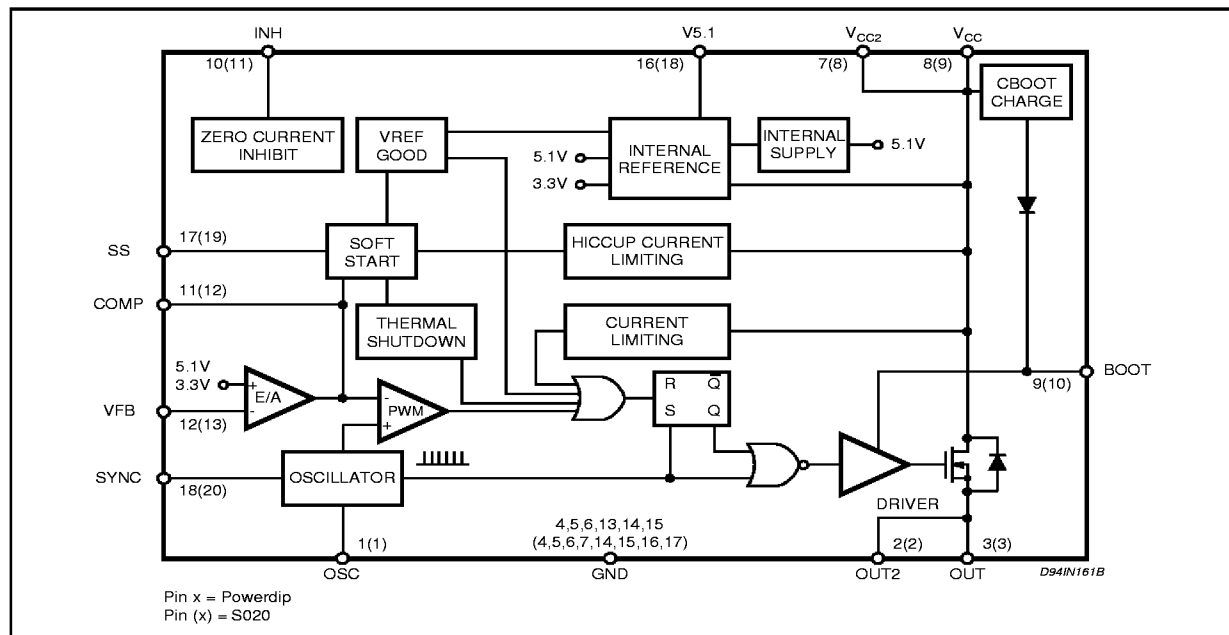
Features of this new generation of DC-DC converter includes pulse by pulse current limit, hiccup mode for output short circuit protection, voltage feed forward regulation, soft start, input/output synchronization, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown.

The proposed packages are in plastic dual in line, DIP-18 (12+3+3) for standard assembly, and SO20 (12+4+4) for SMD assembly.

PIN CONNECTIONS (Top view)



BLOCK DIAGRAM



THERMAL DATA

Symbol	Parameter		DIP18	SO20	Unit
$R_{th(j-pin)}$	Thermal Resistance Junction to pin	Max.	12	15	°C/W
$R_{th(j-amb)}$	Thermal Resistance to Ambient	Max.	60 (*)	80 (*)	°C/W

(*) Package mounted on board.

ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit	
DIP-18	SO-20				
V_7, V_8	V_9, V_8	Input voltage	58	V	
V_2, V_3	V_2, V_3	Output DC voltage Output peak voltage at $t = 0.1\mu s$ $f=200KHz$	-1 -5	V V	
I_2, I_3	I_2, I_3	Maximum output current	int. limit.		
V_9-V_8	$V_{10}-V_8$		14	V	
V_9	V_{10}	Bootstrap voltage	70	V	
V_{11}, V_{17}	V_{12}, V_{19}	Analogs input voltage ($V_{CC} = 24V$)	12	V	
V_{12}	V_{13}	($V_{CC} = 24V$)	6 -0.3	V V	
V_{18}	V_{20}	($V_{CC} = 24V$)	5.5 -0.3	V V	
V_{10}, V_1	V_{11}, V_1	Inhibit	V_{CC} -0.6	V V	
P_{tot}		Power dissipation a $T_{pins} \leq 90^\circ C$ ($T_{amb} = 70^\circ C$ no copper area) ($T_{amb} = 70^\circ C$ 4cm copper area on PCB)	DIP-18	5 1.3 2	W W W
		Power dissipation a $T_{pins} = 90^\circ C$	SO-20	4	W
		T_J, T_{STG}		Junction and storage temperature	-40 to 150

PIN FUNCTIONS

PIN DIP-18	PIN SO-20	NAME	DESCRIPTION
11	13	COMP	E/A output to be used for frequency compensation
10	11	INH	A logic signal (active high) disables the device (sleep mode operation). If not used it must be connected to GND; if floating the device is disabled.
9	10	BOOT	A capacitor connected between this pin and the output allows to drive the internal D-MOS.
18	20	SYNC	Input/Output synchronization.
7,8	8,9	Vcc	Not regulated DC input voltage
2,3	2,3	OUT	Stepdown regulator output.
12	12	VFB	Stepdown feedback input. Connecting directly this pin to the output 3.3V and 5.1V are obtained; a voltage divider is requested for higher output voltages. For voltage below 3.3V see note **
16	18	V5.1	Reference voltage externally available.
4,5,6 13,14,15	4,5,6,7 14,15,16,17	GND	Signal ground
1	1	OSC	An external resistor connected between the unregulated input voltage and Pin 1 and a capacitor connected from Pin 1 to ground fixes the switching frequency. (Line feed forward is automatically obtained)
17	19	SS	Soft start time constant. A capacitor connected between this terminal and ground determinates the soft start time.

L4973V3 - L4973V5 - L4973D3 - L4973D5

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25^\circ\text{C}$, $C_{\text{osc}} = 1.2\text{nF}$, $R_{\text{osc}} = 47\text{Kohm}$ $V_{\text{cc}} = 24\text{V}$ unless otherwise specified) • = specifications referred to T_j from 0 to 125°C .

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
	Input Voltage range (*)	$V_o = V_{\text{REF}}$ to 40V $I_o = 3.5\text{A}$	•	8		55	V
	Output Voltage L4973V5.1	$I_o = 1\text{A}$		5.05	5.1	5.15	V
		$I_o = 0.5\text{A}$ to 3.5A $V_{\text{CC}} = 8\text{V}$ to 55V		5.00	5.1	5.20	V
			•	4.95	5.1	5.25	V
	Output Voltage L4973V3.3	$I_o = 1\text{A}$		3.327	3.36	3.346	V
		$I_o = 0.5\text{A}$ to 3.5A $V_{\text{CC}} = 8\text{V}$ to 40V		3.292	3.36	3.427	V
			•	3.26	3.36	3.46	V
	$R_{\text{DS(on)}}$	$V_{\text{CC}} = 10.5\text{V}$, $I_o = 3.5\text{A}$			0.15	0.22	Ω
			•			0.35	Ω
	Maximum limiting current	$V_{\text{CC}} = 8\text{V}$ to 55V	•	4	4.5	5.5	A
η	efficiency	$V_o = 5.1\text{V}$ $I_o = 3.5\text{A}$			90		%
		$V_o = 3.3\text{V}$ $I_o = 3.5\text{A}$				85	
	Switching frequency		•	90	100	110	KHz
	Supply Voltage Ripple Rejection	$V_i = V_{\text{CC}} + 2\text{VRMS}$ $V_o = V_{\text{ref}}$, $I_o = 1\text{A}$, $f_{\text{ripple}} = 100\text{Hz}$		60			dB
Δf_{sw}	Switching frequency stability vs. supply voltage	$V_{\text{CC}} = 8\text{V}$ to 55V			2	5	%
REFERENCE SECTION							
	Reference voltage			5.025	5.1	5.175	V
		$I_{\text{ref}} = 0$ to 20mA $V_{\text{CC}} = 8\text{V}$ to 55V	•	4.950	5.1	5.250	V
	Line regulation	$V_{\text{CC}} = 8\text{V}$ to 55V $I_{\text{ref}} = 0\text{mA}$			5	10	mV
	Load regulation	$I_{\text{ref}} = 0$ to 5mA			2	10	mV
		$I_{\text{ref}} = 0$ to 20mA				6	25
	Short circuit current			30	65	100	mA
SOFT START							
	Soft start charge current			30	45	60	μA
	Soft start discharge current			15	22	30	μA
INHIBIT (not compatible with the 3.3V)							
	High level voltage		•	3.0			V
	Low level voltage		•			0.8	V
	I_{source} High level	$V_{\text{INH}} = 3\text{V}$	•	10	20	50	μA
	I_{source} Low level	$V_{\text{INH}} = 0.8\text{V}$	•	10	20	50	μA
DC CHARACTERISTICS							
	Total operating quiescent current	duty cycle = 50%			4	8	mA
	Quiescent current	duty cycle = 0			2.5	4.5	mA
	Total stand by quiescent current	Inhibit floating or $V_{\text{INH}} = 5\text{V}$ $V_{\text{CC}} = 24\text{V}$ $V_{\text{CC}} = 55\text{V}$			100	200	μA
						150	300
ERROR AMPLIFIER							
	High level output voltage			11.0			V
	Low level output Voltage					0.65	V
	Source Bias Current			1	2	3	μA

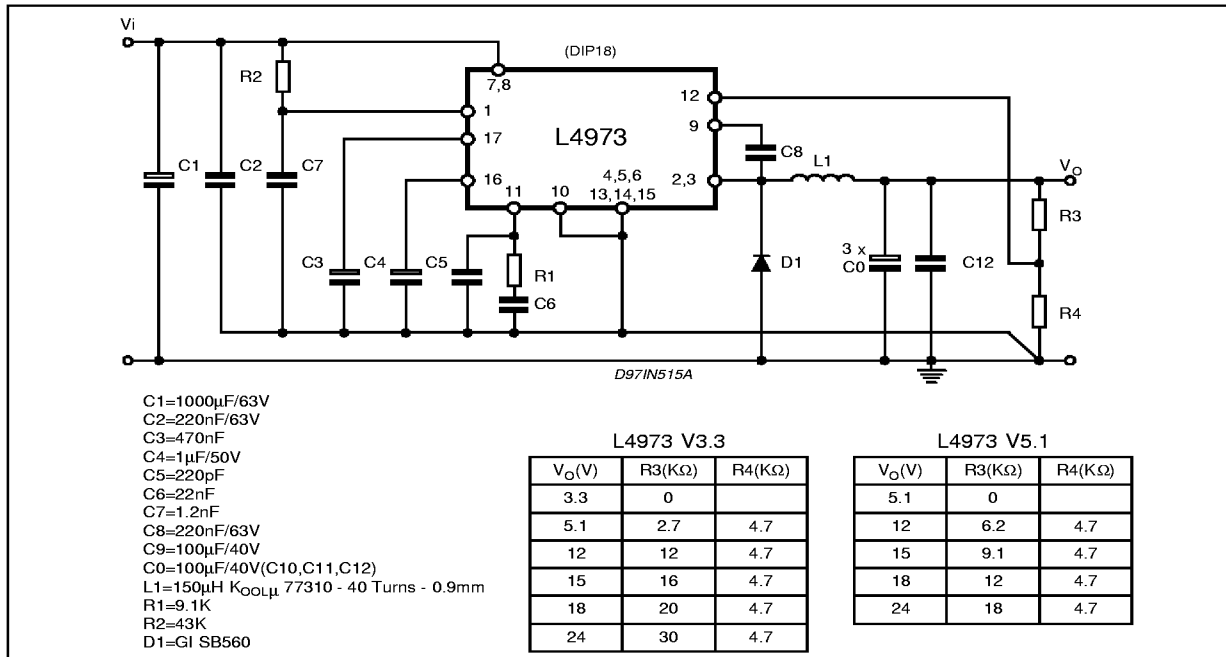
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Source output current		200	300	600	μA
	Sink output current		200	300		μA
	Supply voltage ripple rejection	V _{COMP} = VFB V _{CC} = 8V to 55V	60	80		dB
	DC open loop gain	R _L = ∞	50	60		dB
	Transconductance	I _{comp} = -0.1mA to 0.1mA; V _{comp} = 6V		2.5		mS
OSCILLATOR SECTION						
	Ramp valley		0.78	0.85	0.92	V
	Ramp peak	V _{CC} = 8V	1.9	2.1	2.3	V
		V _{CC} = 55V	9	9.6	10.2	V
	Maximum duty cycle		95	97		%
	Maximum Frequency	Duty cycle = 0% R _{osc} = 20kΩ C _{osc} = 680pF			500	kHz
SYNC FUNCTION						
	High input voltage	V _{CC} = 8V to 55V	3.5			V
	Low input voltage	V _{CC} = 8V to 55V			0.9	V
	Slave sink current		0.15	0.25	0.45	mA
	Master output amplitude	I _{source} = 3mA	4	4.5		V
	Output pulse width	no load, V _{sync} = 4.5V	0.20	0.35		μs

(*) Pulse testing with a low duty cycle.

(**) The maximum power dissipation of the packages must be observed.

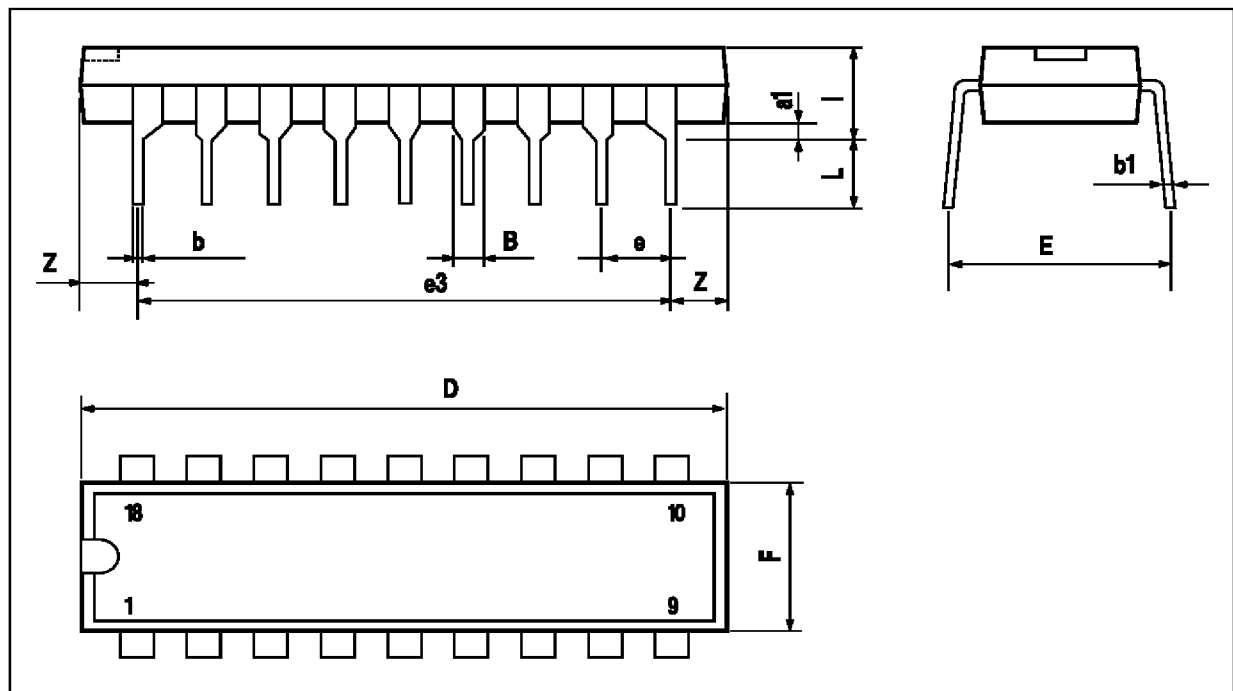
APPLICATION CIRCUIT



L4973V3 - L4973V5 - L4973D3 - L4973D5

POWERDIP 18 PACKAGE MECHANICAL DATA

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
l			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					

