MN35503

D/A Converter for Digital Audio Equipment

■ Overview

The MN35503 is a CMOS digital-to-analog converter designed especially for PCM digital audio equipment. It features a built-in digital filter with 16/20-bit input.

It uses pulse edge modulation (PEM) and JVC advanced noise shaping (VANS) to yield the high resolution and low distortion ratio equivalent to those of 20-bit systems covering the range between 0 and 20 kHz.

The chip incorporating an 8-fold oversampling digital filter that eliminates a low-pass filter after the D/A converter and greatly reduces the power consumption of the overall D/A conversion system.

The chip makes a major contribution to reducing the cost and size of CD players and other digital audio equipment.

■ Features

- Built-in 8-fold oversampling digital filter using I^2S bus
  - Bandwidth ripple: within ±0.05 dB for 0 to 0.454 f_s
  - Cutoff band attenuation (0.546 to 7.454) f_s : 37dB

    (n–0.03125) f_s to (n+0.03125) f_s : min. 60dB

    n=1 to 7 (integer)

    (The above characteristics include those for an external primary low-pass filter with f_s=1.95 f_s.)
- Built-in digital de-emphasis

  f_s=32.0 kHz 0 to14.5 kHz max. deviation +0.072dB/ – 0.047 dB

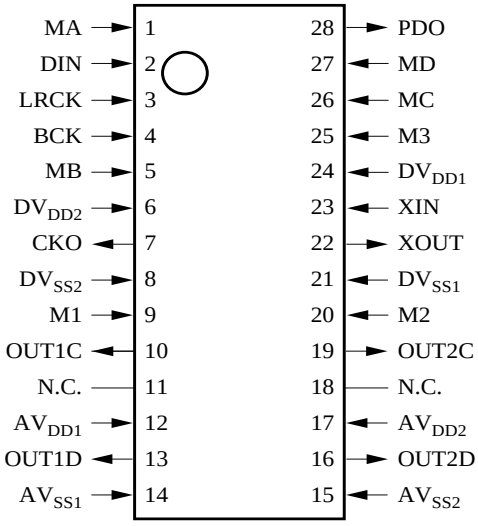
  f_s=44.1 kHz 0 to 20 kHz max. deviation +0.077dB/ – 0.028 dB

  f_s=48.0 kHz 0 to 21.8 kHz max. deviation +0.052dB/ – 0.053 dB

  (The above characteristics include those for an external primary low-pass filter with f_c=1.95 f_s.)
- The digital filter is designed to deliver the above bandwidth characteristics when used with an external primary low-pass filter with f_c=1.95 f_s.
- Built-in digital attenuation

  Up/down over 32 steps
- Support for double-speed operation (192 f_s clock)
- 4PEM output configuration (2PEM output per channel)
- Support for low-voltage (3.0 volt) operation

■ Pin Assignment



(TOP VIEW)

SOP028-P-0375

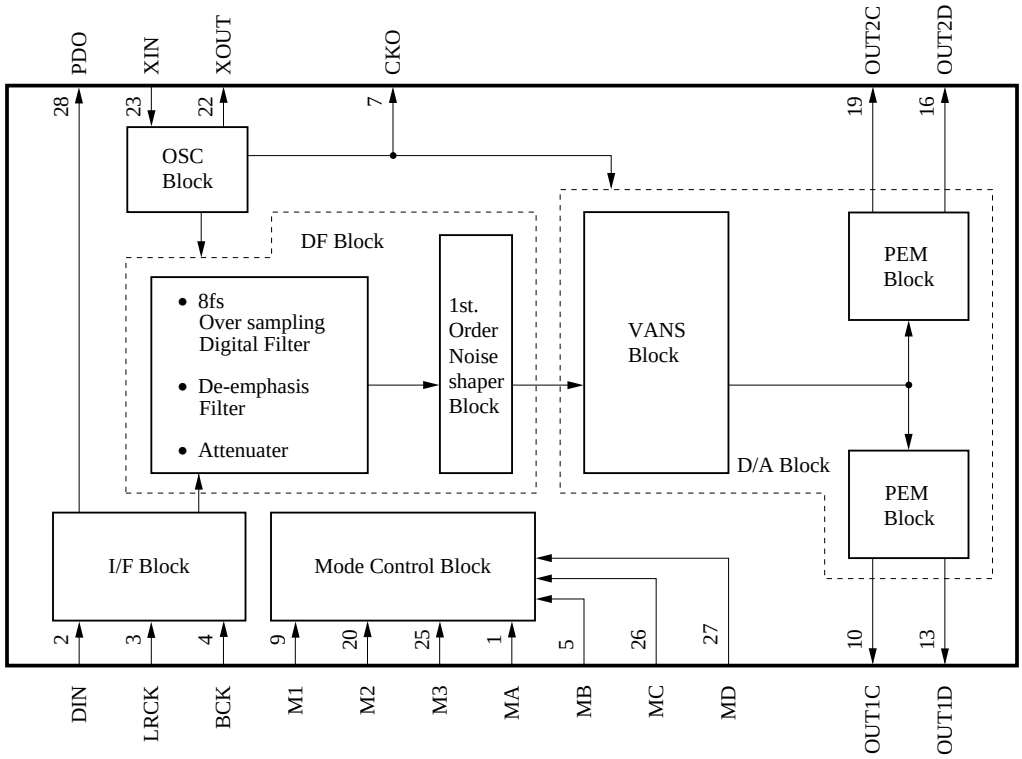
- Choice of system clocks:

  192f_s , 256f_s, 384f_s , 512f_s , 576f_s
- Choice of input data formats: right-packed or I^2S bus (16 or 20 bits, alternating channel input, MSB first)
- Built-in phase comparator

■ Applications

- CD players and other digital audio equipment

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	MA	Operating mode selection pin 4 (See Table 1.)
2	DIN	Serial data input pin (MSB first)
3	LRCK	LR synchronization signal input pin (f_s rate)
4	BCK	Data shift bit clock input pin
5	MB	Operating mode selection pin 5 (See Table 1.)
6	DV_{DD2}	Power supply pin 2 for digital circuits
7	CKO	Clock output pin
8	DV_{SS2}	Ground pin 2 for digital circuits
9	M1	Operating mode selection pin 1, with pull-up resistor (See Table 1.)
10	OUT1C	PEM output pin 1C (Left channel with reversed phase)
11	N.C.	No connection (Leave this pin open.)
12	AV_{DD1}	Power supply pin 1 for analog circuits
13	OUT1D	PEM output pin 1D (Left channel with reversed phase)
14	AV_{SS1}	Ground pin 1 for analog circuits
15	AV_{SS2}	Ground pin 2 for analog circuits
16	OUT2D	PEM output pin 2D (Right channel with reversed phase)
17	AV_{DD2}	Power supply pin 2 for analog circuits
18	N.C.	No connection (Leave this pin open.)
19	OUT2C	PEM output pin 2C (Right channel with reversed phase)
20	M2	Operating mode selection pin 2, with pull-up resistor (See Table 1.)
21	DV_{SS1}	Ground pin 1 for digital circuits (Ground for oscillator circuit)
22	XOUT	Crystal oscillator pin
23	XIN	Crystal oscillator pin (external clock input pin) (Built-in feedback resistor)
24	DV_{DD1}	Power supply pin 1 for digital circuits (for oscillation circuit)
25	M3	Operating mode selection pin 3 (See Table 1.)
26	MC	Reset pin/digital attenuation control pin (See Table 1.)
27	MD	Reset pin/digital attenuation control pin (See Table 1.)
28	PDO	Phase comparator output pin (tristate output)*1

Note*1: This pin provides tristate output indicating the result of comparing the phases of the internal f_s-rate-signal and the LRCK input signal. It is at "H" level when the LRCK signal leads and is at "L" level when the signal lags. At all other times, it is in the high-impedance state.

■ Operating Mode Descriptions

Table 1-1. MN35503 Operating Modes

Mode Selection Pins	Pin States and Operating Modes															
M1 Includes pull-up resistor	L															
M2 Includes pull-up resistor	L								H							
M3	L				H				L				H			
MA	L		H		L		H		MDAT				L		H	
MB	L	H	L	H	L	H	L	H	MCLK				L	H	L	H
MC	RSBUP								MLAT				RSBUP			
MD	RSBDN								L		H		RSBDN			
MODE	0_0	0_1	0_2	0_3	1_0	1_1	1_2	1_3	2_0		2_1		3_0	3_1	3_2	3_3
									Serial mode							

Input data form	Right-packed															
Input word length (bits)	16															
LRCK level for left channel data	H															
XIN clock frequency (f_s)	384				*1 192		*2 576		*2 384/576 See Table 3.		*2 256/384 See Table 3.		256			
CKO output frequency (f_s)	384				192		576		384/576 See Table 3.		256/384 See Table 3.		STOP			
DE-EMP. (f_s=[kHz])	–	44.1	32	48	–	44.1	–	32	See Table 3				–	44.1	32	48
Output level	$0.598 \times AV_{DD}$										$0.448 \times AV_{DD}$					
VANS oversampling (f_s)	64				32		96		64/96		64/96		64			
Theoretical signal-to-noise ratio (dB)	122				95		138		122/138		116/132		116			

Notes

*1: During 192 f_s operation, the chip supports fs clock speeds up to 88.2 kHz.

*2: During 576 f_s operation and 384 f_s operation in modes 2_1 or 6_1, the chip supports f_s clock speeds up to 32 kHz; for other modes, it supports up to 48 kHz.

Table 1-2. MN35503 Operating Modes

Mode Selection Pins	Pin States and Operating Modes															
M1 Includes pull-up resistor	H															
M2 Includes pull-up resistor	L								H							
M3	L				H				L				H			
MA	L		H		L		H		MDAT				L		H	
MB	L	H	L	H	L	H	L	H	MCLK				L	H	L	H
MC	RSBUP								MLAT				RSBUP			
MD	RSBDN								L		H		RSBDN			
MODE	4_0	4_1	4_2	4_3	5_0	5_1	5_2	5_3	6_0		6_1		7_0	7_1	7_2	7_3
									Serial mode							
Input data form	Right-packed						I²S						Right-packed			
Input word length (bits)	16				20		to 20						16		20	
LRCK level for left channel data	L				H		L						H			
XIN clock frequency (f_s)	384			*1 576	384			*1 576	*1 384/576 See Table 3.		*1 256/384 See Table 3.		512			
CKO output frequency (f_s)	384	STOP	384	STOP	384			576	384/576 See Table 3.		256/384 See Table 3.		512			
DE-EMP.(f_s=[kHz])	–	48	44.1	32	–	44.1	–		See Table 3.				–	44.1	–	
Output level					$0.598 \times AV_{DD}$						$0.448 \times AV_{DD}$					
VANS oversampling (f_s)	64			94	64		96		64/96		64/96		64			
Theoretical signal-to-noise ratio (dB)	122			138	122		138		122/138		116/132		122			

Test Mode

Note*1: During 576 f_s operation and 384 f_s operation in modes 2_1 or 6_1, the chip supports f_s clock speeds up to 32 kHz; for other modes, it supports up to 48 kHz.

- Serial Mode (MODE=2_0, 2_1, 6_0, 6_1)

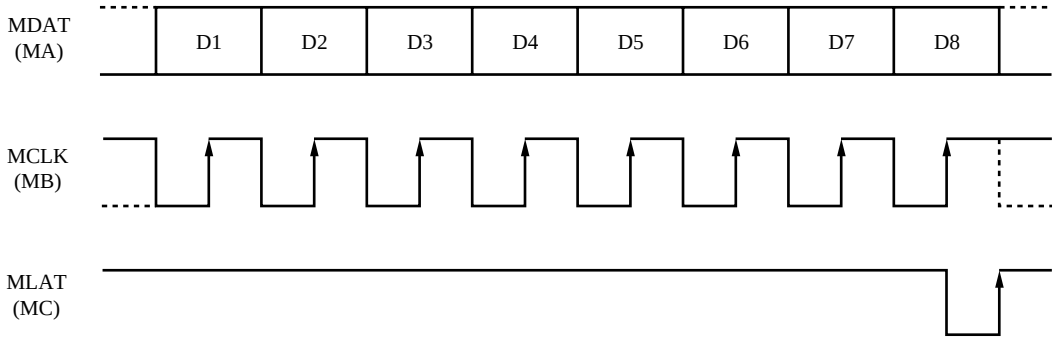


Figure 1. Serial Mode Input Signal Timing

Table 2. Attenuation Control

The 5-bit from D1 (MSB) to D5 (LSB) specifies a code of the 32 available attenuation step. (See Table 2.)

D1	D2	D3	D4	D5	Code	Output Level (dB)
0	0	0	0	0	00H	0.0
0	0	0	0	1	01H	–1.0
0	0	0	1	0	02H	–2.0
		⋮			⋮	⋮
1	1	1	1	0	1EH	– 48.1
1	1	1	1	1	1FH	−∞ (mute)

0=L, 1=H

Table 3. Mode Control

The combination of 3-bit from pins D6 to D8 controls XIN clock frequency, de-emphasis, and reset operation.

D6	D7	D8	XIN Clock Frequency [f_S] at MD=L	XIN Clock Frequency [f_S] at MD=H	DE-EMP. f_S=[kHz]	Reset ●: Reset —: Normal
0	0	0	384	256	OFF	—
0	0	1	384	256	32	—
0	1	0	384	256	OFF	●
0	1	1	576	384	32	—
1	0	0	384	256	44.1	—
1	0	1	384	256	48	—
1	1	0	576	384	OFF	●
1	1	1	576	384	OFF	—

0=L, 1=H MD=L: MODE=2_0, 6_0
MD=H: MODE=2_1, 6_1

- Digital attenuation and reset (Parallel mode)

Table 4 shows how the inputs from the two pins MC (RSBUP) and MD (RSBDN) control digital attenuation except the serial modes.

Table 4. Attenuation Modes

Pin Name	Pin States and Operating Modes				
MC (RSBUP)	L	↑↓	L	↑	H
MD (RSBDN)	L	L	↑	H	↑
Mode	Reset	Mute	Normal	Attenuation control	
Volume	Mute (–∞)		0dB	UP	DOWN

Note: The upward arrow indicates the rising edge change of the input signal; the paired arrows, the rising and falling edge changes.

There are a total of 32 attenuation levels.

According to the attenuation control shown in Table-4, volume goes up or down in one step every input-signal rising-edge. Still, in the 0 dB state, up-pulse does not change the volume. Similary, in the muting state (–∞), down-pulse does not change the volume.

The change of the input signals is detected by inner clock of 16 f_s period, so always use a frequency of 8 f_s or less for changes in the RSBUP and RSBDN signals. Note, however, that changes in attenuation level require a period corresponding to 2 f_s to complete.

Do not simultaneously change the RSBUP and RSBDN signals unless setting up for a reset.

■ Conversion Characteristics

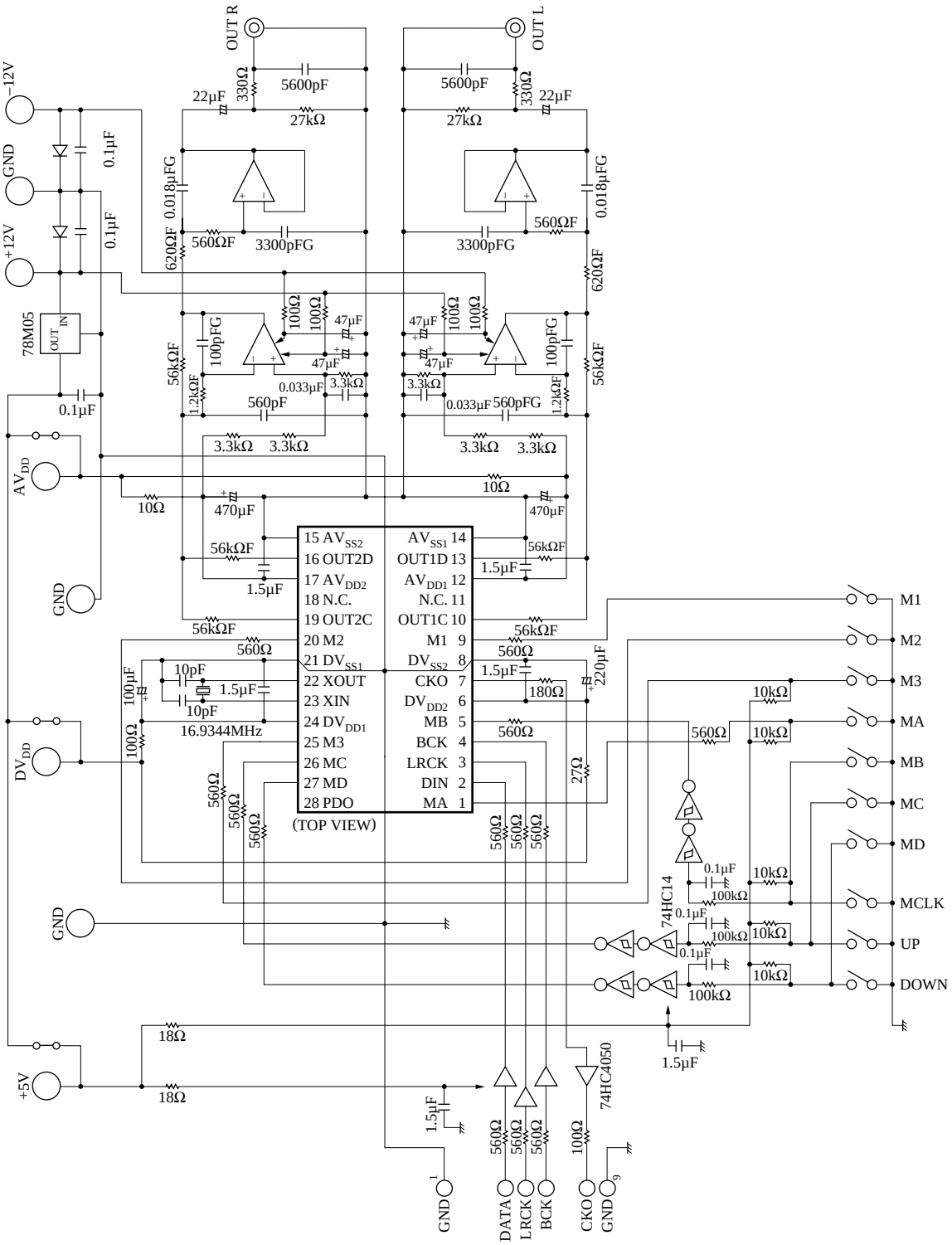
DV_{DD}=5.0V, DV_{SS}=0V, AV_{DD}=5.0V, AVss=0V, f=16.9344MHz, Ta=25˚C

Analog Characteristics for 20-bit, 1 f_s input

Parameter	Symbol	Test Condition	min	typ	max	Unit
Signal-to-noise ratio		EIAJ (1kHz)		108		dB
Dynamic range	D.R.	EIAJ (1kHz)		107		dB
Total harmonic distortion	THD+N	EIAJ (1kHz)		0.0008	0.0015	%
Output level		1 kHz full scale		2.0		V_{rms}

The above analog characteristics are based on measurements with the sample application circuit using mode 5_0.

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

SOP028-P-0375