

MOS FIELD EFFECT TRANSISTOR
2SK2512

**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The 2SK2512 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 15 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 23 \text{ A}$)
 $R_{DS(on)2} = 23 \text{ m}\Omega$ ($V_{GS} = 4 \text{ V}$, $I_D = 23 \text{ A}$)
- Low C_{iss} $C_{iss} = 2 \text{ 100 pF TYP.}$
- Built-in G-S Protection Diode

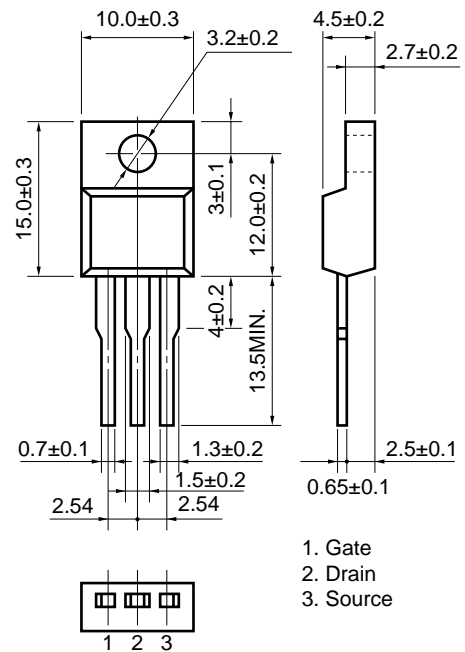
ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{bSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 45	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 180	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

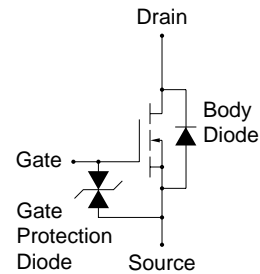
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**PACKAGE DIMENSIONS
(in millimeter)**



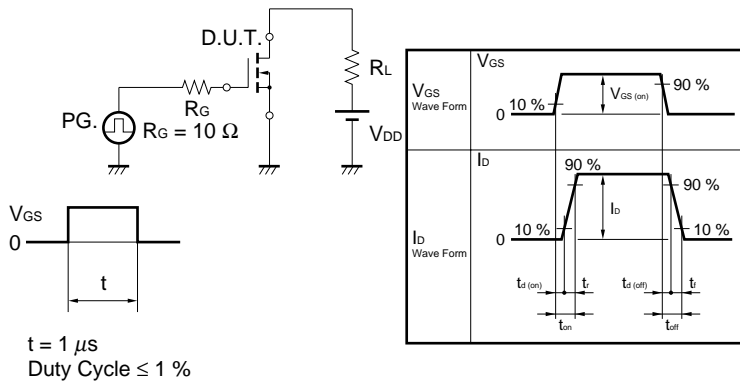
MP-45F (ISOLATED TO-220)



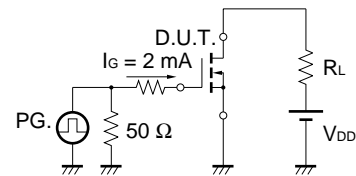
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R _{DS (on)1}		11	15	mΩ	V _{GS} = 10 V, I _D = 23 A
Drain to Source On-Resistance	R _{DS (on)2}		16	23	mΩ	V _{GS} = 4 V, I _D = 23 A
Gate to Source Cutoff Voltage	V _{GS (off)}	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	15	20		S	V _{DS} = 10 V, I _D = 23 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 100		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		1 100		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		500		pF	f = 1 MHz
Turn-On Delay Time	t _{d (on)}		45		ns	I _D = 23 A
Rise Time	t _r		380		ns	V _{GS (on)} = 10 V
Turn-Off Delay Time	t _{d (off)}		320		ns	V _{DD} = 30 V
Fall Time	t _f		320		ns	R _G = 10 Ω
Total Gate Charge	Q _G		101		nC	I _D = 45 A
Gate to Source Charge	Q _{GS}		7		nC	V _{DD} = 48 V
Gate to Drain Charge	Q _{GD}		40		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F (S-D)}		1.0		V	I _F = 45 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		100		ns	I _F = 45 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		180		nC	di/dt = 100 A/μs

Test Circuit 1 Switching Time

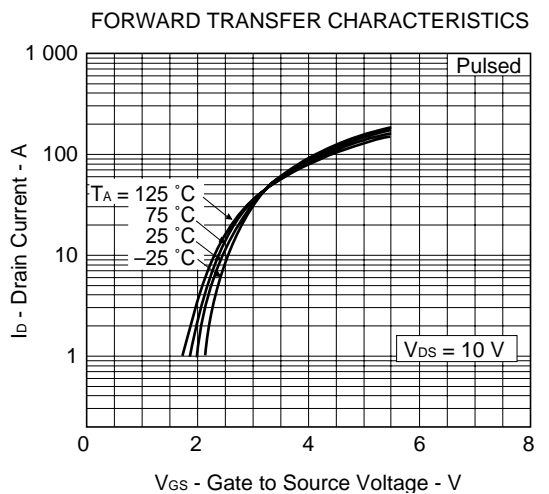
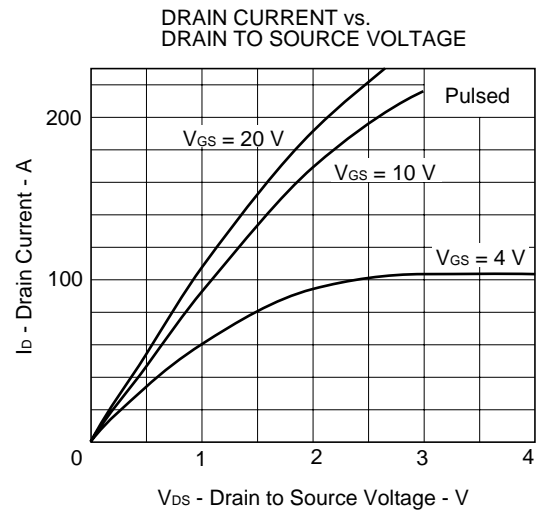
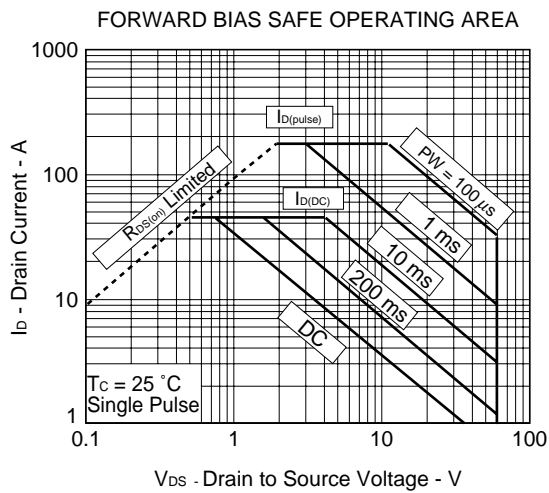
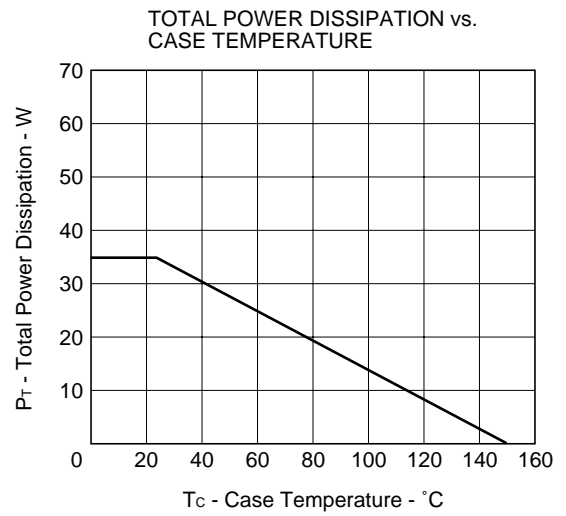
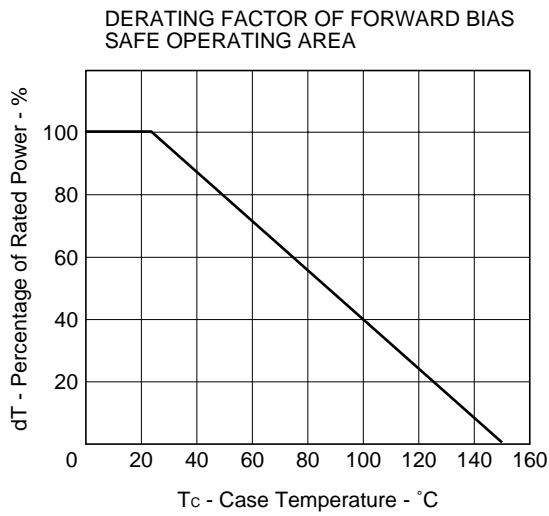


Test Circuit 2 Gate Charge

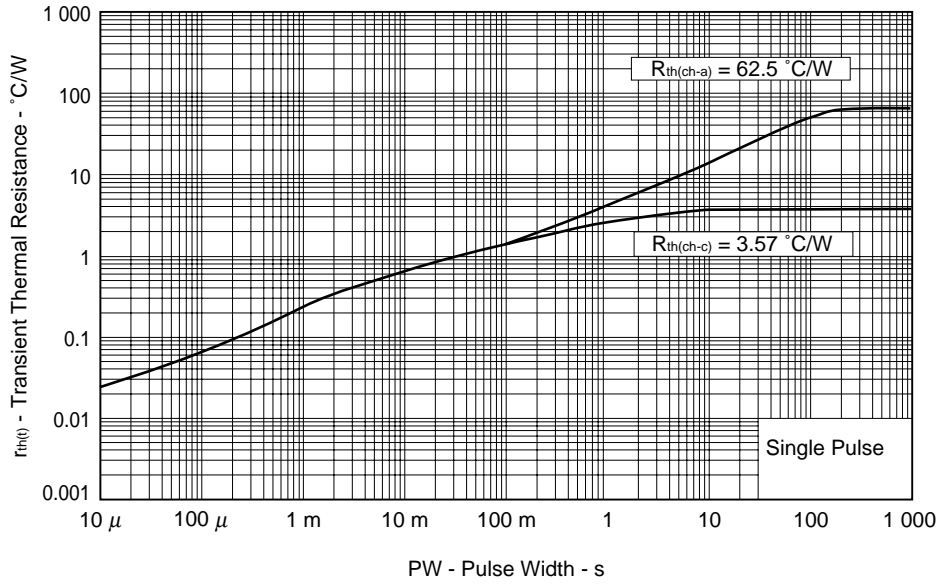


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

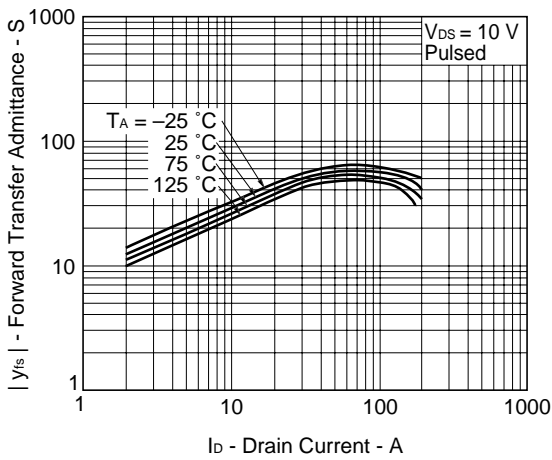
TYPICAL CHARACTERISTICS (T_A = 25 °C)



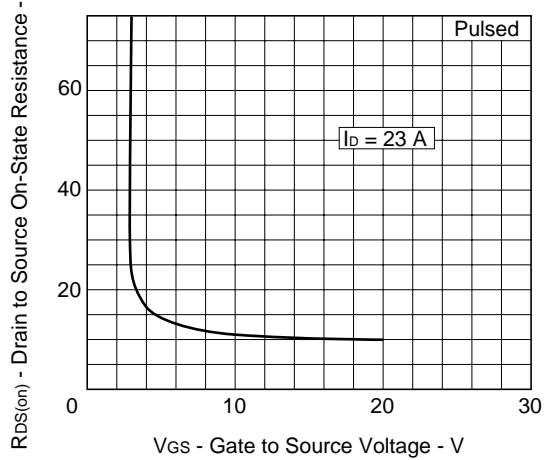
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



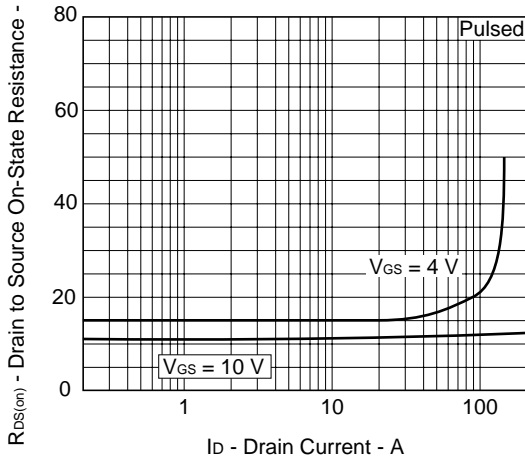
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



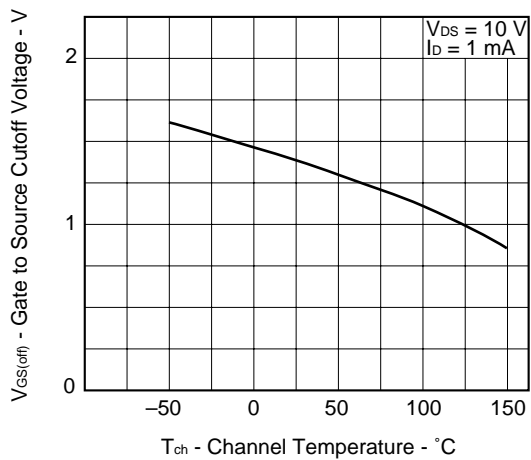
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

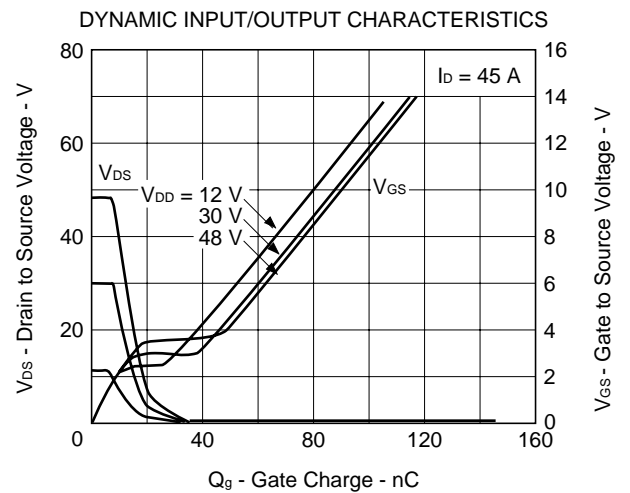
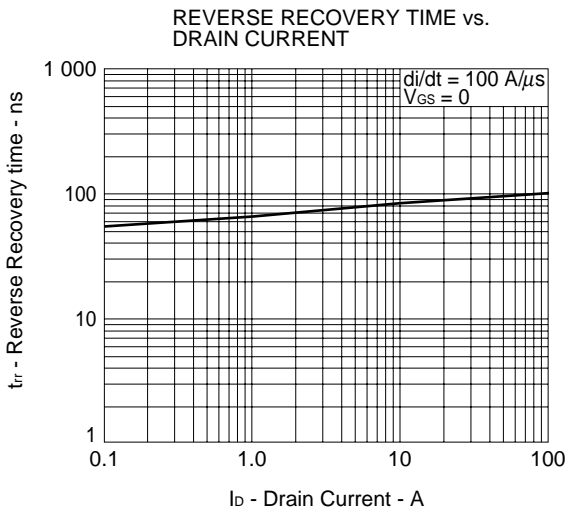
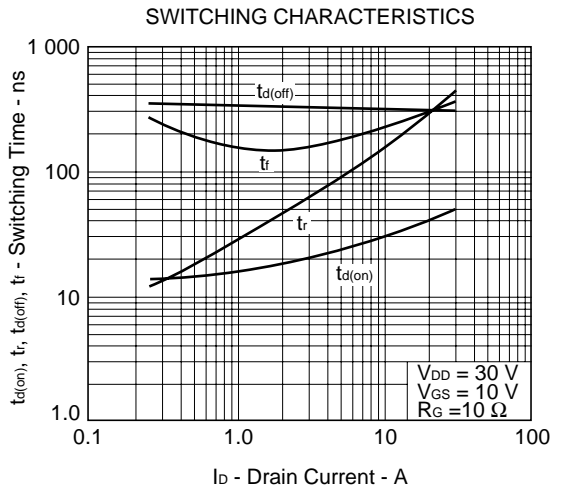
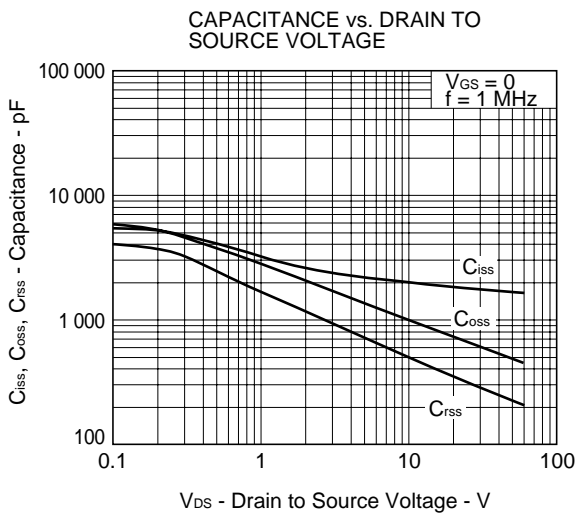
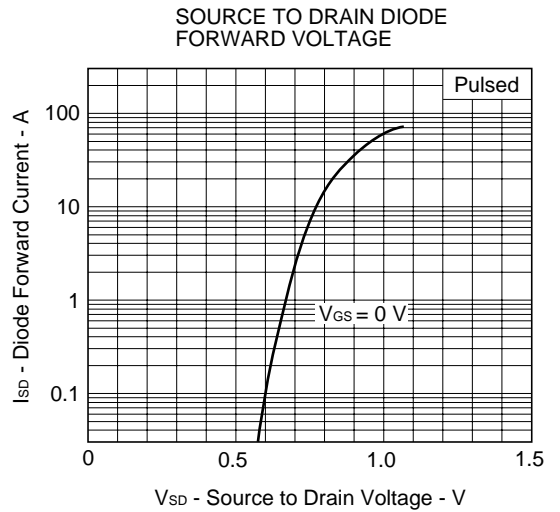
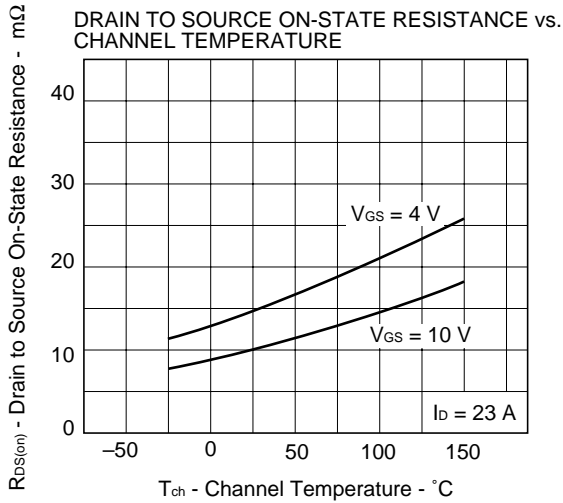


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.