



Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

General Description

The MAX9181 is an LVPECL-to-LVDS level translator that accepts a single LVPECL input and translates it to a single LVDS output. It is ideal for interfacing between LVPECL and LVDS interfaces in systems that require minimum jitter, noise, power, and space.

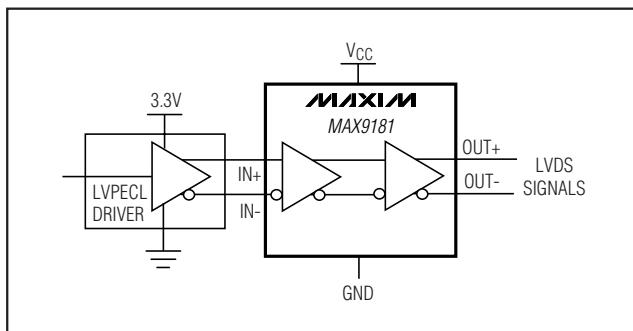
Ultra-low, 23psp-p added deterministic jitter and 0.6psRMS added random jitter ensure reliable communication in high-speed links that are highly sensitive to timing errors, especially those incorporating clock-and-data recovery, PLLs, serializers, or deserializers. The MAX9181's switching performance guarantees a 400Mbps data rate, but minimizes radiated noise by guaranteeing 0.5ns minimum output transition time.

The MAX9181 operates from a single 3.3V supply and consumes only 10mA supply current over a -40°C to +85°C temperature range. It is available in a tiny 6-pin SC70 package (half the size of a SOT23). Refer to the MAX9180 data sheet for a low-jitter, low-noise LVDS repeater in an SC70 package.

Applications

Digital Cross-Connects
Add/Drop Muxes
Network Switches/Routers
Cellular Phone Base Stations
DSLAMs
Multidrop Buses

Typical Operating Circuit



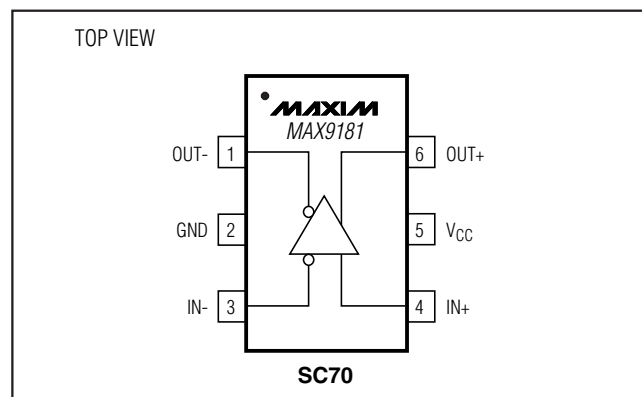
Features

- ◆ Tiny SC70 Package
- ◆ Ultra-Low Jitter
 - 23psp-p Added Deterministic Jitter (2^{23} - 1 PRBS)
 - 0.6psRMS Added Random Jitter
- ◆ 0.5ns (min) Transition Time Minimizes Radiated Noise
- ◆ 400Mbps Guaranteed Data Rate
- ◆ Low 10mA Supply Current
- ◆ Conforms to ANSI/EIA/TIA-644 LVDS Standard
- ◆ High-Impedance Inputs and Outputs in Power-Down Mode

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9181EXT-T	-40°C to +85°C	6 SC70-6	ABD

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{CC} to GND	-0.3V to +4.0V	Operating Temperature Range	-40°C to +85°C
IN+, IN- to GND	-0.3V to +4.0V	Storage Temperature Range	-65°C to +150°C
OUT+, OUT- to GND	-0.3V to +4.0V	Junction Temperature	+150°C
Short-Circuit Duration (OUT+, OUT-)	Continuous	ESD Protection	
Continuous Power Dissipation (T _A = +70°C)		Human Body Model, IN+, IN-, OUT+, OUT-	±8kV
6-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW	Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω ±1%, |V_{ID}| = 0.05V to V_{CC}, V_{CM} = |V_{ID} / 2| to V_{CC} - |V_{ID} / 2|, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
LVPECL INPUT							
Differential Input High Threshold	V _{TH}			7	50	mV	
Differential Input Low Threshold	V _{TL}		-50	-7		mV	
Input Resistor	R _{IN}	Figure 1	360	1328		kΩ	
Input Current	I _{IN+} , I _{IN-}	IN+ = 3.6V, IN- = 0V	-10	+2.7	+10	μA	
		IN+ = 0V, IN- = 3.6V	-10	+2.7	+10		
Power-Off Input Current	I _{IN+} , I _{IN-}	V _{CC} = 0V, Figure 1	IN+ = 3.6V, IN- = 0V	-10	+2.7	+10	μA
			IN+ = 0V, IN- = 3.6V	-10	+2.7	+10	
LVDS OUTPUT							
Differential Output Voltage	V _{OD}	Figure 2	250	360	450	mV	
Differential Output Voltage	ΔV _{OD}	Figure 2		0.008	25	mV	
Offset (Common-Mode) Voltage	V _{OS}	Figure 2	1.125	1.25	1.375	V	
Change in V _{OS} for Complementary Output States	ΔV _{OS}	Figure 2		0.005	25	mV	
Output High Voltage	V _{OH}			1.44	1.6	V	
Output Low Voltage	V _{OL}		0.9	1.08		V	
Differential Output Voltage	V _{OD+}	IN+, IN- open	+250	+360	+450	mV	
Power-Off Output Leakage Current	I _O OFF	V _{CC} = 0V	OUT+ = 3.6V, other output open	-10	+0.02	+10	μA
			OUT- = 3.6V, other output open	-10	+0.02	+10	
Differential Output Resistance	R _{ODIFF}	V _{CC} = 3.6V or 0V	100	260	400	Ω	
Output Short Current	I _{SC}	V _{ID} = 50mV, OUT+ = GND		-5	-15	mA	
		V _{ID} = -50mV, OUT- = GND		-5	-15		
POWER SUPPLY							
Supply Current	I _{CC}			10	15	mA	

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$, $C_L = 10pF$, $|V_{ID}| = 0.15V$ to V_{CC} , $V_{CM} = |V_{ID}| / 2$ to $V_{CC} - |V_{ID}| / 2$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^\circ C$.) (Notes 3, 4, 5) (Figures 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}		1.3	2.0	2.8	ns
Differential Propagation Delay Low to High	t_{PLHD}		1.3	2.0	2.8	ns
Added Deterministic Jitter	t_{DJ}	400Mbps 2^{23} - 1 PRBS data pattern (Notes 6, 11)		23	100	psp-p
Added Random Jitter	t_{RJ}	$f_{IN} = 200MHz$ (Notes 7, 11)		0.6	2.9	psRMS
Differential Part-to-Part Skew	t_{SKPP1}	(Note 8)		0.16	0.6	ns
Differential Part-to-Part Skew	t_{SKPP2}	(Note 9)			1.5	ns
Switching Supply Current	I_{CCSW}			12.2	18	mA
Rise Time	t_{TLH}		0.5	0.67	1.0	ns
Fall Time	t_{THL}		0.5	0.66	1.0	ns
Input Frequency	f_{MAX}	(Note 10)	200			MHz

Note 1: All devices are 100% tested at $T_A = +25^\circ C$. Limits over temperature are guaranteed by design and characterization.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} , V_{TL} , V_{OD} , and ΔV_{OD} .

Note 3: Guaranteed by design and characterization.

Note 4: Signal generator output (unless otherwise noted): frequency = 200MHz, 50% duty cycle, $R_O = 50\Omega$, $t_R = 1.5ns$, and $t_F = 1.5ns$ (0% to 100%).

Note 5: C_L includes scope probe and test jig capacitance.

Note 6: Signal generator output for t_{DJ} : $V_{OD} = 150mV$, $V_{OS} = 1.2V$, t_{DJ} includes pulse (duty cycle) skew.

Note 7: Signal generator output for t_{RJ} : $V_{OD} = 150mV$, $V_{OS} = 1.2V$.

Note 8: t_{SKPP1} is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same supply voltage, input common-mode voltage, and ambient temperature.

Note 9: t_{SKPP2} is the magnitude difference of any differential propagation delays between devices operating over rated conditions.

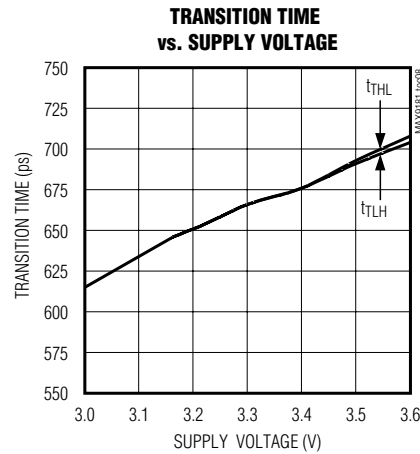
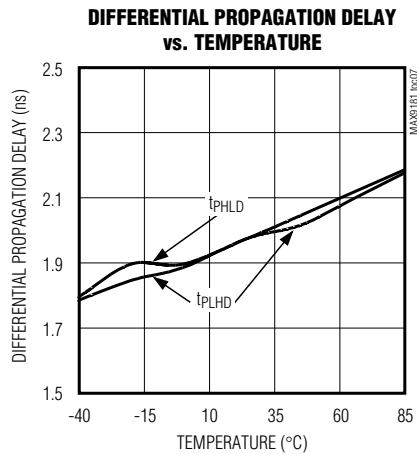
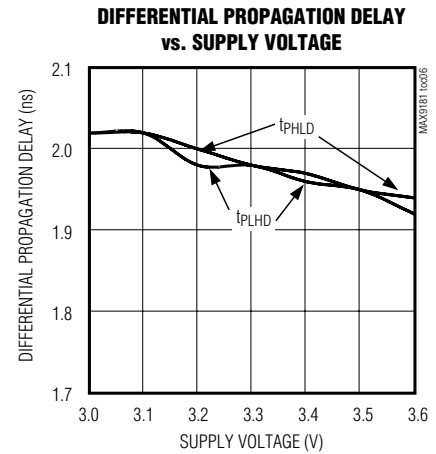
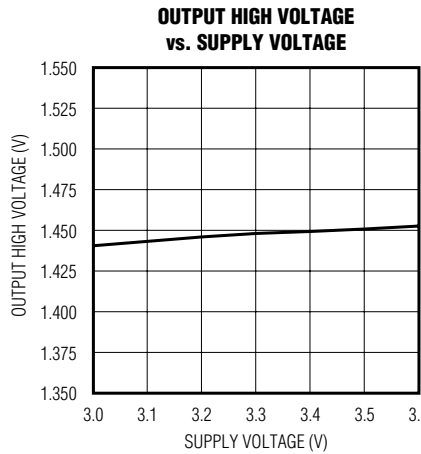
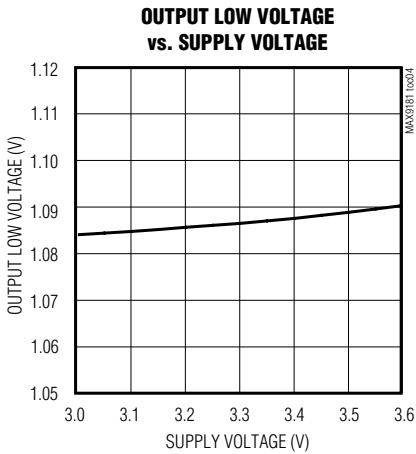
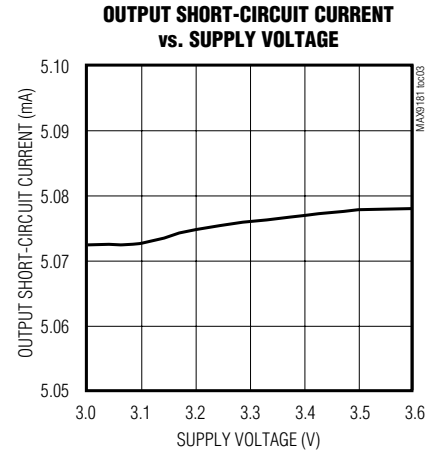
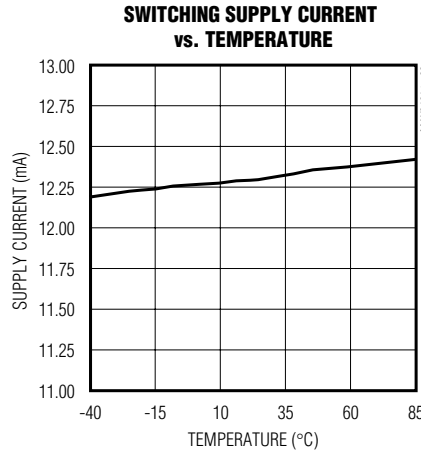
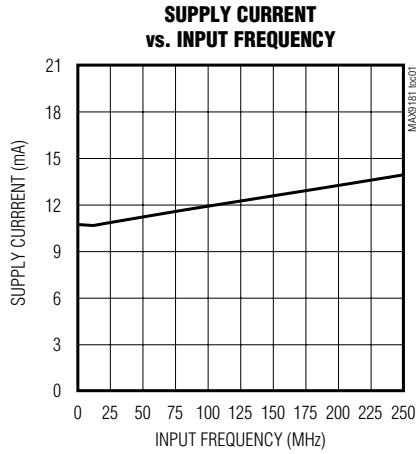
Note 10: Device meets V_{OD} DC specifications and AC specifications while operating at f_{MAX} .

Note 11: Jitter added to the input signal.

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Typical Operating Characteristics

($V_{CC} = 3.3V$, $R_L = 100\Omega \pm 1\%$, $C_L = 10pF$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ C$, unless otherwise noted. Signal generator output: frequency = 200MHz, 50% duty cycle, $R_O = 50\Omega$, $t_R = 1.5ns$, and $t_F = 1.5ns$ (0% to 100%), unless otherwise noted.)

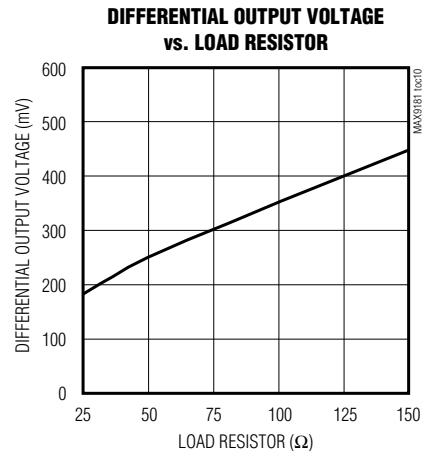
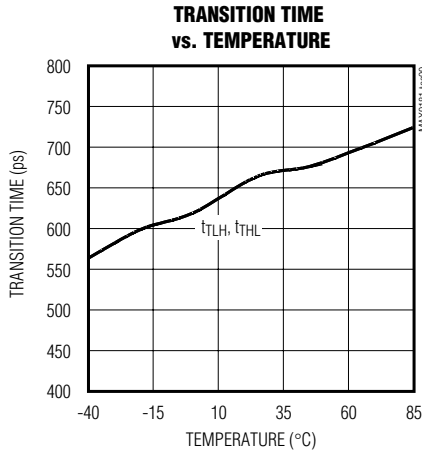


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Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $R_L = 100\Omega \pm 1\%$, $C_L = 10pF$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ C$, unless otherwise noted. Signal generator output: frequency = 200MHz, 50% duty cycle, $R_O = 50\Omega$, $t_R = 1.5ns$, and $t_F = 1.5ns$ (0% to 100%), unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	OUT-	Inverting LVDS Output
2	GND	Ground
3	IN-	Inverting LVPECL-Compatible Input
4	IN+	Noninverting LVPECL-Compatible Input
5	V _{CC}	Power Supply. Bypass V _{CC} to GND with a 0.01μF ceramic capacitor.
6	OUT+	Noninverting LVDS Output

Table 1. Function Table (Figure 2)

INPUT, V _{ID}	OUTPUT, V _{OD}
≥50mV	High
≤-50mV	Low
50mV > V _{ID} > -50mV	Indeterminate
Open	High

Note: $V_{ID} = (IN+ - IN-)$, $V_{OD} = (OUT+ - OUT-)$
 High = 450mV ≥ V_{OD} ≥ 250mV
 Low = -250mV ≥ V_{OD} ≥ -450mV

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium, as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9181 is a 400Mbps LVDS translator intended for high-speed, point-to-point, low-power applications. The MAX9181 accepts differential LVPECL inputs and produces an LVDS output. The input voltage range includes signals from GND up to V_{CC}, allowing interoperability with 3.3V LVPECL devices.

The MAX9181 provides a high output when the inputs are open. See Table 1.

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Applications Information

Supply Bypassing

Bypass V_{CC} with a high-frequency surface-mount ceramic $0.01\mu\text{F}$ capacitor as close to the device as possible.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9181. Use controlled-impedance differential traces. Ensure that noise couples as common mode by running the traces within a differential pair close together.

Maintain the distance within a differential pair to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

The LVDS standards define signal levels for interconnect with a differential characteristic impedance and termination of 100Ω . Interconnects with a characteristic impedance and termination of 90Ω to 132Ω impedance are allowed, but produce different signal levels (see *Termination*).

LVPECL signals are typically specified for 50Ω single-ended characteristic impedance interconnect terminated through 50Ω to $V_{CC} - 2V$.

Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Termination

For point-to-point LVDS links, the termination resistor should be located at the LVDS receiver input and

match the differential characteristic impedance of the transmission line.

Each line of a differential LVPECL link should be terminated through 50Ω to $V_{CC} - 2V$ or be replaced by the Thevinin equivalent.

The LVDS output voltage level depends upon the differential characteristic impedance of the interconnect and the value of the termination resistance. The MAX9181 is guaranteed to produce LVDS output levels into 100Ω . With the typical 3.6mA output current, the MAX9181 produces an output voltage of 360mV when driving a 100Ω transmission line terminated with a 100Ω termination resistor ($3.6\text{mA} \times 100\Omega = 360\text{mV}$). For typical output levels with different loads, see the Differential Output Voltage vs. Load Resistor curve in the *Typical Operating Characteristics*.

Chip Information

TRANSISTOR COUNT: 401

PROCESS: CMOS

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Test Circuits and Timing Diagrams

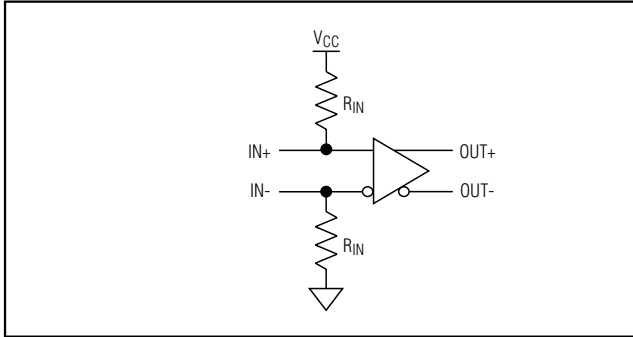


Figure 1. LVPECL Input Bias

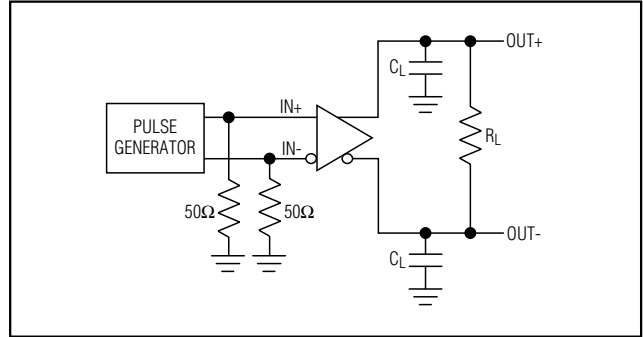


Figure 3. Transition Time and Propagation Delay Test Circuit

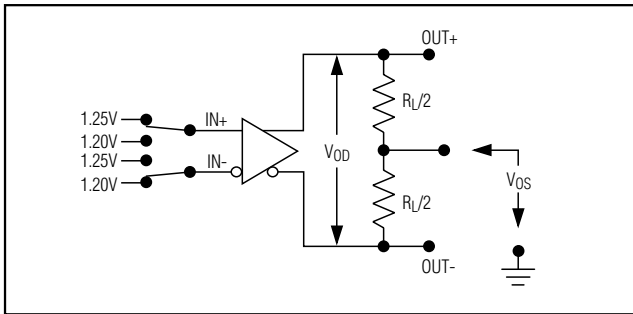


Figure 2. DC Load Test Circuit

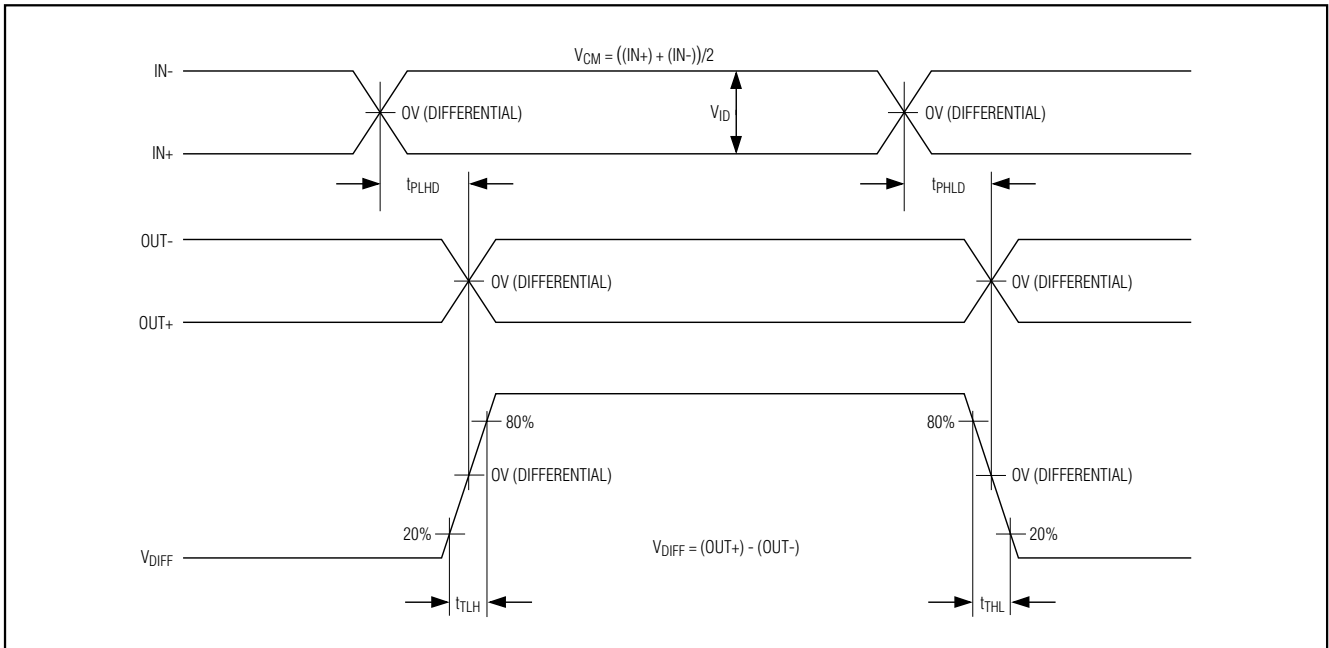
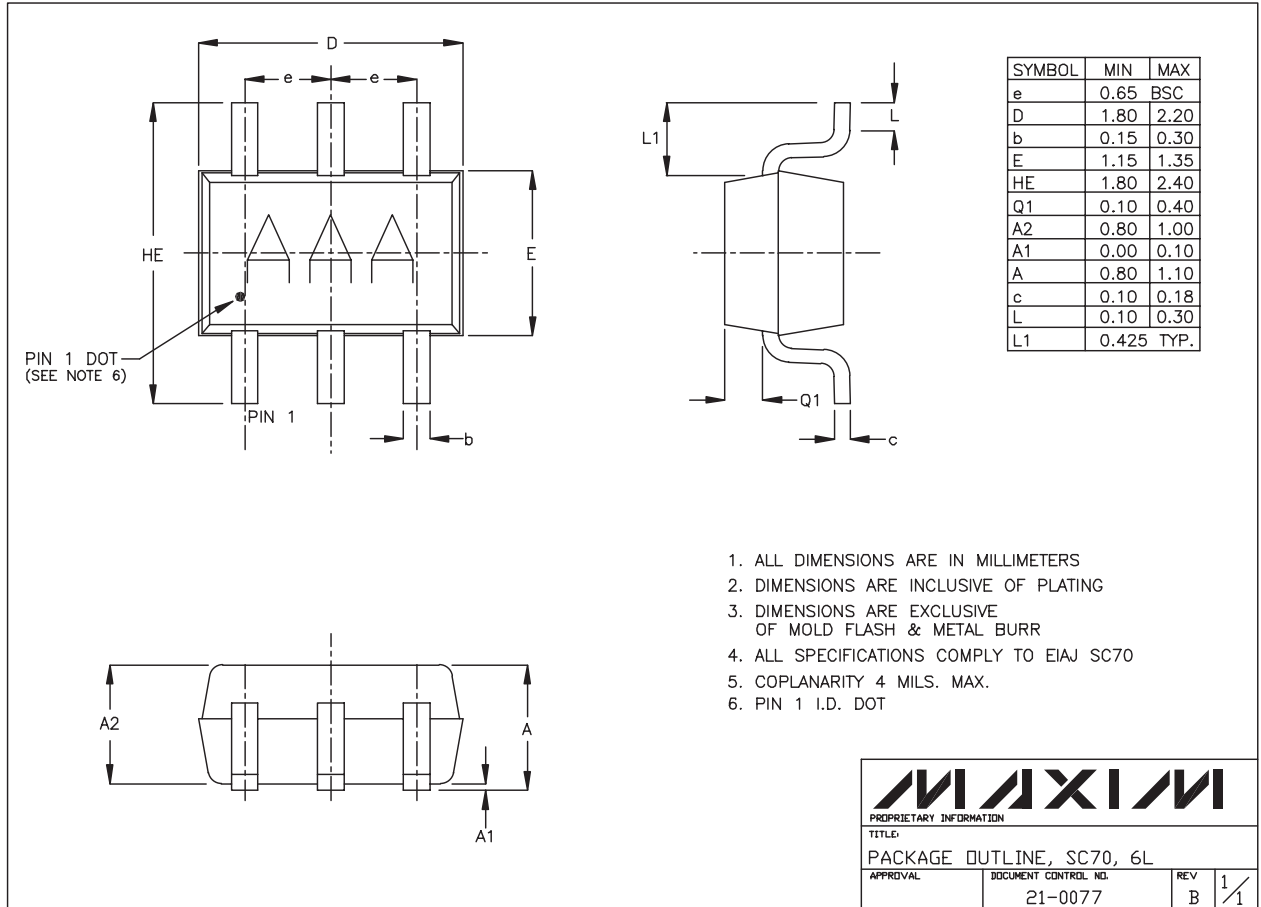


Figure 4. Transition Time and Propagation Delay Timing Diagram

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



SC70, 6L EPS

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SC70, 6L

APPROVAL	DOCUMENT CONTROL NO. 21-0077	REV B
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