OKI Semiconductor

MSM9841

Recording and Playback IC with Built-in FIFO

Contents

Preliminary

OKI Semiconductor

This version: Jun. 1999
Previous version: Mar. 1999

MSM9841

Recording and Playback LSI with Built-in FIFO

GENERAL DESCRIPTION

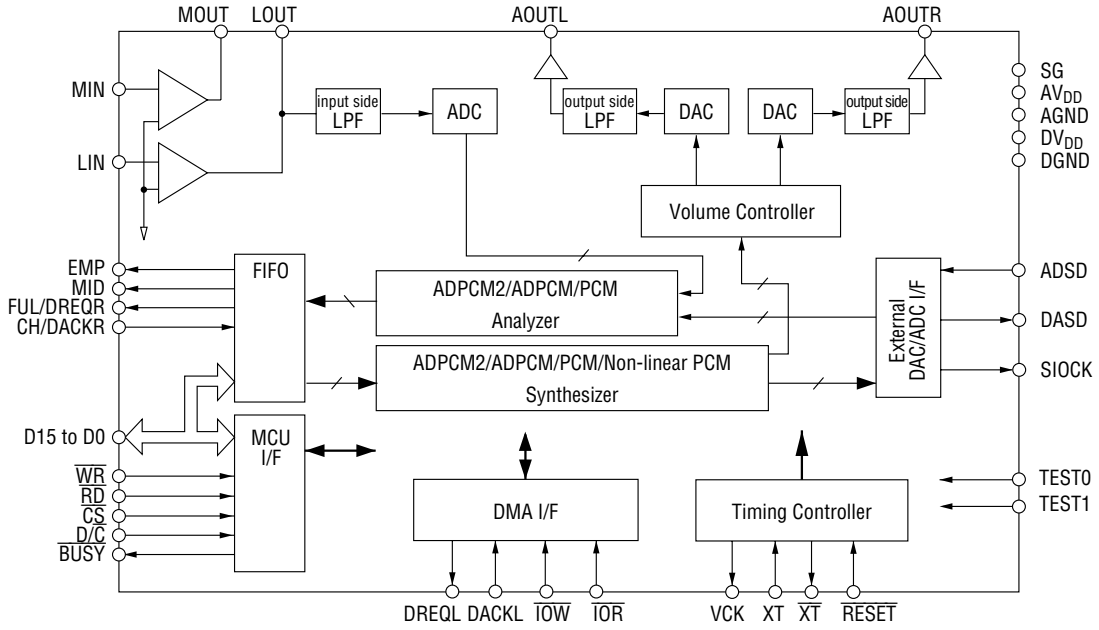
The MSM9841 is a mono/stereo record and playback LSI with a built-in 1K bit FIFO for easy interface with external systems or non-semiconductor memory. It utilizes multiple record and playback modes, including the new ADPCM2 algorithm, which allows for even higher quality sound reproduction. The record and playback functions of the MSM9841 is controlled by an MCU via 8/16-bit bus interface.

FEATURES

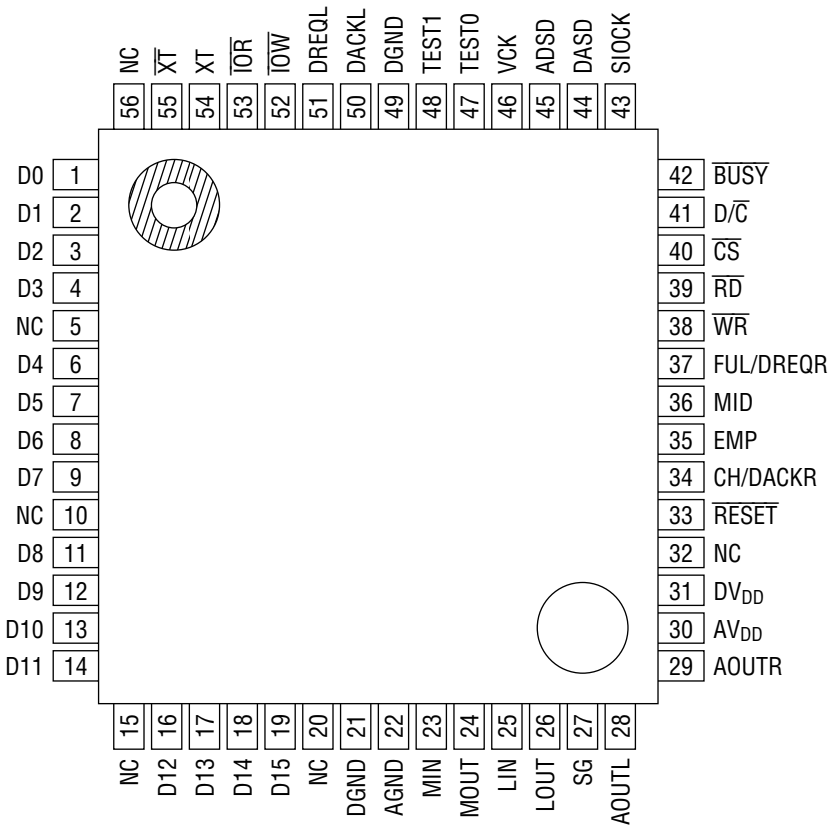
- 16/8-bit bus interface support
- FIFO capacity: User-definable (256/512/1024 bits)
  (buffering time of 32 ms when using 8 kHz sampling frequency, 4-bit ADPCM2/ADPCM, and in monaural playback)
- Supports four compression algorithms for record and playback:
  4, 5, 6, 7, 8-bit ADPCM2; 4-bit ADPCM; 8; 16-bit PCM; and 8-bit Nonlinear PCM
- Sampling frequency: 4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz* (fosc=4.096 MHz)
- Sampling frequency: 22.05 kHz*, 44.1 kHz* (fosc=5.6448 MHz)
- For the built-in ADC, set the sampling frequency at 16 kHz or less.
- DMA interface support
- Volume control (8 steps: 0 dB to –21 dB)
- Built-in 14-bit A/D converter
- Built-in 14-bit D/A converter
- Built-in low pass filter (LPF) : (input side: analog LPF)
  : (output side: digital LPF)
- Power supply voltage: 2.7 V to 5.5 V
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM9841GS-2K)

*note 32 kHz, 22.05 kHz and 44.1 kHz are available only for playback.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No Connection

56-pin plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
D15-D8	I/O	For 8-bit bus interface, the command allows these pins to be configured to be inputs or outputs to input or output data to and from an external memory. Otherwise, these pins are configured to be inputs only. For 16-bit interface, these pins are a bidirectional data bus to input or output data to and from an external microcontroller and memory.
D7-D0	I/O	Birirectional data bus to input or output data and output status to and from an external microcontroller and memory.
$\overline{WR}$	I	Write pulse input pin. This pin pulses "L" when command or voice data is input to D15-D0 pins.
$\overline{RD}$	I	Read pulse input pin. This pin pulses "L" when status or voice data is output to D15-D0 pins.
$\overline{CS}$	I	Accepts write pulse and read pulse when this pin is "L". Does not accept write pulse and read pulse when this pin is "H".
D/$\overline{C}$	I	Voice data is input or output to and from D15-D0 pins when this pin is "H". Command is input to and status is output from D7-D0 pins when this pin is "L".
$\overline{BUSY}$	O	This pin outputs a "L" level during RECORDING, PLAYBACK or PAUSE.
EMP	O	"H" level indicates that there is no data in FIFO memory. Active "H" can be changed to active "L" by command input.
MID	O	"H" level indicates that more than half of the FIFO memory space is filled with data. During playback, voice synthesis starts when MID changes to "H" level. Active "H" can be changed to active "L" by command input. This pin outputs a synchro signal for voice data input/output when non-use of FIFO is selected.
FUL/DREQR	O	"H" level indicates that FIFO memory is full of data. During playback, this pin is "H" and data cannot be written in FIFO memory. Active "H" can be changed to active "L" by command input. When DMA transfer and stereo playback are selected, "H" level DREQR outputs a signal to request a DMA transfer. Active "H" can be changed to active "L" by command input.
CH/DACKR	I	When stereo playback is selected and CH is "H", the EMP, MID or FUL pin outputs the status of right FIFO memory. When CH is "L", the EMP, MID or FUL pin outputs the status of left FIFO memory. Set this pin to "L" during recording and monophonic playback. When DMA transfer and stereo playback are selected, DACKR is selected. In this case, input a DMA transfer acknowledge signal to DACKR. When DACKR is "L", the $\overline{IOW}$ signal is accepted. Active "L" can be changed to active "H" by command input.
DREQL	O	When DMA transfer is selected, "H" level DREQL outputs a signal to request a DMA transfer. When stereo playback is selected, "H" level DREQL outputs a signal to request a DMA transfer. Active "H" can be changed to active "L" by command input.
DACKL	I	Input to DACKL a signal when DMA transfer is permitted by the DMA controller. When DACKL is "L", $\overline{IOR}$ and $\overline{IOW}$ signals are accepted. When stereo playback is selected, input to DACKL a DMA transfer acknowledge signal for left FIFO memory. Active "L" can be changed to active "H" by command input. If DMA transfer is not used, set this pin to "H" level.

PIN DESCRIPTIONS

Symbol	Type	Description
$\overline{IOW}$	I	Write pulse input pin to write external memory data to MSM9841 during DMA transfer. If DMA transfer is not used, set this pin to "H" level.
$\overline{IOR}$	I	Read pulse input pin to read data of MSM9841 during DMA transfer. If DMA transfer is not used, set this pin to "H" level.
ADSD	I	16-bit serial data input pin when external ADC is used. If external ADC is not used, set this pin to "L" level.
DASD	O	16-bit serial data output pin when external DAC is used.
SIOCK	O	Synchronizing clock for 16-bit serial data input/output when external ADC or DAC is used.
XT $\overline{XT}$	I O	Oscillator connection pins. When external clock is used, input clock into XT pin and leave $\overline{XT}$ pin open.
VCK	O	Outputs sampling frequency selected at recording or playback. VCK pin is used as a synchronizing signal when external ADC or DAC is used.
$\overline{RESET}$	I	When this pin is "L" level input, the LSI is initialized.
TEST0 TEST1	I	Pins for testing. Set the pins to "L".
SG	O	Analog circuit signal ground output pin.
MIN LIN	I	Inverting input pin for built-in OP amplifier. Noninverting input pin is connected to SG (Signal Ground) internally.
MOUT LOUT	O	MOUT is the output of internal OP amplifier to MIN, and LOUT is to LIN.
AOUTL	O	Left analog output pin from built-in LPF. This is the output pin of playback wavefroms, and is connected to the amplifier for driving speakers.
AOUTR	O	Right analog output pin from built-in LPF. This is the output pin of playback wavefroms, and is connected to the amplifier for driving speakers.
DV_{DD}	—	Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin.
DGND	—	Digital GND pin.
AV_{DD}	—	Analog power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and AGND pin.
AGND	—	Analog GND pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +155	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	DGND=AGND=0V	2.7 to 5.5			V
Operating Temperature	T_{OP}	—	–40 to +85			°C
Master Clock Frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			4.0	4.096	6.0	

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD}=AV_{DD}=2.7 to 5.5V, DGND=AGND=0V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	V_{DD}×0.85	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	V_{DD}×0.2	V
High-level output Voltage	V_{OH}	I_{OH}=–40 µA	V_{DD}–0.3	—	—	V
Low-level output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High-level Input Current (*1)	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High-level Input Current (*2)	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
High-level Input Current (*3)	I_{IH3}	DV_{DD}=AV_{DD}=4.5 to 5.5 V, V_{IH}=V_{DD}	30	150	300	µA
		DV_{DD}=AV_{DD}=2.7 to 3.6 V, V_{IH}=V_{DD}	10	50	100	µA
Low-level Input Current (*1)	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low-level Input Current (*2)	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Operating Current consumption	I_{DD}	DV_{DD}=AV_{DD}=4.5 to 5.5 V, fosc=4.096 MHz, whithout load	—	15	30	mA
		DV_{DD}=AV_{DD}=2.7 to 3.6 V, fosc=4.096 MHz, whithout load	—	10	20	mA
Stanby Current consumption	I_{DDS}	At power down, without load Ta=–40 to +70°C	—	—	10	µA
		At power down, without load Ta=–40 to +85°C	—	—	50	µA

*1 Applicable to input pins excluding XT pin.
*2 Applicable to XT pin.
*3 Applicable to TEST0 pin and TEST1 pin.

Analog Characteristics

DV_{DD}=AV_{DD}=2.7 to 5.5V, DGND=AGND=0V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\|V_{DAE}\|$	No load	—	—	10	mV
LOUT Allowable Voltage Range	V_{LOUT}	DV_{DD}=AV_{DD}=4.5 V to 5.5 V	1	—	V_{DD}–1	V
		DV_{DD}=AV_{DD}=2.7 V to 3.6 V	0.25V_{DD}	—	0.75V_{DD}	V
OP Amplifier Open Loop Gain	Gop	f_{IN}=0 to 4 kHz	40	—	—	dB
OP Amplifier Input Impedance	R_{INA}	—	1	—	—	MΩ
OP Amplifier Output Load	R_{OUTA}	—	200	—	—	kΩ
AOUTL Output Load	R_{AOL}	—	50	—	—	kΩ
AOUTR Output Load	R_{AOR}	—	50	—	—	kΩ
DAC Output Impedance	R_{DAO}	When DAC output is selected.	15	25	35	kΩ
AOUTL, AOUTR output impedance during standby mode	R_{SAO}	During standby mode or power down mode	15	25	35	kΩ

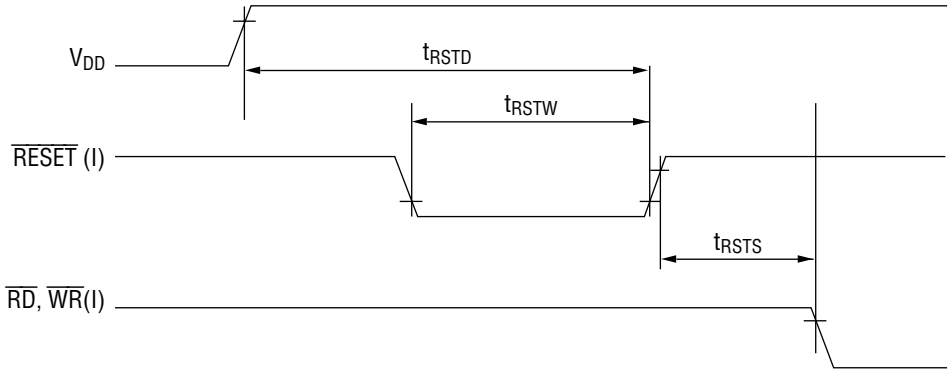
AC Characteristics

DV_{DD}=AV_{DD}=2.7 to 5.5V, DGND=AGND=0V, Ta=–40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{RESET}$ Pulse Width	t_{RSTW}	300	—	—	ns
Setup Time after Rise of Power Supply for Fall of $\overline{RESET}$	t_{RSTD}	500	—	—	ns
Time to Active First $\overline{RD}$, $\overline{WR}$ after Fall of $\overline{RESET}$	t_{RSTS}	200	—	—	ns
$\overline{RD}$ Pulse Width	t_{RR}	160	—	—	ns
$\overline{CS}$, D/$\overline{C}$, CH Setup and Hold Time for $\overline{RD}$	t_{CR}	30	—	—	ns
Time from Fall of $\overline{RD}$ till Data and Status Definition	t_{DRE}	—	—	120	ns
Time from Fall of $\overline{RD}$ till Data Float	t_{DRF}	—	10	50	ns
Time from Rise of $\overline{RD}$ till Fall of Next $\overline{RD}$ (1) during status read	t_{CRC}	500	—	—	ns
Time from Rise of $\overline{RD}$ till Fall of Next $\overline{RD}$ (2) during data read	t_{CRC}	200	—	—	ns
$\overline{WR}$ Pulse Width	t_{WW}	160	—	—	ns
$\overline{CS}$, D/$\overline{C}$, CH Setup and Hold Time for $\overline{WR}$	t_{CW}	30	—	—	ns
Setup Time of Data, and Command for Rise of $\overline{WR}$	t_{DWS}	100	—	—	ns
Setup Time of REC and PLAY Command for Rise of $\overline{WR}$	t_{DWS}	t_{WW}+50	—	—	ns
Hold Time of Data, and Command for Rise of $\overline{WR}$	t_{DWH}	10	—	—	ns
Time from Rise of $\overline{WR}$ till Fall of Next $\overline{WR}$ (1) during command write	t_{CWC}	500	—	—	ns
Time from Rise of $\overline{WR}$ till Fall of Next $\overline{WR}$ (2) during data write	t_{CWC}	200	—	—	ns
Time from Rise of MID till rise of $\overline{RD}$ (For synchro timing when FIFO memory is not used)	t_{MR}	2	—	15	µs
Time from Rise of MID till rise of $\overline{WR}$ (For synchro timing when FIFO memory is not used)	t_{MW}	2	—	15	µs
MID pulse width (For synchro timing when FIFO memory is not used)	t_{MM}	15.6	—	125	µs
$\overline{IOR}$ Pulse Width	t_{IORW}	160	—	—	ns
Setup and Hold Time of DACKL/R for $\overline{IOR}$	t_{DR}	10	—	—	ns
Time from Fall of $\overline{IOR}$ till Data Definition	t_{IORE}	—	—	160	ns
Time from Fall of $\overline{IOR}$ till Data Float	t_{IORF}	—	10	50	ns
Time from Rise of $\overline{IOR}$ till Fall of Next $\overline{IOR}$	t_{IORC}	200	—	—	ns
$\overline{IOW}$ Pulse Width	t_{IOWW}	160	—	—	ns
Setup and Hold Time of DACKL/R for $\overline{IOW}$	t_{DW}	10	—	—	ns
Setup Time of Data for Rise of $\overline{IOW}$	t_{IOWS}	100	—	—	ns
Hold Time of Data for Rise of $\overline{IOW}$	t_{IOWH}	10	—	—	ns
Time from Rise of $\overline{IOW}$ till Fall of Next $\overline{IOW}$	t_{IOWC}	200	—	—	ns

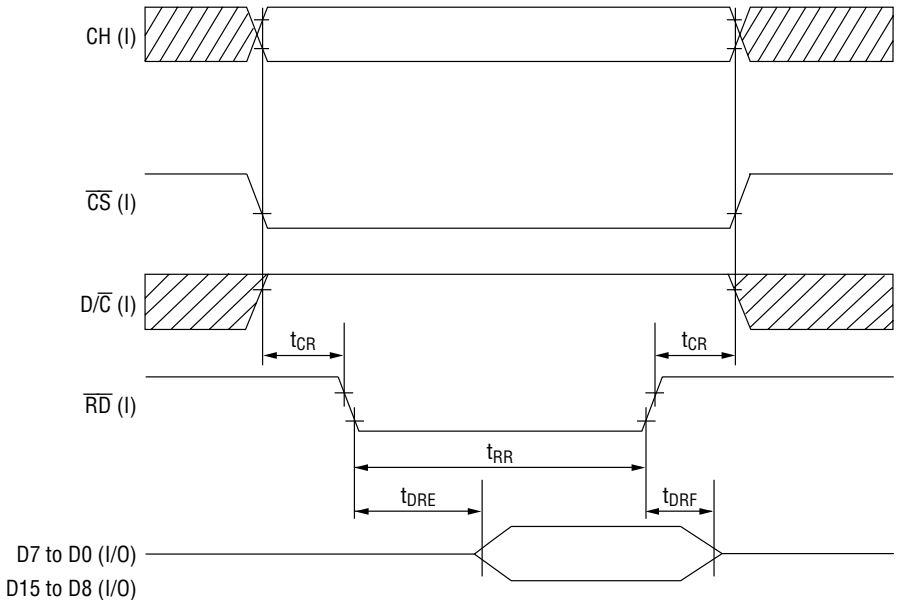
TIMING DIAGRAMS

Reset Timing

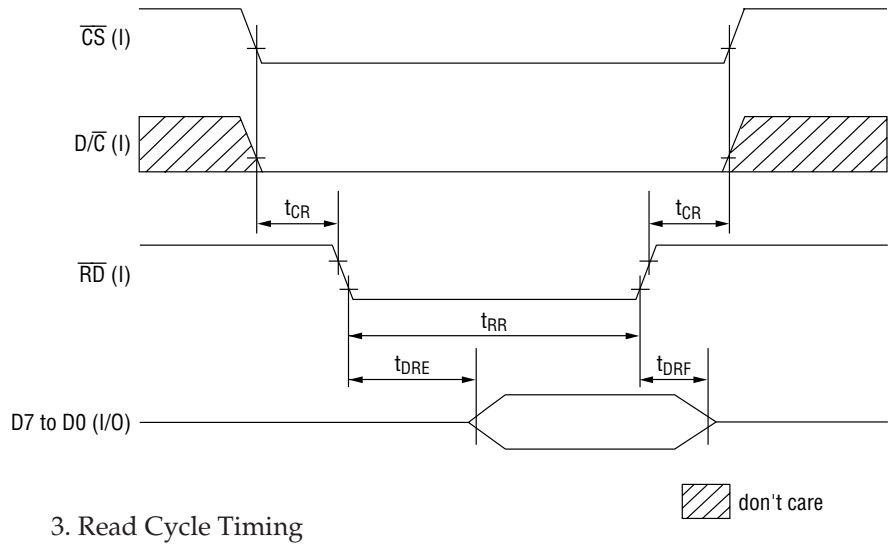


Read Timing

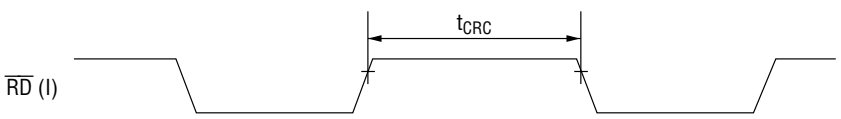
1. Data Read Timing



2. Status Read Timing

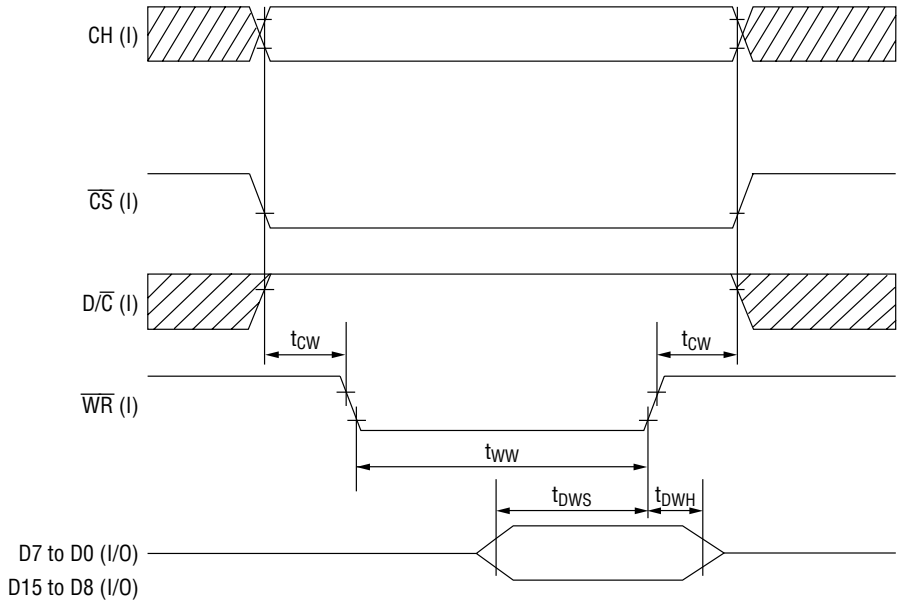


3. Read Cycle Timing

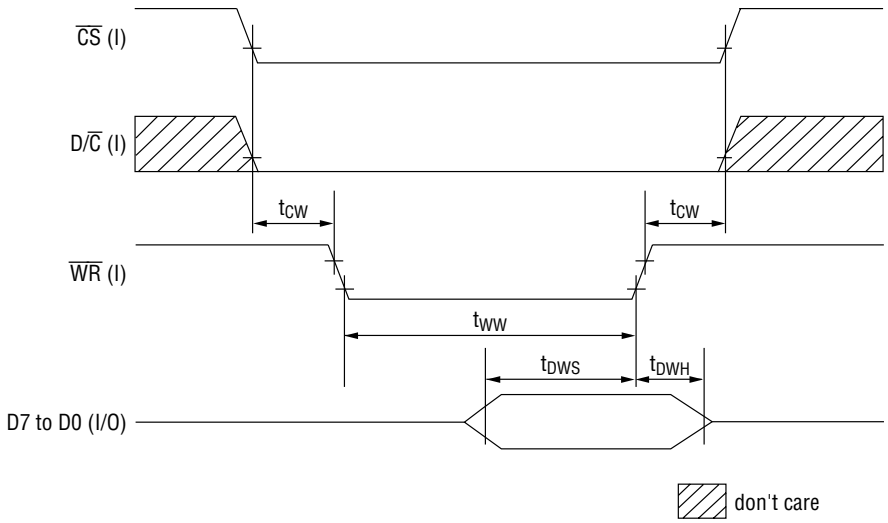


Write Timing

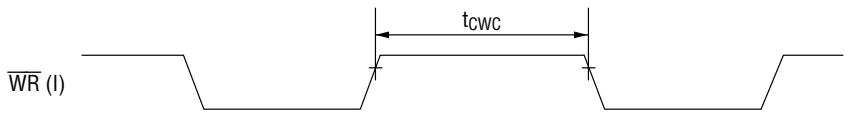
1. Data Write Timing



2. Command Write Timing

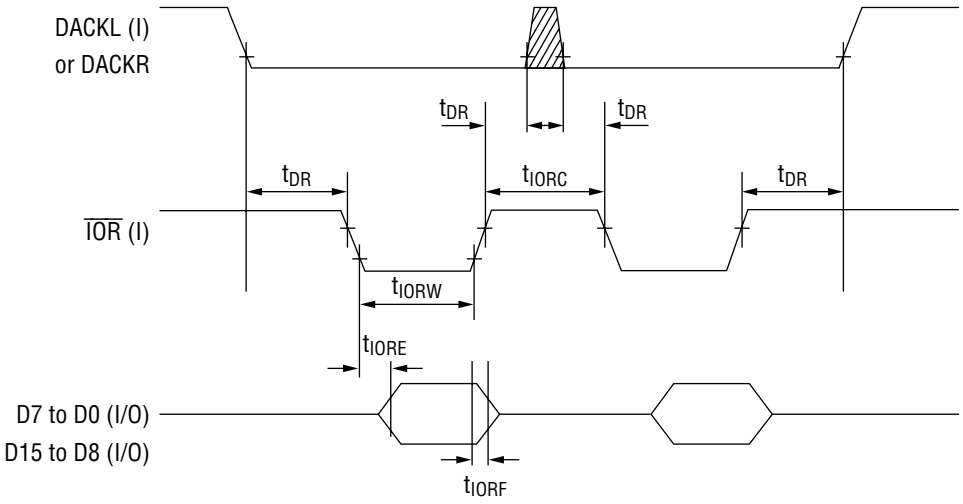


3. Write Cycle Timing

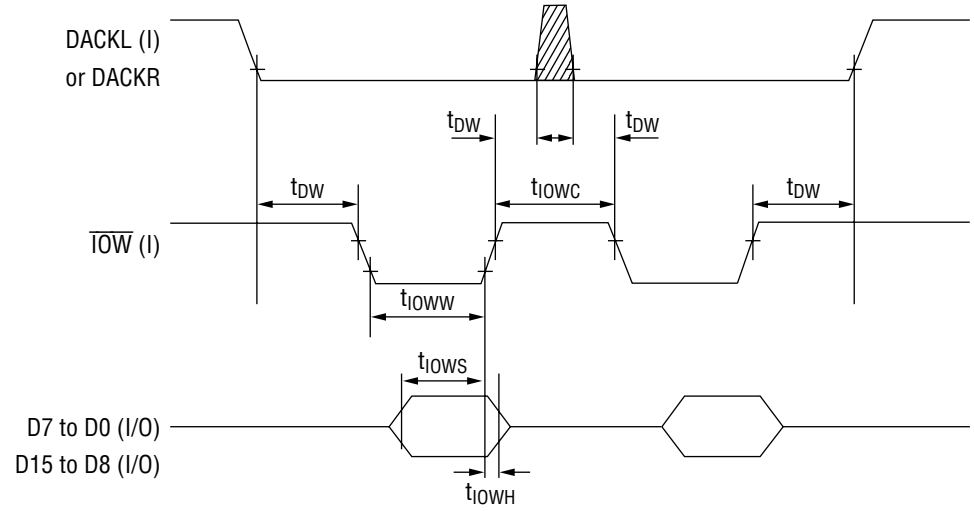


DMA Transfer Timing

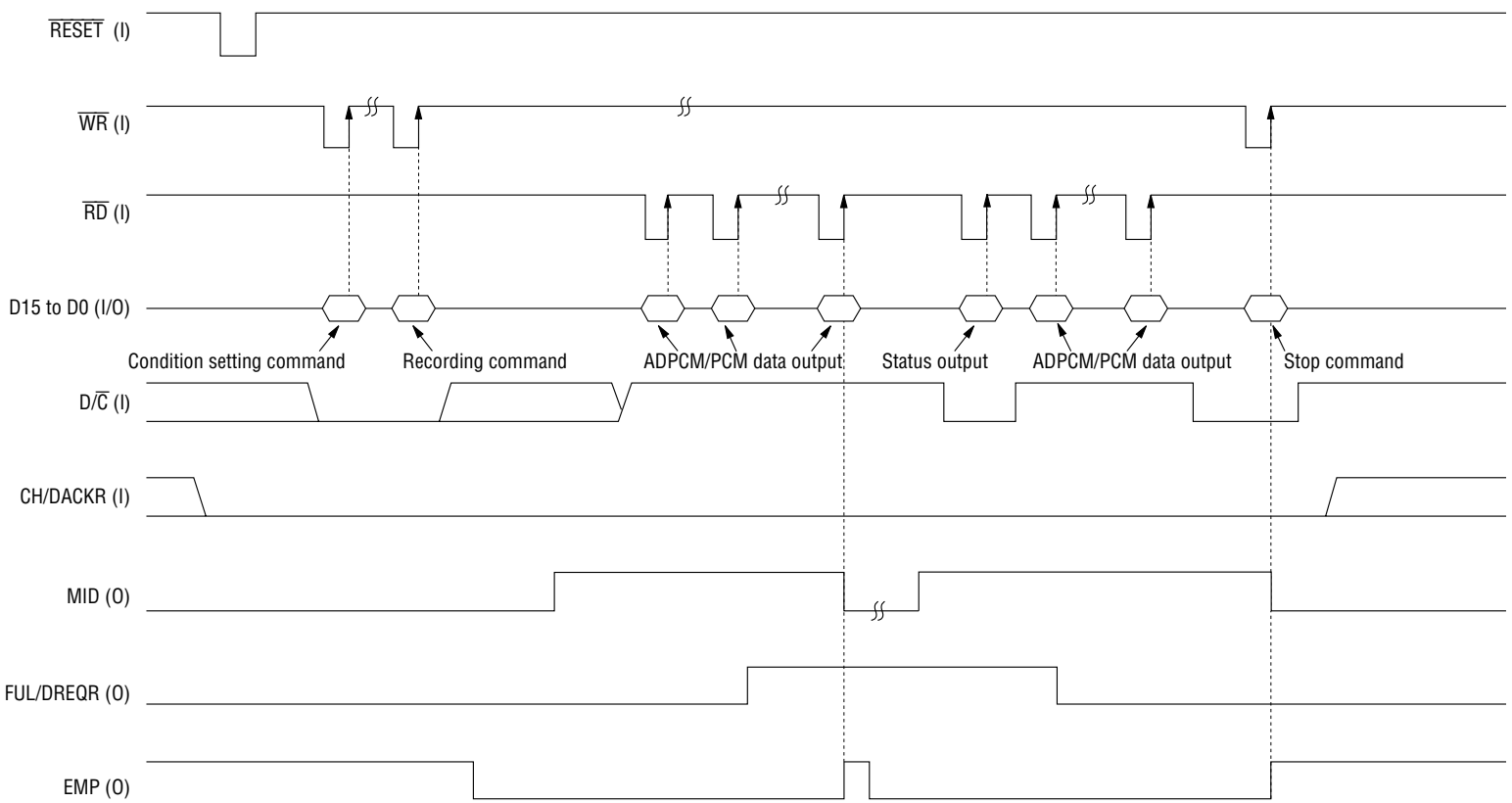
1. $\overline{IOR}$ (during recording and 2-byte reading)



2. $\overline{IOW}$ (during playback and 2-byte writing)



Recording Timing (When FIFO memory is used)

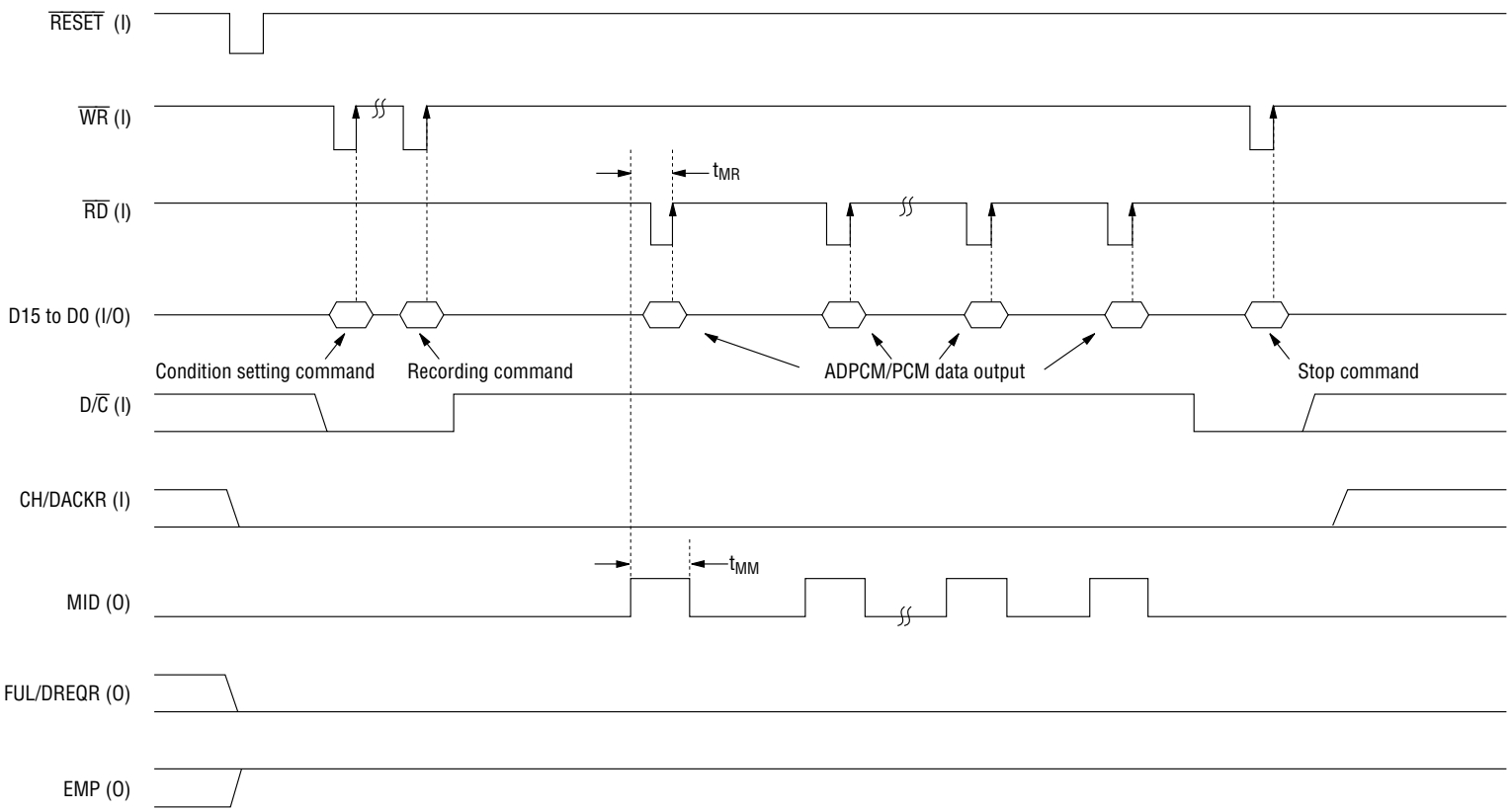


Note 1) 16-bit PCM recording is impossible when 8-bit Bus is selected.
8-bit PCM recording and 8-bit OKI non-linear PCM recording are impossible when 16-bit Bus is selected.

Note 2) Enter a condition setting command for every item to be set.

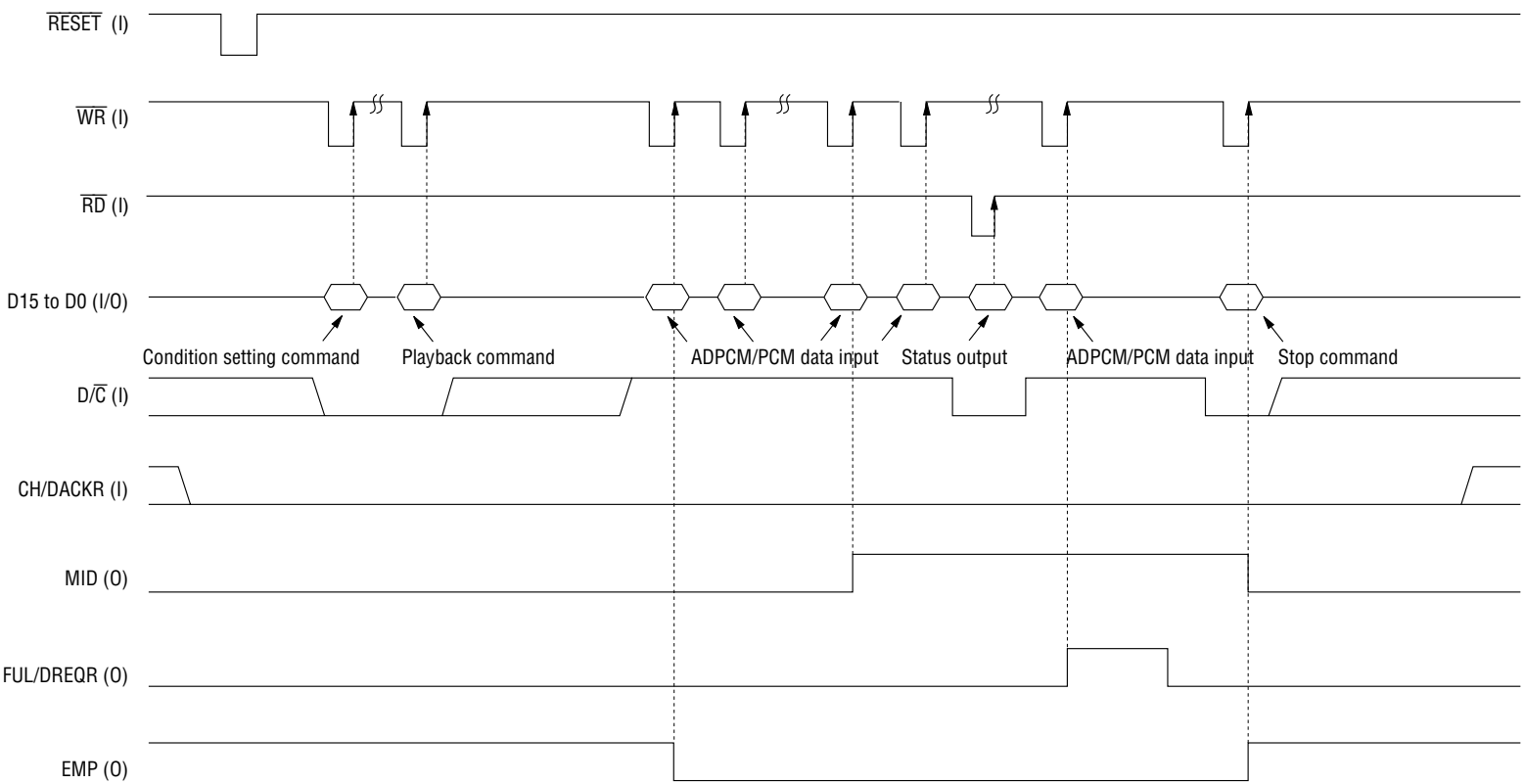
Note 3) When you selected 64 words FIFO, you need to transfer 32 words during one sampling clock after FUL and DREQR go "H" level.

Recording Timing (When FIFO memory is not used)



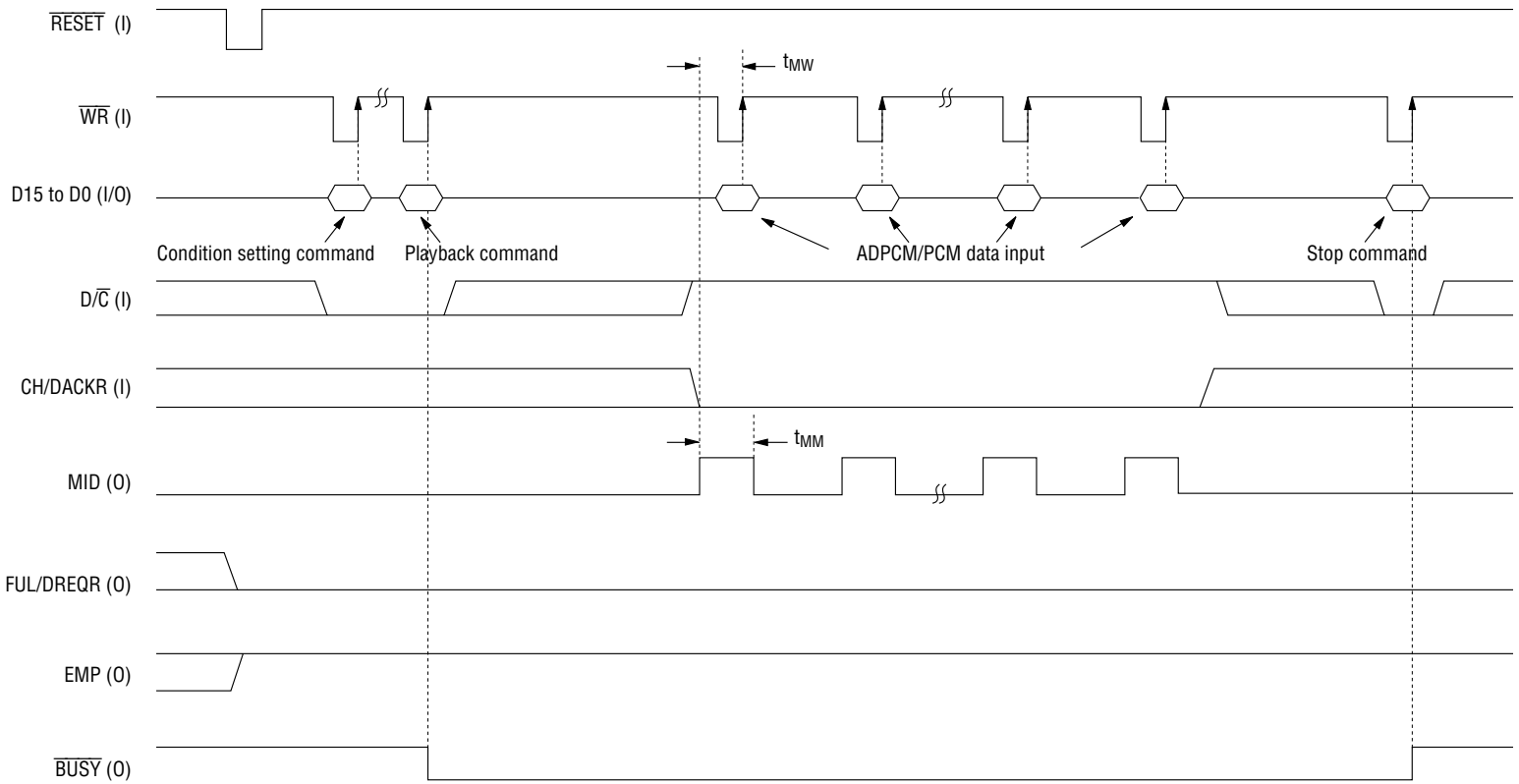
Note) Enter a condition setting command for every item to be set.

Monaural Playback Timing (When FIFO memory is used)



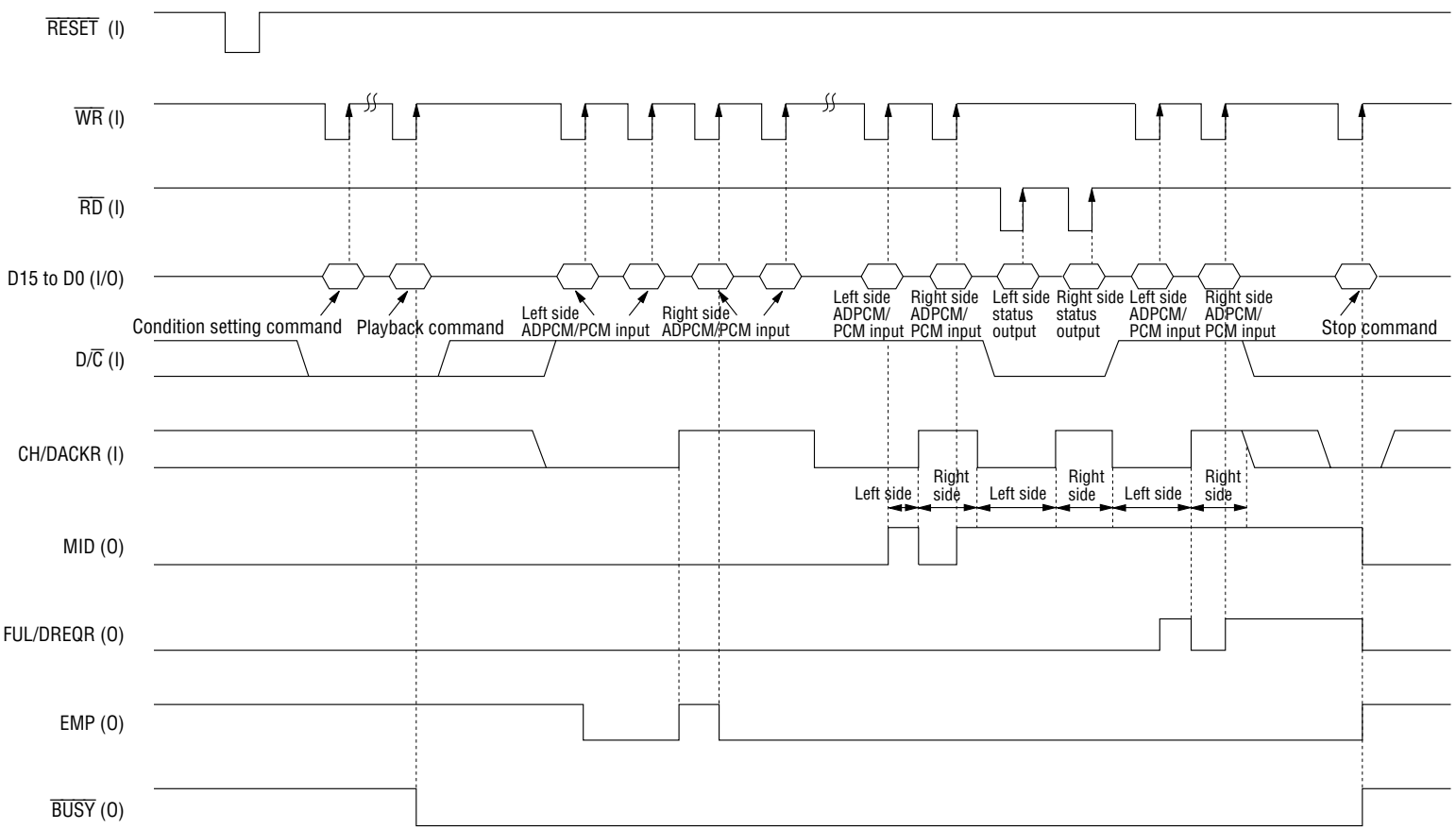
Note) Enter a condition setting command for every item to be set.

Monaural Playback Timing (When FIFO is not used)



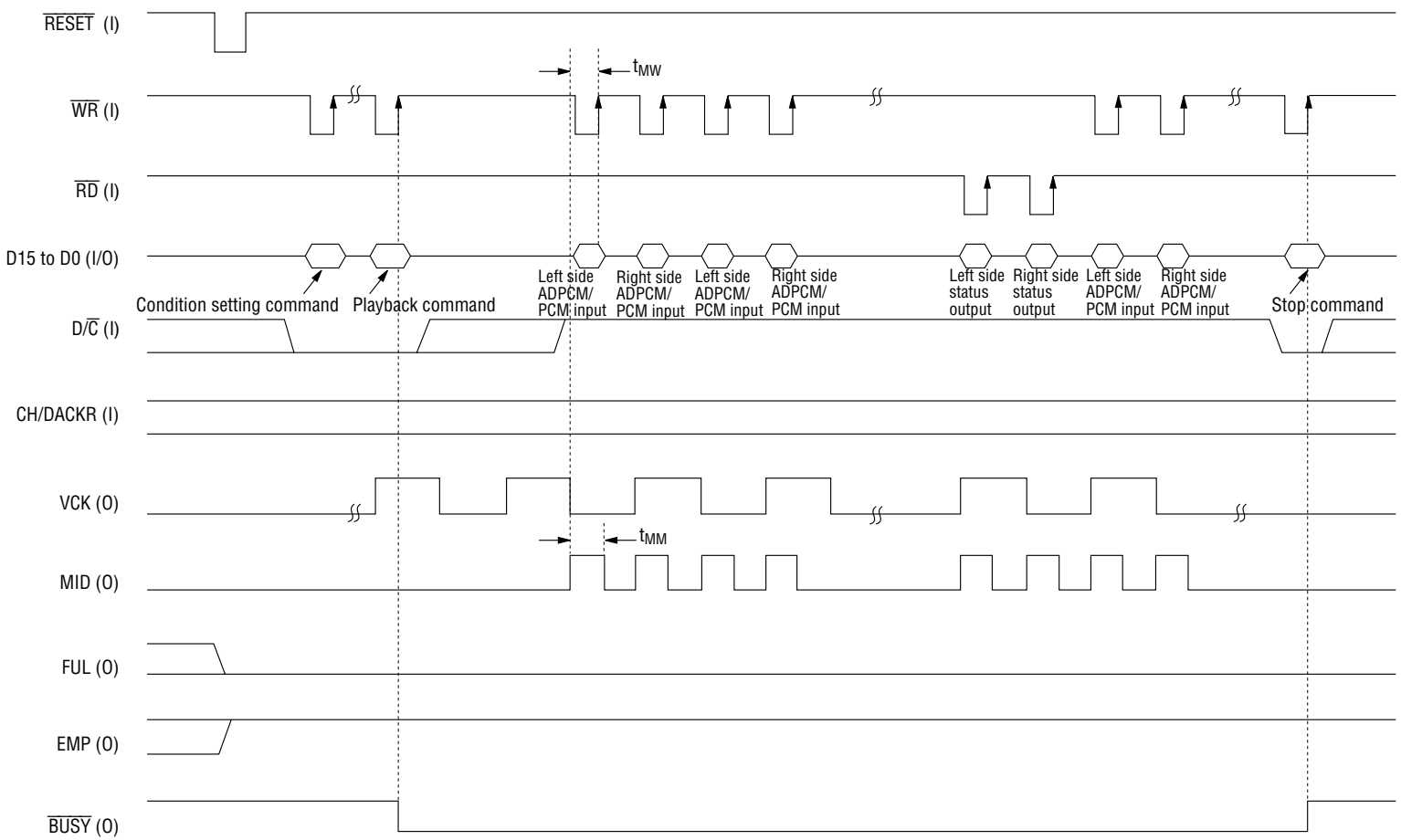
Note) Enter a condition setting command for every item to be set.

Stereo Playback Timing (When FIFO memory is used)



Note) Enter a condition setting command for every item to be set.

Stereo Playback Timing (When FIFO memory is not used)



Note) Enter a condition setting command for every item to be set.

FUNCTIONAL DESCRIPTION

Voice synthesis method

The MSM9841 supports four PCM methods to process various kinds of voices :4-bit ADPCM; 4-, 5-, 6-, 7-, or 8-bit ADPCM2; 8- or 16-bit straight PCM; and 8-bit non-linear PCM methods.

1. 4-bit ADPCM method (Adaptive Differential Pulse Code Modulation)
   This method encodes 4-bit data while adaptively varying the basic quantization width "Δ" at each sampling. This method reduces storage requirements by storing differences between successive digital samples rather than full values. This method very effectively processes human and animal voices and natural sounds, reducing voice data storage space. This method offers high sound reproduction quality.

2. 4-, 5-, 6-, 7-, or 8-bit ADPCM2 method
   This method has higher sound reproduction quality than the ADPCM method. The ADPCM2 method offers five compression methods (4-, 5-, 6-, 7-, or 8-bit). Note that data used in the 4-bit ADPCM method is not compatible with data in the 4-bit ADPCM2 method.
   Data conversion for these methods can be made by a development tool, AR204.

3. 8- or 16-bit straight PCM method
   This method has the highest sound reproduction characteristics in all frequencies (of the above four PCM methods). This method is suitable for sound effects having high frequencies and sounds having pulse-like waveforms.

4. 8-bit non-linear PCM method
   The method emphasizes the value of the center of each sound wave and processes it with 10 bit perceived accuracy. It is effective in improving the tone quality of frequency low voices and sounds.

Voice synthesis methods and sampling frequencies during recording and playback

The voice synthesis methods available during recording and playback and sampling frequency not available during recording with internal ADC are shown below.

Setup / Voice synthesis method	Recording		Playback			
	Monaural		Monaural		Stereo	
	8bit Bus	16bit Bus	8bit Bus	16bit Bus	8bit Bus	16bit Bus
4-bit ADPCM	✔	✔	✔	✔	✔	✔
4- to 8-bit ADPCM2	✔	✔	✔	✔	✔	✔
8-bit PCM	✔		✔	✔	✔	✔
16-bit PCM		✔	✔	✔	✔	✔
8-bit non-linear PCM			✔	✔	✔	✔

Sampling frequency	Recording	Playback	
	Monaural	Monaural	Stereo
4.0 to 16.0kHz	✔	✔	✔
22.05 kHz, 32 kHz, 44.1 kHz	*	✔	✔

*note It is available with an external ADC

Data configuration for each voice synthesis method

Input/output data configuration are shown as bellows at recording and playback.
When you selected 8-bit bus, you select which you use D15 to D8 pins or D7 to D0 pins.
If you want to use D15 to D8 pins, please refer to replacing D7 to D0.

Data configuration when 8-bit bus is used

"X" outputs "L" level during recording and is "don't care" during playback.

1. 4-bit ADPCM method and 4-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2

2. 5-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	×	×	MSB1	4SB1	3SB1	2SB1	LSB1

3. 6-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	×	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1

4. 7-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

6. 16-bit straight PCM method

D7	D6	D5	D4	D3	D2	D1	D0	
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1	1st transfer
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1	2nd transfer

Data configuration when 16-bit bus is used

"X" outputs "L" level during recording and is "don't care" during playback.

1. 4-bit ADPCM method and 4-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSB3	3SB3	2SB3	LSB3	MSB4	3SB4	2SB4	LSB4

2. 5-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	×	×	MSB1	4SB1	3SB1	2SB1	LSB1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
×	×	×	MSB2	4SB2	3SB2	2SB2	LSB2

3. 6-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	×	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
×	×	MSB2	5SB2	4SB2	3SB2	2SB2	LSB2

4. 7-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
×	MSB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSB2	7SB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

6. 16-bit straight PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

FIFO memory configuration

The configuration of FIFO memory can be changed with command on the D7 to D0 pins. Select FIFO memory configuration for bus width, monaural/stereo, and buffering times. Initially, the FIFO memory is 512 bits (64 words by 8 bits).

(1) FIFO memory configuration when an 8-bit bus and at monaural reproduction are selected
The following three FIFO memory sizes are selectable by commands :
1024 bits (128 words by 8 bits)
512 bits (64 words by 8 bits, initial value)
256 bits (32 words by 8 bits)

(2) FIFO memory configuration when 16-bit bus and at monaural reproduction are selected
The following three FIFO memory sizes are selectable by commands :
1024 bits (64 words by 16 bits)
512 bits (32 words by 16 bits)
256 bits (16 words by 16 bits)

(3) FIFO memory configuration when an 8-bit bus and at stereo reproduction are selected
The following two FIFO memory sizes are selectable by commands :
512 bits (64 words by 8 bits) × 2
256 bits (32 words by 8 bits) × 2

(4) FIFO memory configuration when 16-bit bus and at stereo reproduction are selected
The following two FIFO memory sizes are selectable by commands :
512 bits (32 words by 16 bits) × 2
256 bits (16 words by 16 bits) × 2

Voice synthesis methods and maximum buffering times
FIFO capacity of 1024 bits and sampling frequency of 8 kHz

(1)	8-bit bus selected	(Monaural)	(Stereo)
	4-bit ADPCM2 or ADPCM :	32 ms	16 ms
	5-, 6-, 7-, and 8-bit ADPCM2 :	16 ms	8 ms
	8-bit PCM :	16 ms	8 ms
(2)	16-bit bus selected	(Monaural)	(Stereo)
	16-bit PCM :	16 ms	8 ms

The other methods are the same as those when the 8-bit bus is used.

Recording operation (8-bit bus, 512-bit FIFO configuration)

(1) Voice synthesis, sampling frequncy, and bus length are set with commands.
In the recording mode, the 8-bit non-linear PCM method is not available.
The 16-bit PCM method when 8-bit Bus is selected and 8-bit PCM method when 16-bit Bus is selected are not available.

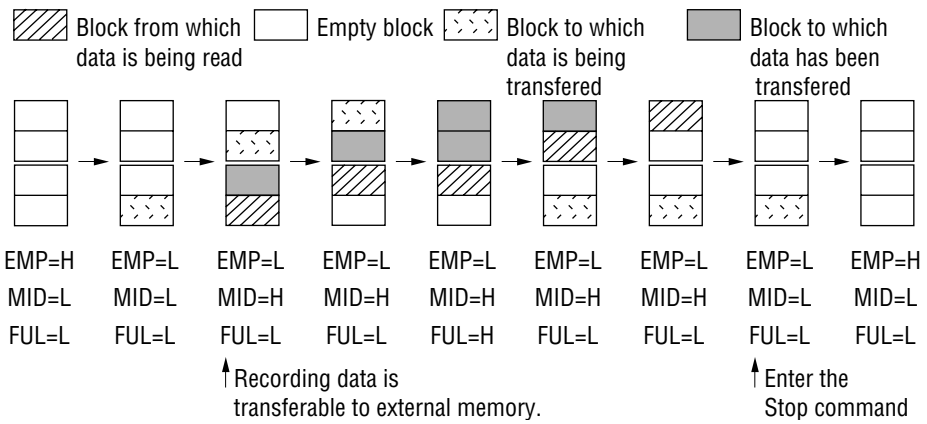
(2) Recording is started by a command.

(3) During recording, when the voice analyzer has written one word in FIFO, the EMP pin goes low.

(4) Status indication by EMP, MID, and FUL pins
- EMP="H", MID="L", FUL="L"
  No data is written in FIFO memory.
- EMP="L", MID="L," FUL="L"
  Data of 1 word to 31 words has been written in FIFO memory. In this state, data cannot be read from FIFO memory.
- EMP="L", MID="H", FUL="L"
  Data of 32 words to 63 words has been written in FIFO memory. While the MID pin is "H," you can read data from FIFO memory. When 32 words have been read from the FIFO memory, if MID="L", additional data can not be continuously read from the FIFO memory. If MID="H", additional 32 words can be continuously read from the FIFO memory.
- EMP="L," MID="H," FUL="H"
  Data of 64 words is written in FIFO memory
  In this state, it is required to set the FUL pin to "L" before next data is transfered to the FIFO memory. If the FUL pin fails to be set to "L", the data transfer error flag is set. The data transfer error flag can be monitored by status read.

(5) End of recording
Recording is terminated by a command. After Stop command is entered, the contents of the FIFO memory are cleared. Therefore, monitor the status of the EMP, MID and FUL pins before terminating recording after reading all FIFO memory data.

Change of FIFO memory status during recording



Playback operation (8-bit bus, 512-bit FIFO configuration)

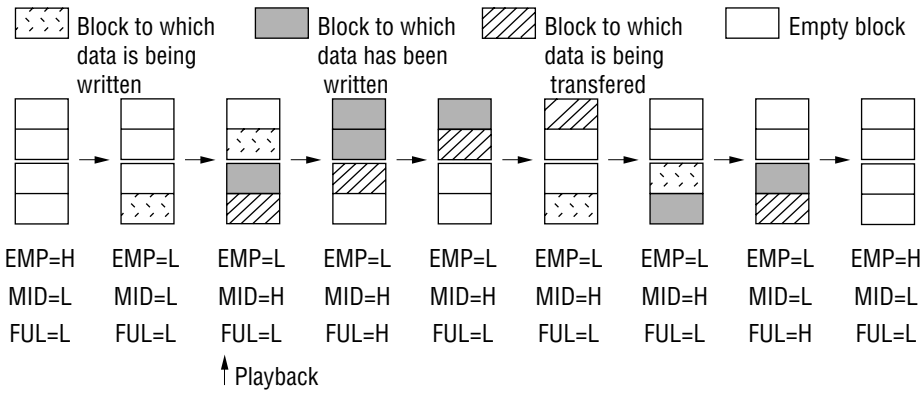
(1) Voice synthesis, sampling frequncy, bus length, and stereo playback modes can be set by commands.

(2) When a Playback Start command is entered or when data of 1 word is written in FIFO, the MSM9841 recognizes the start of playback and starts synthesizing voices when the MID pin goes high ("H").

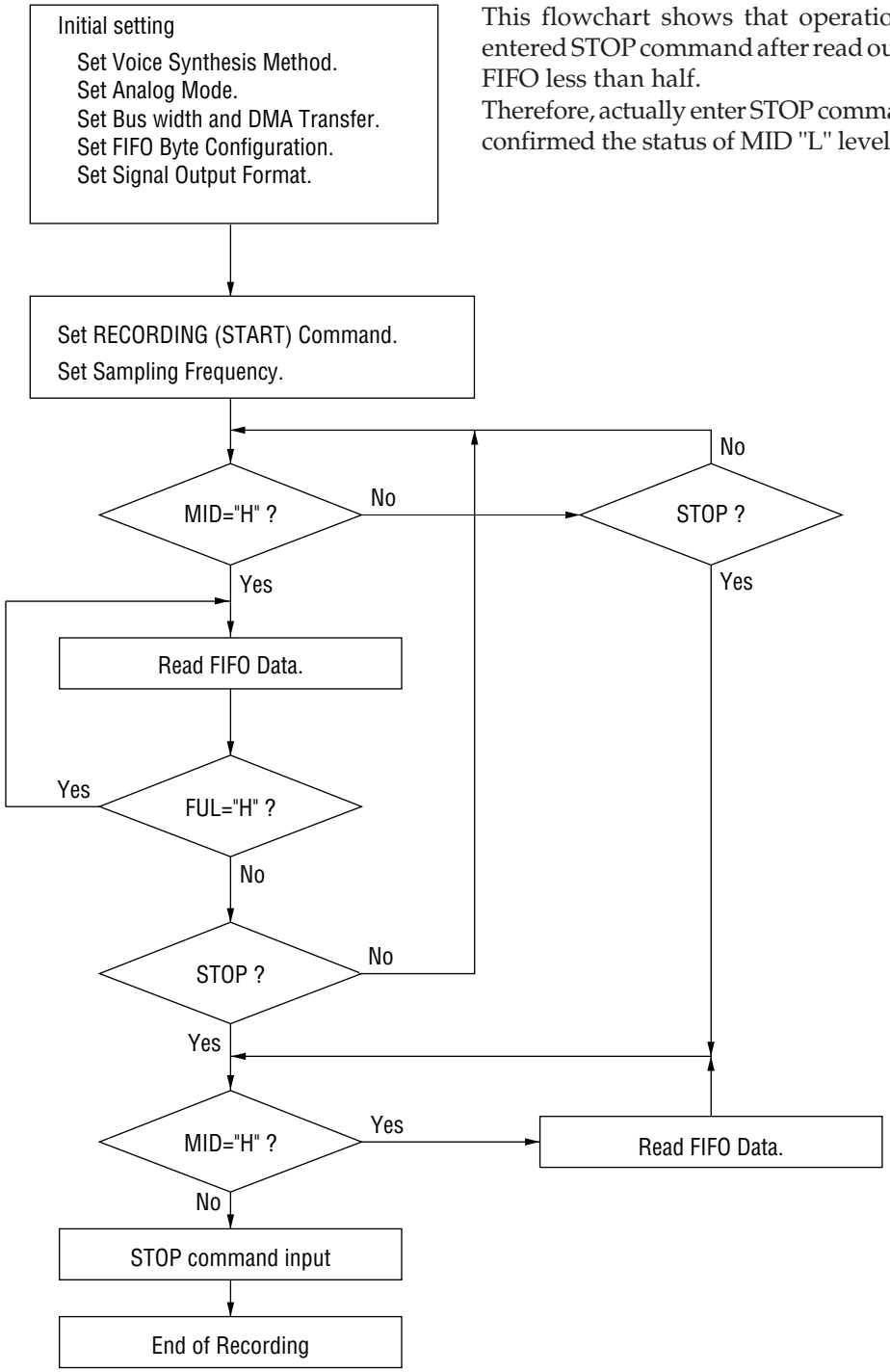
(3) Status indication by EMP, MID, and FUL pins (64 words FIFO memory configuration)
- EMP="H", MID="L", FUL="L"
  No data is written in FIFO memory.
- EMP="L", MID="L", FUL="L"
  Data of 1 word to 31 words has been written in FIFO memory. In this state, the voice synthesizer cannot read data from FIFO memory.
- EMP="L", MID="H", FUL="L"
  Data of 32 words to 63 words has been written in FIFO memory. While the MID pin is "H," the voice synthesizer can read data from FIFO memory. If the MID and FUL pins fail to be set to "H", when the voice synthesizer has completed reading 32 words from FIFO, the MID pin goes low.
- EMP="L," MID="H," FUL="H"
  Data of 64 words is written in FIFO memory
  In this state, writing of 32 words into FIFO is completed before the voice synthesizer reads 32 words from FIFO and no data can be written in FIFO memory.

(4) End of playback
In the case of EMP="L", MID="H", and FUL="L", if data is not written into the FIFO memory, playback is autimatically terminated. Playback also can be terminated with the Stop command. However, the FIFO memory data is cleared by input of the Stop command. The Stop command also can stop the playback the way.

Change of FIFO memory status during playback



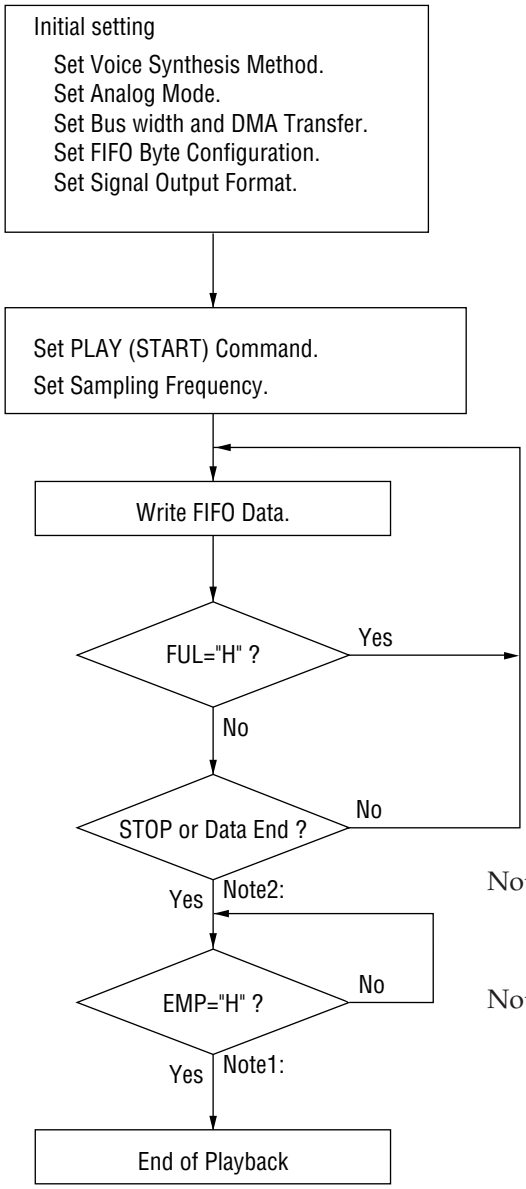
Recording Data Transfer Flowchart (without DMA transfer)



This flowchart shows that operations until entered STOP command after read out data in FIFO less than half.
Therefore, actually enter STOP command after confirmed the status of MID "L" level.

Note : At the STOP command is entered, EMP pin goes "H" and all data in FIFO is cleared.

Playback Data Transfer Flowchart (without DMA transfer)



Note1 : When the EMP pin is "H" during playback, the MSM9841 goes to stop playback.

Note2 : When a stop command is entered or when data writing ends, the last data is transferred to the LSI and the EMP pin goes high. With this, all data transfer is completed.
There are two cases to stop playback.
One case is by STOP command.
The other case is playback automatically stops after finishing data transfer.

DMA Control Method

The MSM9841 sends a DMA Transfer request to the DMA controller and waits for a DMA transfer permission from the DMA controller. Upon reception of the permission, the MSM9841 starts data transfer at a transfer cycle of the DMA controller. The DMA Transfer function is enabled or disabled by commands.
Default setting is disable.

DREQL and DREQR pins (8-bit bus, 512-bit FIFO configuration)
These pins are used to send a DMA Transfer request to the DMA controller. The amount of DMA transfer data is 32 words or 64 words, selected by commands.

(1) Playback. When the PLAY (START) command is entered, the DREQL or DREQR pin goes high to request a cycle to write data into FIFO memory. After playback status, the DREQL/R pins remain high until the 64-word write cycle is completed. When a 32-word write cycle is completed, voice synthesis starts. From now on, each time the amount of data in FIFO memory becomes half, the DREQL/R pins go high to send a request to DMA-transfer 32 words.
(2) Recording. Recording starts with a command. When data of 32 words has been transfered to FIFO memory from the voice analyzer, the DREQL/R pins go high to request a cycle to read 32 words from FIFO memory. From now on, each time 32 words has been transfered to FIFO memory, the DREQL/R pins go high to send a request to DMA-transfer of 32 words.

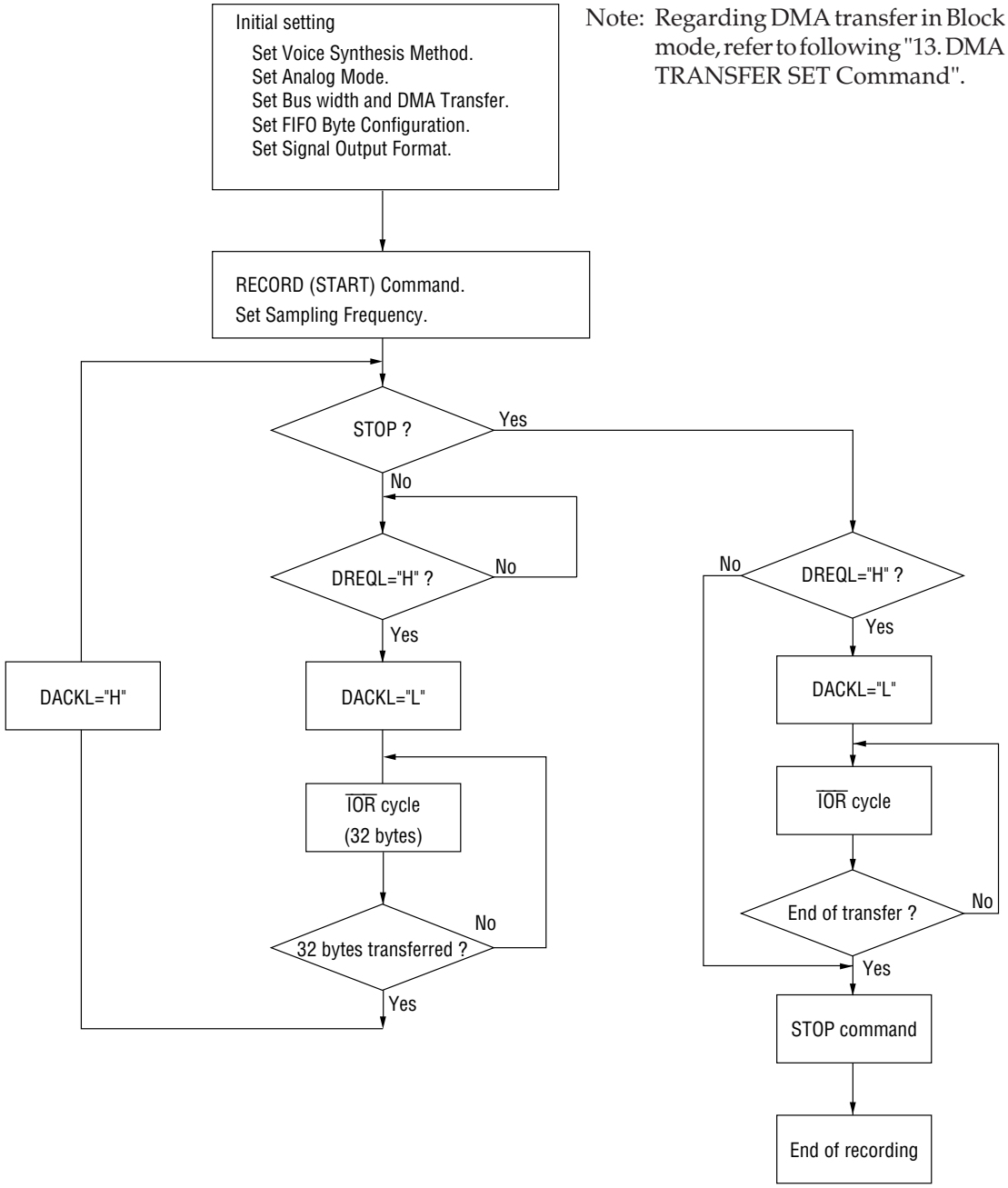
DACKL and DACKR

Connect these pins to a DMA Transfer acknowledge signal from the DMA controller. When the DACKL/DACKR pins are at a low level ("L"), the $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ pins are enabled.

$\overline{\text{IOW}}$ and $\overline{\text{IOR}}$

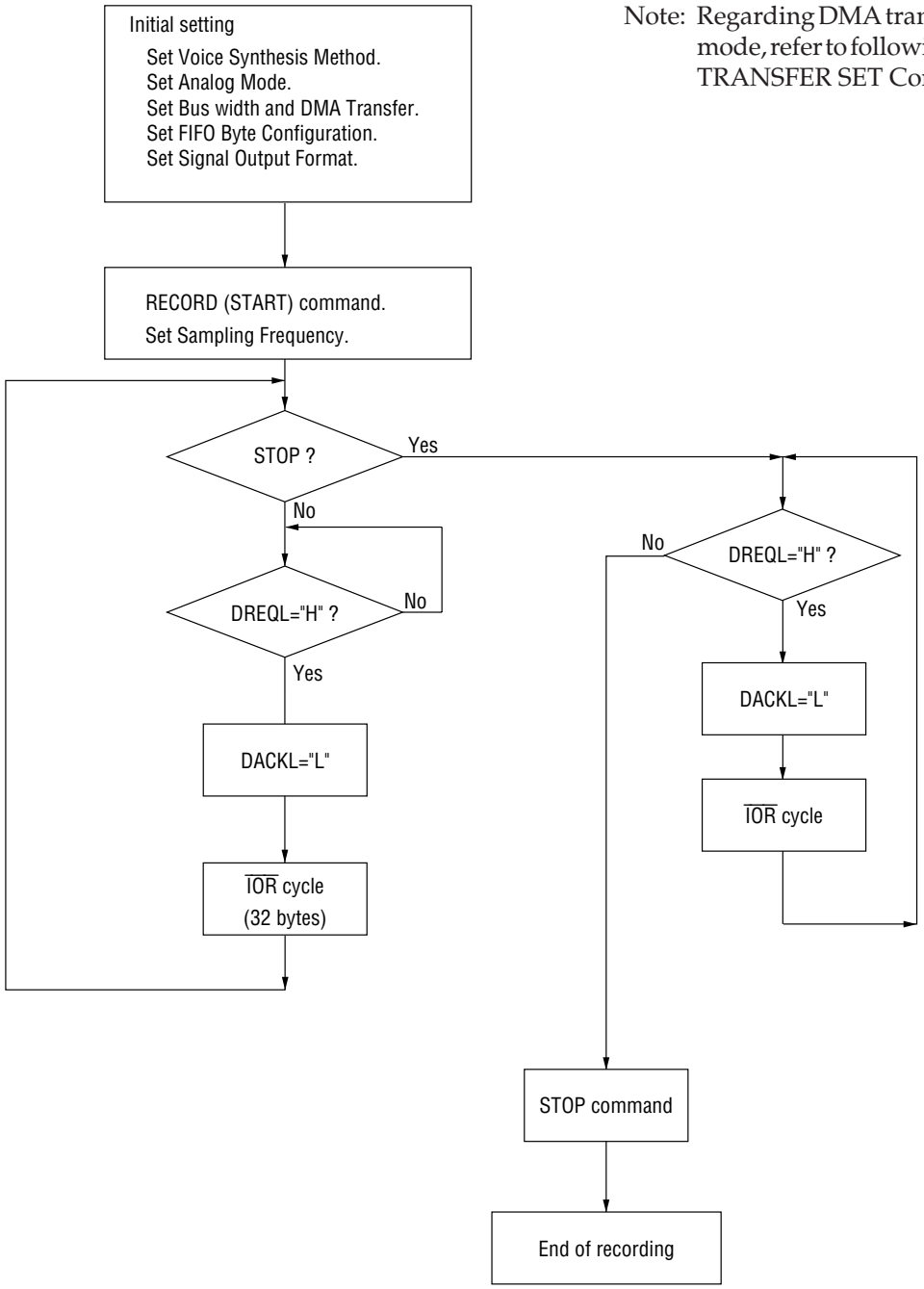
The $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ pins are enebled when the DACKL or DACKR pin goes low and their states are controlled by the DMA controller.
The $\overline{\text{IOW}}$ pin is an input pin to transfer data from external memory to the MSM9841.
The $\overline{\text{IOR}}$ pin is an input pin to transfer data from the MSM9841 to external memory.

Recording Data Transfer Flowchart (with DMA transfer in Block mode)



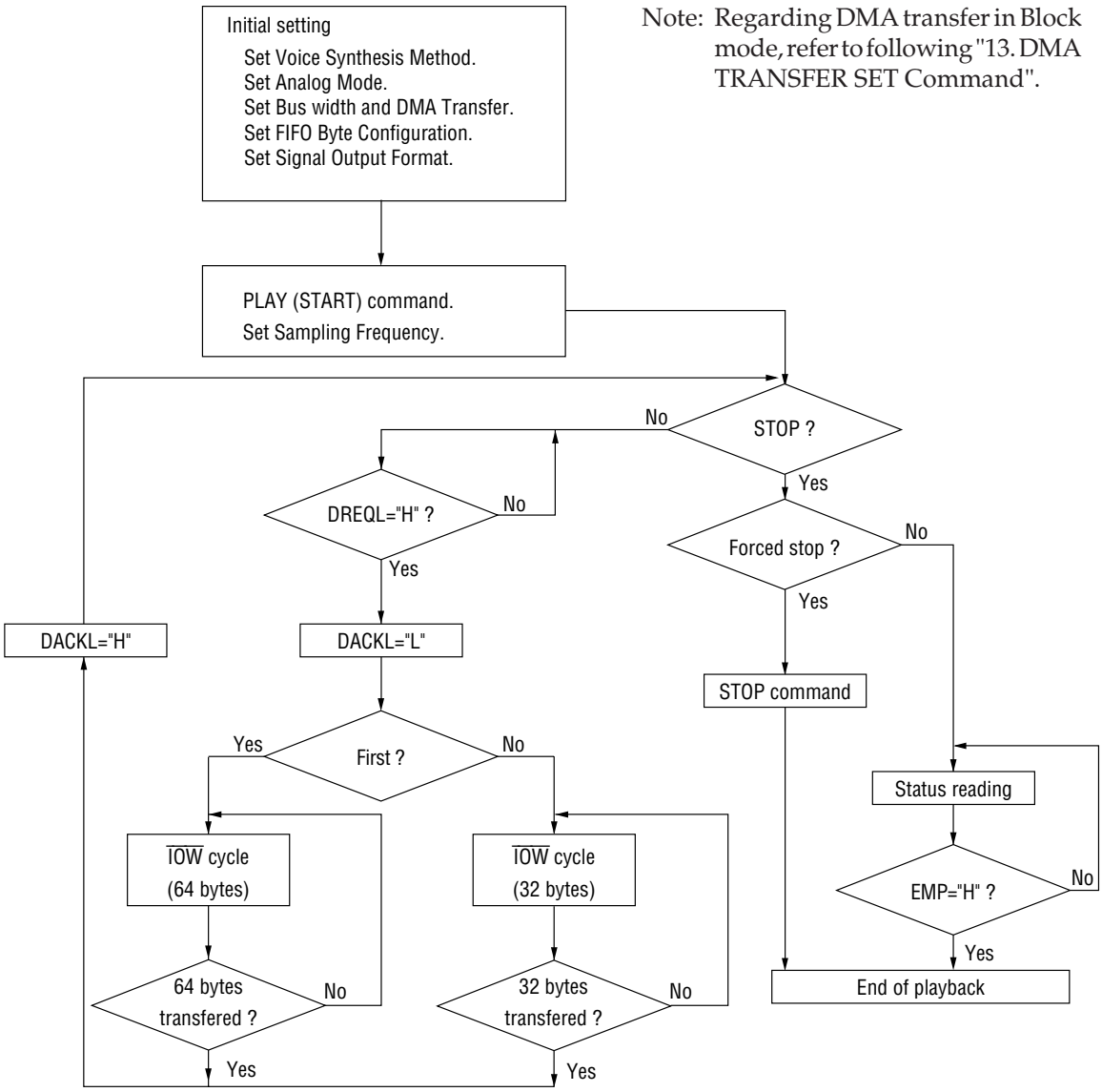
Note: Regarding DMA transfer in Block mode, refer to following "13. DMA TRANSFER SET Command".

Recording Data Transfer Flowchart (with DMA transfer in Single mode)



Note: Regarding DMA transfer in single mode, refer to following "13. DMA TRANSFER SET Command".

Playback Data Transfer Flowchart (with DMA transfer in Block mode)

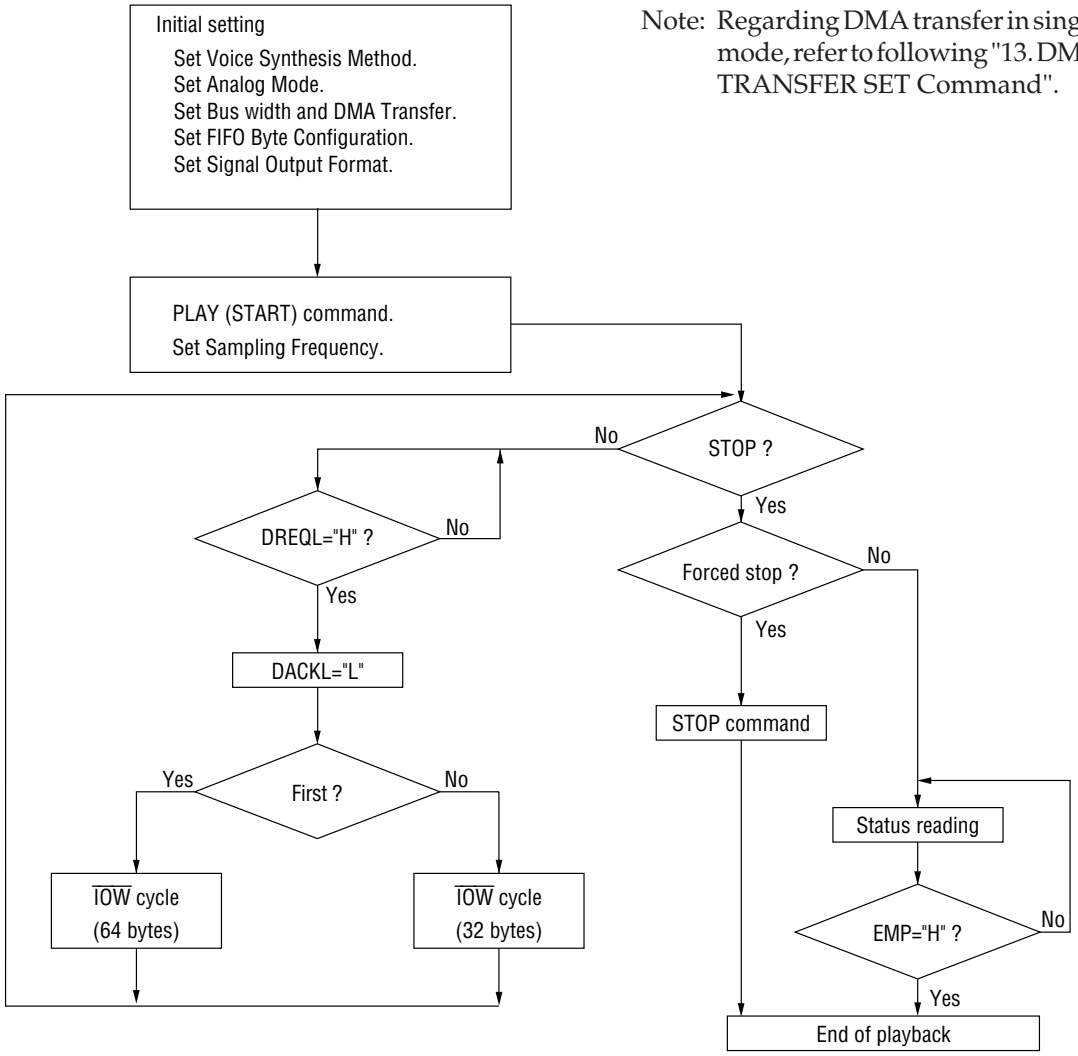


Note: Regarding DMA transfer in Block mode, refer to following "13. DMA TRANSFER SET Command".

Note 1 : The above flowchart assumes that FIFO memory is 64 bytes long. The MSM9841 writes data 64 bytes as a block in the first write-operation and writes a 32-byte block in the second and later write operations. A time period between the input of a DREQ request and the end of block writing depends upon a sampling frequency and the voice synthesis method. For example, when a 8 kHz sampling frequency and a 8-bit ADPCM2 voice synthesis method are set, a 32-byte block writing must be completed within 2 ms.

Note 2 : The MSM9841 supports two kinds of Playback Stop sequence:Forced stop by a STOP command and stop by status reading. When Playback is forcibly stopped by a STOP command, data in FIFO memory is all cleared. When status reading is made, Playback is stopped after all data left in FIFO memory is processed (EMP="H").

Playback Data Transfer Flowchart (with DMA transfer in Single mode)



Note: Regarding DMA transfer in single mode, refer to following "13. DMA TRANSFER SET Command".

Recording time and memory capacity

The recording time of the MSM9841 is dependent on the storage capacitance of external memory, the sampling frequency, and the width of ADPCM bits that have been specified. The recording time of the MSM9841 is expressed by

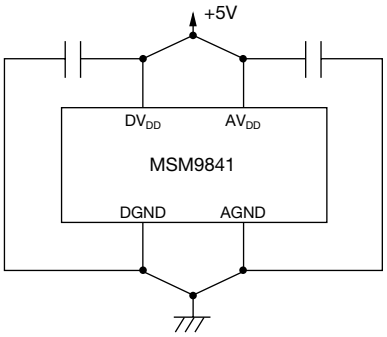
$$\text{Recording time} = \frac{1.024 \times \text{Memory size (in K bits)}}{\text{Sampling frequency (kHz)} \times \text{Width of ADPCM bits}} \text{ (seconds)}$$

For example, when 8.0 kHz of sampling frequency, 4 bit of ADPCM 2, and 8 M bit of memory size are set, the recording time is calculated as follows:

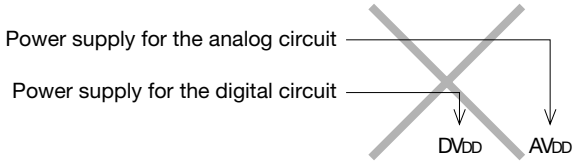
$$\text{Recording time} = \frac{1.024 \times 8000}{8.0 \times 4} = 256 \text{ (second)} = 4 \text{ minutes } 16 \text{ seconds}$$

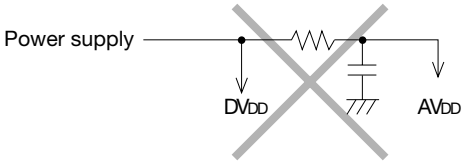
Connection of power supply

The MSM9841 contains a single power supply as shown below.
The power supply is connected to the analog unit and digital unit separately.



Avoid following power supply connections:

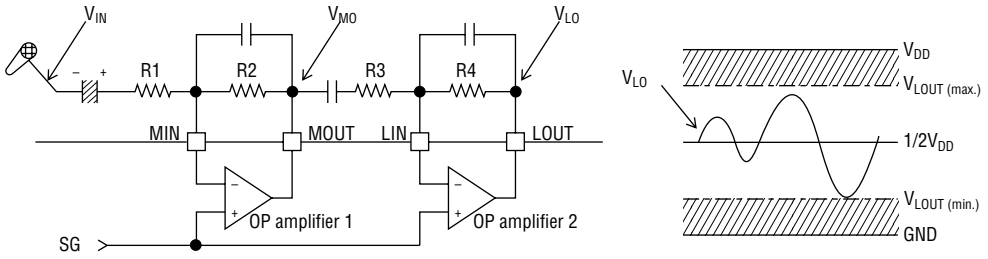




Analog Input Amplifier Circuit

The MSM9841 contains two OP amplifiers to amplify a voice signal from a microphone. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is input internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \bullet R4}{R1 \bullet R3} V_{IN} \text{ (V)}$$

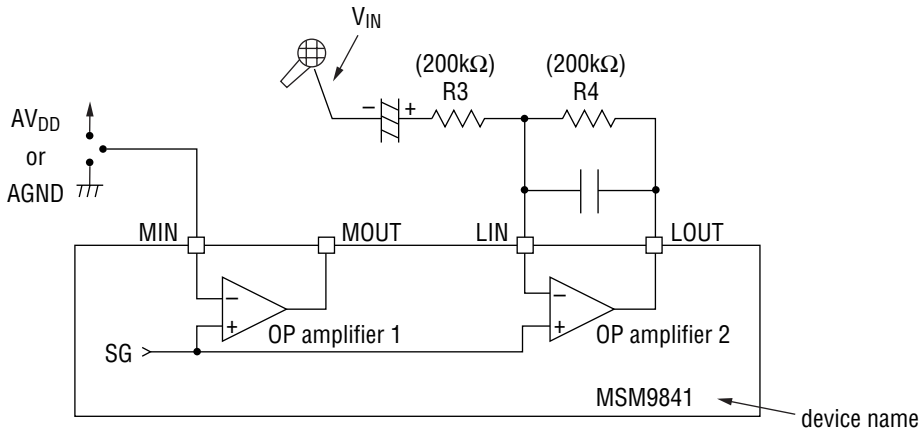
During recording, the output V_{LO} of the OP amplifier 2 is fed to LPF. Adjust the amplification ratio by an external resistor so that the output voltage V_{LOUT} may be in the LOUT-permissible input voltage range.

If V_{LOUT} is not in this range, the waveform of the LPF output may be deformed.

The table below shows an examples of LOUT- permissible input voltage ranges of the MSM9841.

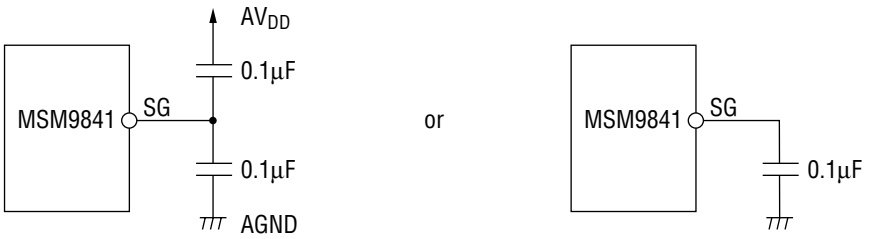
Model name	Supply Voltage V_{DD}	LOUT-permissible voltage range V_{LOUT}		LOUT-permissible voltage
		min	max	
MSM9841	5 V	1 V	4 V	$3V_{p-p}$
	3 V	0.75 V	2.25 V	$1.5V_{p-p}$

The load resistance R_{OUTA} of the OP amplifier is 200 kΩ (minimum). Therefore, the feedback resistors R2 and R4 of the inversion type amplifying circuit must be 200 kΩ or higher.
If you use only OP amplifier 2, connect MIN pin to AGND, and leave MOUT pin open as bellows.
If you don't need to amplify, you must use OP amplifier 2. The bellows figure shows the circuit example of one times the amplification ratio with setting R3 and R4 to 200 kΩ.

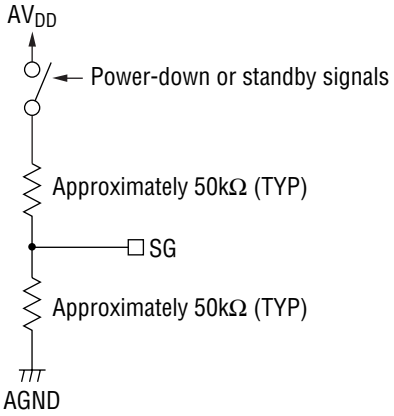


The process of SG pin

SG signal indicades the reference voltage SG (Signal Ground) for internal OP amplifiers and input LPF. To avoid the noise on this signal, insert capacitors to SG pin as bellows. We recommend capacitance of 0.1 µF, and to fix the value of capacitor after sound quality evaluation.



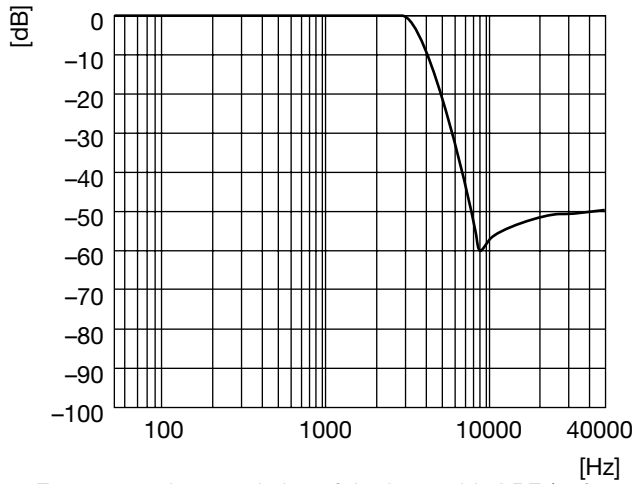
The figure shows the internal equivalence circuit of SG pin.



After canceled the Power Down states or Standby states, it takes about scores millisecond until DC level for SG pin and Analog circuit stabilize.
It takes longer in proportion to the value of capacitance.
Start to read or write operation after DC level stabilized.

Frequency characteristics of the input side LPF

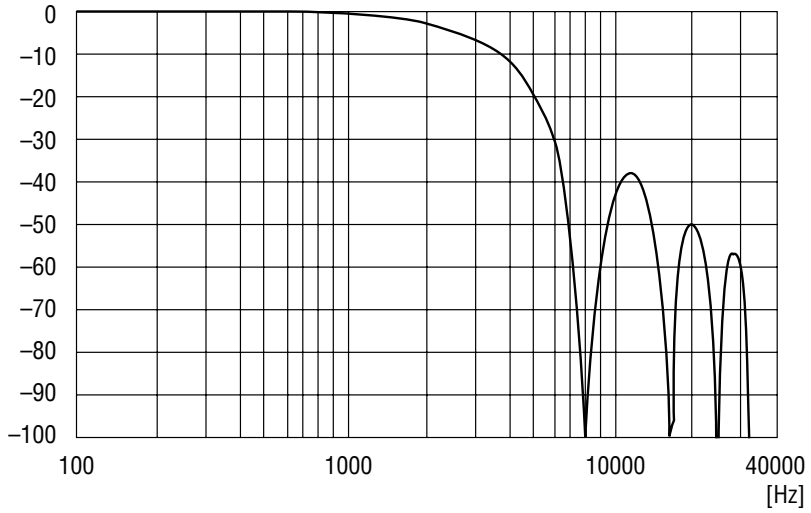
The MSM9841 contains a 4-order low path filter (LPF) produced in the switch capacitor filter technology in the input of a analog signal during recording. The attenuation characteristic is –40 dB/oct. The cut-off frequency and frequency characteristic vary in proportion to the sampling frequency (fs). The cut-off frequency is always 0.4 times the sampling frequency. Below is shown the frequency characteristics of the input side LPF (at fs = 8 kHz).



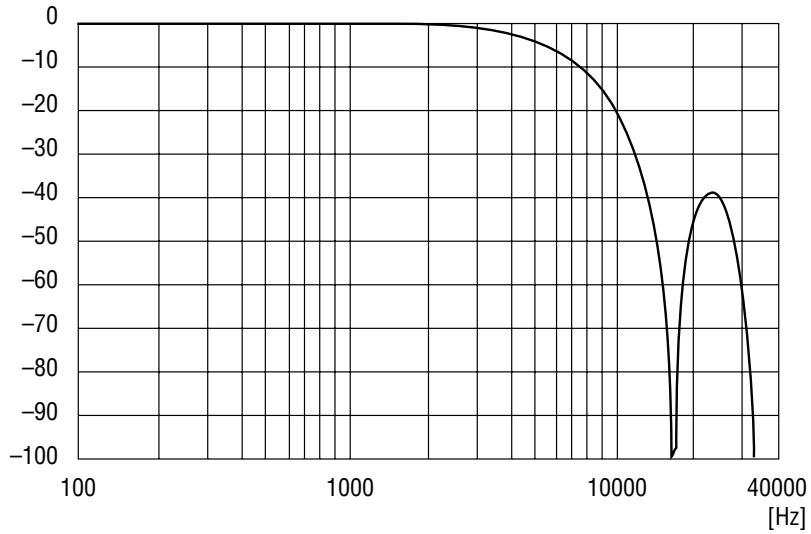
Frequency characteristics of the input side LPF (at fs = 8 kHz)

Frequency characteristics of the output side LPF

The MSM9841 contains two low path filters (LPF) produced in the digital filter technology in the output of the DA converter during playback. Below are shown the frequency characteristics of the output side LPF (at fs = 8 kHz and 16 kHz).



Frequency characteristics of the output side LPF (at fs = 8 kHz)

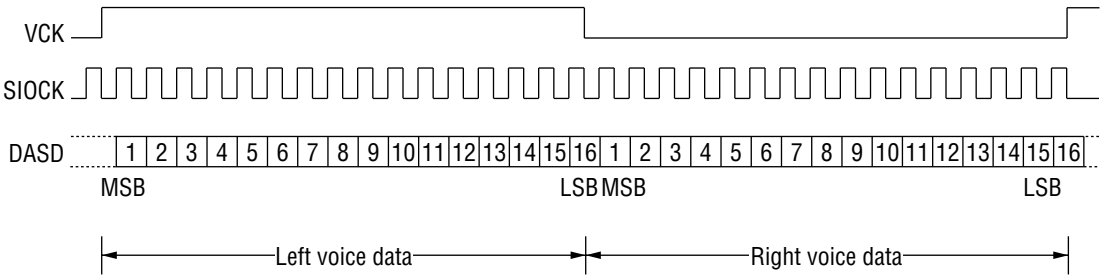


Frequency characteristics of the output side LPF (at fs = 16 kHz)

Using an External DAC

Select the External DAC mode and, 2's Complementary or Binary by commands. The MSM9841 interfaces to the external DAC through the DASD, SIOCK, and VCK pins. In monaural playback, the MSM9841 outputs data when the VCK pin is at a high level ("H"). In stereo playback, the MSM9841 outputs left data when the VCK pin is at a high level ("H") and right data when the VCK pin is at a low level ("L"). Figure 6 shows stereo playback timing of the external DAC at a sampling frequency of 32 kHz (maximum).

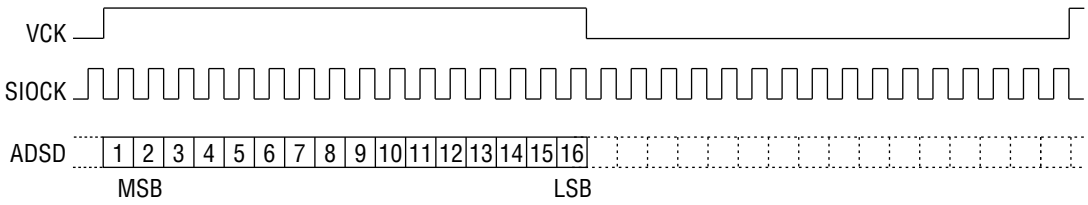
Data is valid in back justification. Left voice data is valid if it is entered before the VCK signal falls. Right voice data is valid if it is entered before the VCK signal rises.



Stereo playback timing of the external DAC at VCK=32 kHz

Using External ADC

Select the External ADC mode and, 2's Complementary or Binary by commands. The MSM9841 interfaces to the external ADC through the ADSD, SIOCK, and VCK pins. Figure 7 shows playback timing of the external ADC at a sampling frequncy of 32 kHz (maximum). Data is valid in back justification. Data is valid if it is entered before the VCK signal falls.



Recording timing of the external ADC at VCK=32 kHz

COMMAND LIST

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	0	0	0	0	NOP (No Operation)
0	0	0	1	×	S2	S1	S0	RECORDING START
0	0	1	0	C3	S2	S1	S0	PLAY START
0	0	1	1	C3	C2	×	×	STOP
0	1	0	0	C3	C2	C1	×	PAUSE
0	1	0	1	C3	V2	V1	V0	VOLUME SETTING
0	1	1	0	W3	W2	×	×	POWER-DOWN MODE
0	1	1	1	P3	P2	P1	P0	VOICE SYNTHESIS METHOD
1	0	0	0	R3	R2	R1	R0	Analog specification 1
1	0	0	1	A3	A2	E1	E0	Analog specification 2 and bus width
1	0	1	0	×	0	B1	B0	FIFO memory configuration
1	0	1	1	F3	D2	D1	D0	Signal output format
1	1	0	0	G2	G1	G0	×	DMA Transfer

×=don't care

Voice synthesis method

P3	P2	P1	P0	Function	
0	0	0	0	4-bit Oki ADPCM2	*
0	0	0	1	5-bit Oki ADPCM2	
0	0	1	0	6-bit Oki ADPCM2	
0	0	1	1	7-bit Oki ADPCM2	
0	1	0	0	8-bit Oki ADPCM2	
0	1	0	1	4-bit Oki ADPCM	
0	1	1	0	8-bit PCM	
0	1	1	1	8-bit Oki non-linear PCM	
1	0	0	0	16-bit PCM	

Volume Setting

V2	V1	V0		
0	0	0	0dB	*
0	0	1	–3dB	
0	1	0	–6dB	
0	1	1	–9dB	
1	0	0	–12dB	
1	0	1	–15dB	
1	1	0	–18dB	
1	1	1	–21dB	

Sampling frequency

S2	S1	S0	f_{SAM}	
0	0	0	8.0 kHz	*
0	0	1	12.8 kHz	
0	1	0	16.0 kHz	
0	1	1	32.0 kHz	
1	0	0	6.4 kHz	
1	0	1	4.0 kHz	

Voice Output Setting

C3	C2	Function	
0	0	Left voice	*
1	0	Right voice	
×	1	Common to both left and right sides	

Pause Setting

C1	Function
0	Starts pausing
1	Cancels pausing

* : initial status

FIFO memory configuration

B1	B0	Function	
0	0	512 bits	*
0	1	1024 bits	
1	0	256 bits	
1	1	FIFO not used	

Note

Note : Disable in the stereo playback mode

Analog specification 2 and data bus transfer setting

A3	Function	
0	With output amplifier	*
1	Without output amplifier	
A2	**Function**	
0	With LPF	*
1	Without LPF	
E1	**Function**	
0	8-bit bus width	*
1	16-bit bus width	
E0	**Function**	
0	D15 to D8 not used for 8-bit bus	*
1	D15 to D8 used for 8-bit bus	

Analog specification 1

R3	Function	
0	Output in 2's complementary.	*
1	Output in binary.	
R2	**Function**	
0	Use internal DAC.	*
1	Use external DAC.	
R1	**Function**	
0	Use internal ADC.	*
1	Use external ADC.	
R0	**Function**	
0	Monaural playback	*
1	Stereo playback	

Signal output format

F3	Function	
0	EMP, MID, and FUL outputs : Active high	*
1	EMP, MID, and FUL outputs : Active low	
D2	**Function**	
0	DREQL and DREQR outputs : Active high	*
1	DREQL and DREQR outputs : Active low	
D1	**Function**	
0	DACKL and DACKR outputs : Active low	*
1	DACKL and DACKR outputs : Active high	
D0	**Function**	
0	No function	*
1	For tesing. Don't use	

*Default

Power-down

W3	Function	
0	Cancel power-down.	*
1	Start power-down.	
W2	**Function**	
0	Retain LSI internal setting.	*
1	Initialize LSI internal setting	

DMA transfer

G3	G2	G1	Function	
0	×	×	Without DMA transfer	*
1	0	0	Single mode transfer	
1	0	1	Block mode transfer	

* : initial status

Description of commands

1. NOP command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

No function

2. RECORDING command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	×	S2	S1	S0

This command starts recording. Bits D2 to D0 specify a sampling frequency.

S2	S1	S0	Sampling frequency	
0	0	0	8.0 kHz	*
0	0	1	12.8 kHz	
0	1	0	16.0 kHz	
0	1	1	32.0 kHz (Note)	
1	0	0	6.4 kHz	
1	0	1	4.0 kHz	

Note : This command can not be used when internal ADC is selected.

3. PLAYBACK command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	C3	S2	S1	S0

This command starts playback. Bits D2 to D0 specify a sampling frequency. Bit D3 selects left or right voice data to be played back. For stereo playback, left and right sampling frequencies must be the same. For monaural playback, when you specify to play continuously phrases of difference sampling frequency, STOP command needs before the next phrase playback.

C3	Function	
0	Playback of left voice.	*
1	Playback of right voice.	

* : initial status

4. STOP command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	C3	C2	×	×

In the recording mode, this command ends recording and the setting of bits D3 and D2 is ignored. After this command is entered, FIFO data is cleared.
In the playback mode, this command aborts playback. When this command is entered, data in FIFO memory is cleared. Bit D3 selects left or right voice whose playback is aborted. Turn on bit D2 to abort playback of both left and right voices at a time.

C3	C2	Function
0	0	Aborts playback of left voice
1	0	Aborts playback of right voice
×	1	Aborts playback of left and reight voices.

5. PAUSE command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	C3	C2	C1	×

This command pauses the current playback or recording operation. Bit D1 enables or disables pausing.
When recording is paused, the setting of bits D3 and D2 is ignored.
When playback is paused, bit D3 selects left or right voice whose playback is paused. Turn on bit D2 to pause playback of both left and right voices.

C1	Function
0	Starts pausing.
1	Cancels pausing.

C3	C2	Function
0	0	Pauses playback of left voice
1	0	Pauses playback of right voice
×	1	Pauses playback of both left and reight voices.

6. VOLUME command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	C3	V2	V1	V0

This command controls the volumes of playback voices.
Bit D3 selects a left or right voice to be volume-controleled during playback. Bits D2 to D0 set a volume.

C3	Function
0	Sets the volume of left voice.
1	Sets the volume of right voice.

V2	V1	V0	Volume	
0	0	0	0 dB	*
0	0	1	–3 dB	
0	1	0	–6 dB	
0	1	1	–9 dB	
1	0	0	–12 dB	
1	0	1	–15 dB	
1	1	0	–18 dB	
1	1	1	–21 dB	

7. POWER-DOWN command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	W3	W2	×	×

When receiving this command, the MSM9841 stops oscillation, minimizes the current consumption, and enters the power-down mode. The AOUTL and AOUTR outputs immediately fall to the GND level. Bit D3 enables or disables the powerdown function and bit D2 enables or disables initialization of the internal circuit of the MSM9841.

W3	Function	
0	Concel the power-down mode	
1	Enter the power-down mode	
	W2	**Function**
	0	Disables initialization of the internal circuit of the LSI.
	1	Enables initialization of the internal circuit of the LSI.

* : initial status

8. VOICE SYNTHESIS METHOD command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	P3	P2	P1	P0

This command selects a voice synthesis method. Bits D3 to D0 select a method. A total of nine voice synthesis methods are selectable. The selected voice synthesis method cannot be changed while playback or recording is in progress.

P3	P2	P1	P0	Voice synthesis method	
0	0	0	0	4-bit ADPCM2	*
0	0	0	1	5-bit ADPCM2	
0	0	1	0	6-bit ADPCM2	
0	0	1	1	7-bit ADPCM2	
0	1	0	0	8-bit ADPCM2	
0	1	0	1	4-bit ADPCM	
0	1	1	0	8-bit straight PCM	
0	1	1	1	8-bit non-linear PCM	
1	0	0	0	16-bit straight PCM	

9. ANALOG SPECIFICATION 1 command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	R3	R2	R1	R0

This command selects the built-in ADC or DAC, the external ADC or DAC, indication of 2's complement or binary, and stereo or monaural playback. When the MSM9841 is turned on, the AOUTL and AOUTR pin voltages immediately rise to 1/2 V_{DD}.

R3	Function	
0	2's complement complementary	*
1	Binary	

R2	Function	
0	Internal DAC	*
1	External DAC	

R1	Function	
0	Internal ADC	*
1	External ADC	

R0	Function	
0	Monaural playback mode	
1	Stereo playback mode	*

* : initial status

10. ANALOG SPECIFICATION DATA BUS WIDTH SET command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	A3	A2	E1	E0

D3 selects use or disuse of the internal output amplifiers to the AOUTL Pin and the AOUTR Pin. D2 selects use or disuse of the internal LPFs to the AOUTL Pin and the AOUTR Pin. D1 and D0 set a data bus width and select use or disuse of D15 to D8 for voice data transfer when the 8-bit bus is selected. D1 and D0 select "D15 to D8 not used for 8-bit bus width" when D7 to D0 pins are used to transfer (input or output) all data including commands, status, and data. D1 and D0 select "D15 to D8 used for 8-bit bus width" when D15 to D8 pins are used to input or output data and D7 to D0 pins are used to input or output commands and statuses.

A3	Function	
0	With output amplifier	*
1	Without output amplifier	

A2	Function	
0	With LPF	*
1	Without LPF	

E1	E0	Function	
0	0	D15 to D8 not used for 8-bit bus width	*
0	1	D15 to D8 used for 8-bit bus width	
1	×	16-bit bus width	

* : initial status

11. FIFO MEMORY SPECIFICATION command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	×	0	B1	B0

This command selects a bit configuration (word configuration) of the FIFO memory. When stereo playback is selected, this command selects a left side or right side bit configuration (word configuration). Therefore, the 1024-bit configuration can not be selected because the MSM9841 contains 1024 bits of FIFO memory.

	B1	B0	8-bit bus configuration	16-bit bus configuration
*	0	0	512 bits (64 words)	512 bits (32 words)
Note	0	1	1024 bits (128 words)	1024 bits (64 words)
	1	0	256 bits (32 words)	256 bits (16 words)
	1	1	FIFO memory not used	

Note: For stereo playback, the word configuration cannot be selected.

* : initial status

12. SIGNAL OUTPUT FORMAT CONTROL command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	F3	D2	D1	D0

This command sets the output formats of the EMP, MID, FUL, DREQL, and DREQR pins and the input formats of the DACKL and DACKR pins.

F3	Function	
0	EMP, MID, FUL outputs : Active high	*
1	EMP, MID, FUL outputs : Active low	

D2	Function	
0	DREQL and DREQR outputs : Active high	*
1	DREQL and DREQR outputs : Active low	

D1	Function	
0	DACKL and DACKR inputs : Active low	*
1	DACKL and DACKR inputs : Active high	

D0	Function
0	No function
1	For test. Not used

13. DMA TRANSFER SET Command

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	G3	G2	G1	×

This command sets use or disuse of DMA transfer or selects DMA transfer mode. When the Single mode DMA transfer is selected, if the DREQL pin or stereo playback is selected, the DREQL pin is active while DMA transfer is being requested. The Single mode DMA transfer is selected when transfering data monitoring the status of the DREQL or DREQR pin without controlling the number of bytes to be transfered. When the Block mode DMA transfer is selected, if the DREQL pin or stereo playback is selected, the DREQR sends a DMA request signal and becomes inactive when the DACKL pin or DACKR pin is active. The Block mode DMA transfer is selected when the number of bytes to be transfered can be controlled and the DREQL or DREQR pin is set to be inactive.

G3	G2	G1	Function	
0	×	×	Without transfer	*
1	0	0	Single mode DMA transfer	
1	0	1	Block mode DMA transfer	

* : initial status

Description of Status

The MSM9841 supports the following seven status flags :

D7	Left Data Recording/Playing flag	High when recording or playback is in progress
D6	Right Data Playing flag	High when playback is in progress
D5	Left Pause flag	High when playback of left voice is paused
D4	Right Pause flag	High when playback of right voice is paused
D3	EMP Information Output flag	Output the same signal as the EMP pin.
D2	MID Information Output flag	Output the same signal as the MID pin.
D1	FUL Information Output flag	Output the same signal as the FUL pin.
D0	Data Transfer Error flag	See the explanation below.

Note: EMP, MID, and FUL output the High Active signals. These bits don't be feedback to the output format by command.

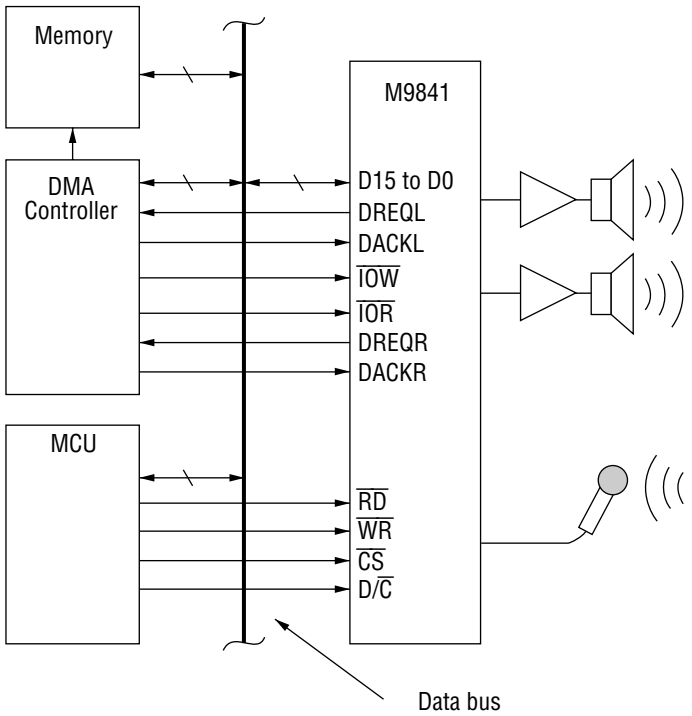
The MSM9841 supports the following three data transfer errors :

When FIFO memory is used

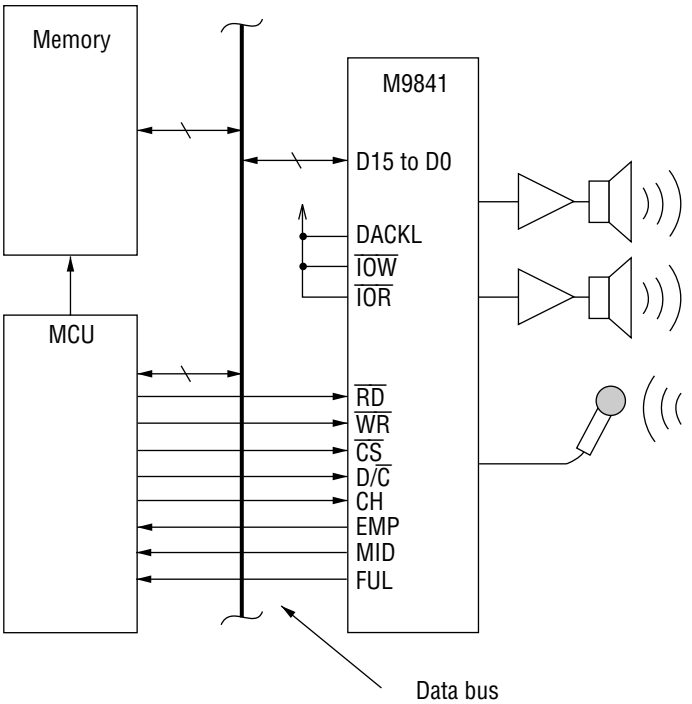
(1) "H" when a read operation is mode while EMP is "H"
(2) "H" when a read operation is mode while MID is "L"
(3) "H" when a write operation is mode while FUL is "H"

CPU INTERFACE EXAMPLES

1) Interface when DMA controller is used (16-bit bus)



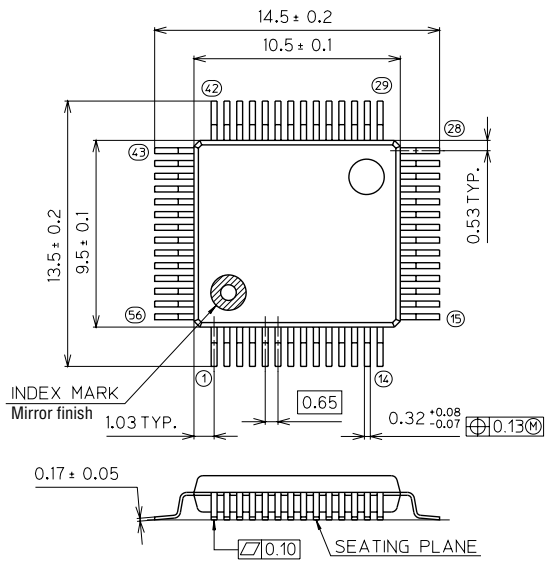
2) MCU & external memory interface (16-bit bus)

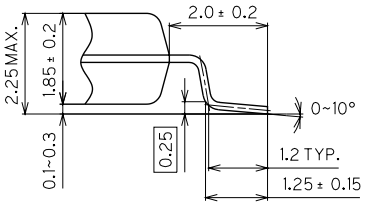


PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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