Quad E1 Framer

FEATURES

- Monolithic single-chip device which integrates four full-featured E1 framers and transmitters for terminating duplex E1 signals.
- Frames to a G.704 2.048 Mbit/s signal. Frames to the signalling multiframe and to the CRC multiframe when enabled.
- Supports HDB3 or AMI line codes.
- Supports transfer of PCM and signalling data to/from 2.048 Mbit/s or 16.384 Mbit/s backplane buses. Supports *n* × DS0 backplane interface for fractional E1.
- Provides Channel-Associated Signalling (CAS) extraction/insertion, programmable idle and digital milliwatt code substitution, and up to three multiframes of signalling debounce on a per-channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all/selected channels.
- Provides an HDLC interface for terminating/generating a datalink.
- Optionally extracts the datalink from timeslot 16 or from any combination of the national bits.
- Software and functionally compatible with the PM6341 E1XC Single E1 Transceiver. Pin-compatible with the PM4344 TQUAD Quad T1 Framer.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 5 V CMOS technology.
- Available in a rectangular 128-pin PQFP (14 by 20 mm) package.

RECEIVE SECTION

- Recovers clock and data using a digital PLL for high jitter tolerance.
- Accepts/provides dual- or single-rail digital PCM inputs/outputs. Accepts gapped data streams to support higher rate demultiplexing.
- Provides Loss Of Signal (LOS) detection, and indicates loss of frame alignment (OOF), loss of signalling multiframe, and loss of CRC multiframe. Indicates reception of remote alarm, remote multiframe alarm, Alarm Indication Signal (AIS) and timeslot 16 AIS.
- Supports Line and Path performance monitoring according to ITU recommendations. Accumulators are provided for counting CRC-4 errors, Far-End Block Errors (FEBEs), frame sync errors, and Line Code Violations (LCVs).
- Extracts the datalink. Extracts selected channels.
- Provides a 2-frame elastic store buffer for jitter and wander attenuation.

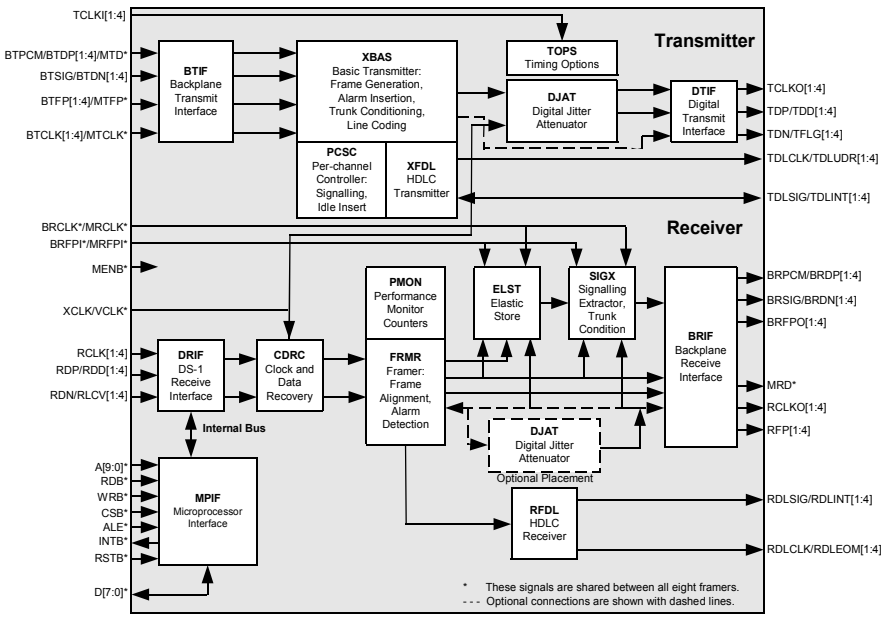
TRANSMIT SECTION

- Optionally accepts/provides dual-rail digital PCM inputs/outputs.
- Formats data to create a G.704 2.048 Mbit/s signal. Optionally inserts signalling multiframe alignment signal. Optionally inserts CRC multiframe structure including optional transmission of FEBEs.
- Allows insertion of a datalink. Allows insertion of selected channels through a serial port.
- Supports transmission of the AIS, timeslot 16 AIS, remote alarm, and remote multiframe alarm.
- Provides a digital PLL for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and transmit rate conversion. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.

APPLICATIONS

- E1/E3 Multiplexers and Digital Private Branch Exchanges (PBXs)
- E1 Frame Relay Interfaces
- E1 ATM Interfaces
- Fractional E1 Interfaces
- Digital Access and Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSXs)
- Digital Loop Carriers (DLCs)
- E1 Channel Service Units (CSUs) and Data Service Units (DSUs)
- ISDN Primary Rate Interfaces (PRI)
- SDH Add/Drop Multiplexers (ADMs)

BLOCK DIAGRAM



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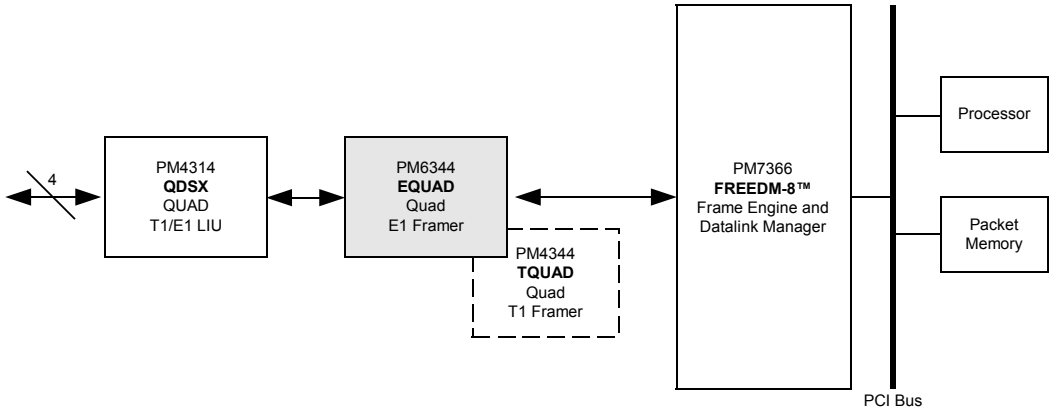
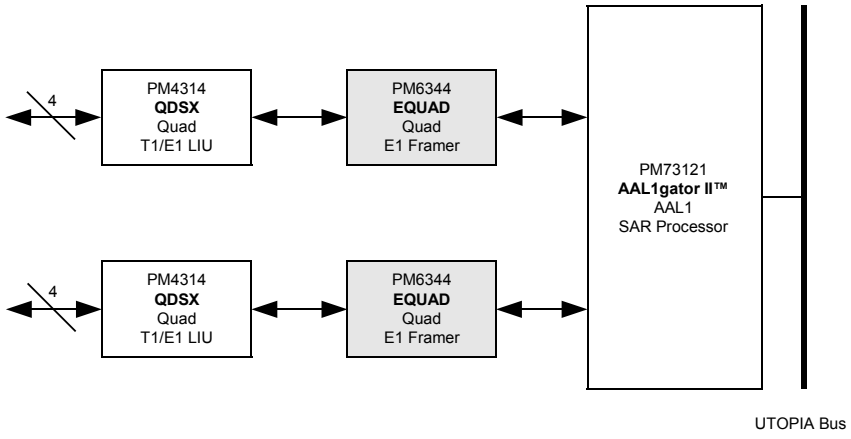
TYPICAL APPLICATIONS

FULLY CHANNELIZED HDLC APPLICATION



STRUCTURED / UNSTRUCTURED E1 AAL1 OCTAL PORT CARD



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