MOTOROLA

SN54/74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to V_{CC} noise is also provided by internal latching circuitry.

Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With R_{ext} = 2.0 kΩ and C_{ext} = 0, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

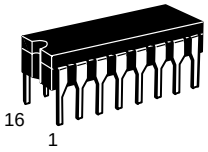
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10 pF to 10 μF), and greater than one decade of timing resistance (2.0 to 70 kΩ for the SN54LS221, and 2.0 to 100 kΩ for the SN74LS221). Pulse width is defined by the relationship: $t_W(out) = C_{ext}R_{ext} \ln 2.0 \approx 0.7\, C_{ext}\, R_{ext}$; where t_W is in ns if C_{ext} is in pF and R_{ext} is in kΩ. If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 kΩ may be used. The range of jitter-free pulse widths is extended if V_{CC} is 5.0 V and 25°C temperature.

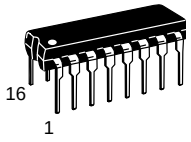
- SN54LS221 and SN74LS221 is a Dual Highly Stable One-Shot
- Overriding Clear Terminates Output Pulse
- Pin Out is Identical to SN54/74LS123

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

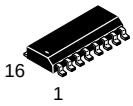
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

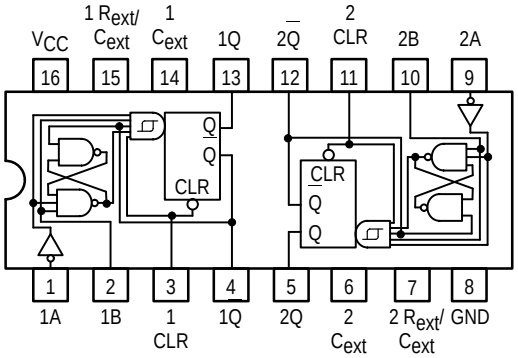


D SUFFIX
SOIC
CASE 751B-03

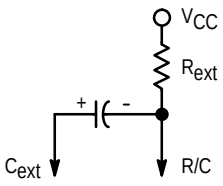
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

(TOP VIEW)



positive logic: Low input to clear resets Q low and Q high regardless of dc levels at A or B inputs.



FUNCTION TABLE (EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
*↑	L	H	⊓	⊔

*See operational notes — Pulse Trigger Modes

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

OPERATIONAL NOTES

Once in the pulse trigger mode, the output pulse width is determined by $t_W = R_{ext}C_{ext}\ln 2$, as long as R_{ext} and C_{ext} are within their minimum and maximum valves and the duty cycle is less than 50%. This pulse width is essentially independent of V_{CC} and temperature variations. Output pulse widths varies typically no more than ±0.5% from device to device.

If the duty cycle, defined as being $100 \bullet \frac{t_W}{T}$ where T is the period of the input pulse, rises above 50%, the output pulse width will become shorter. If the duty cycle varies between low and high valves, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum, R_{ext} should be as large as possible. (Jitter is independent of C_{ext}). With R_{ext} = 100K, jitter is not appreciable until the duty cycle approaches 90%.

Although the LS221 is pin-for-pin compatible with the LS123, it should be remembered that they are not functionally identical. The LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the LS221. Also note that it is recommended to externally ground the LS123 C_{ext} pin. However, this cannot be done on the LS221.

The SN54LS/74LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width, t_W can be varied over 9 decades of timing by proper selection of the external timing components, R_{ext} and C_{ext}.

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers (≥1.0 μV/s). High immunity to V_{CC} noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard V_{CC} bypassing is strongly recommended.

The LS221 has four basic modes of operation.

Clear Mode: If the clear input is held low, irregardless of the previous output state and other input states, the Q output is low.

Inhibit Mode: If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other inputs.

Pulse Trigger Mode: A transition of the A or B inputs as indicated in the functional truth table will trigger the Q output to go high for a duration determined by the t_W equation described above; Q will go low for a corresponding length of time.

The Clear input may also be used to trigger an output pulse, but special logic preconditioning on the A or B inputs must be done as follows:

Following any output triggering action using the A or B inputs, the A input must be set high OR the B input must be set low to allow Clear to be used as a trigger. Inputs should then be set up per the truth table (without triggering the output) to allow Clear to be used a trigger for the output pulse.

If the Clear pin is routinely being used to trigger the output pulse, the A or B inputs must be toggled as described above before and between each Clear trigger event.

Once triggered, as long as the output remains high, all input transitions (except overriding Clear) are ignored.

Overriding Clear Mode: If the Q output is high, it may be forced low by bringing the clear input low.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{T+}	Positive-Going Threshold Voltage at C Input			1.0	2.0	V	V_{CC} = MIN	
V_{T-}	Negative-Going Threshold Voltage at C Input	54	0.7	0.8		V	V_{CC} = MIN	
		74	0.7	0.8		V		
V_{T+}	Positive-Going Threshold Voltage at B Input			1.0	2.0	V	V_{CC} = MIN	
V_{T-}	Negative-Going Threshold Voltage at B Input	54	0.7	0.9		V	V_{CC} = MIN	
		74	0.8	0.9		V		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for A Input	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for A Input	
		74			0.8			
V_{IK}	Input Clamp Voltage				–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.4		V		
V_{OL}	Output LOW Voltage	54		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Input A Input B Clear				–0.4 –0.8 –0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Quiescent			4.7	11	mA	V_{CC} = MAX	
	Triggered			19	27			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

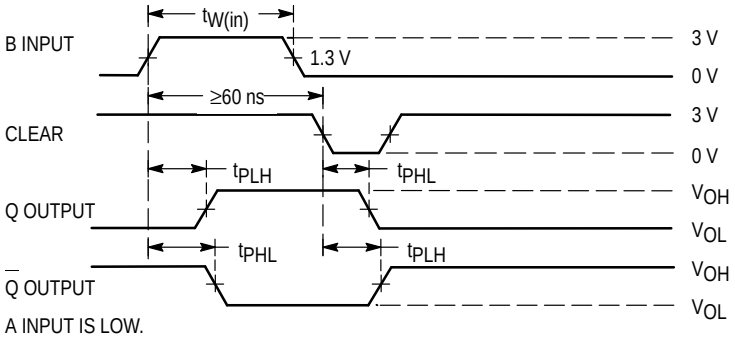
AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	From (Input)	To (Output)	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
t_{PLH}	A	Q		45	70	ns	C_L = 15 pF, See Figure 1	C_{ext} = 80 pF, R_{ext} = 2.0 Ω
	B	Q		35	55			
t_{PHL}	A	$\overline{Q}$		50	80	ns		
	B	$\overline{Q}$		40	65			
t_{PHL}	Clear	Q		35	55	ns		
t_{PLH}	Clear	$\overline{Q}$		44	65	ns		
$t_{W(out)}$	A or B	Q or $\overline{Q}$	70	120	150	ns		C_{ext} = 80 pF, R_{ext} = 2.0 Ω
			20	47	70			C_{ext} = 0, R_{ext} = 2.0 kΩ
			600	670	750			C_{ext} = 100 pF, R_{ext} = 10 kΩ
			6.0	6.9	7.5	ms		C_{ext} = 1.0 μF, R_{ext} = 10 kΩ

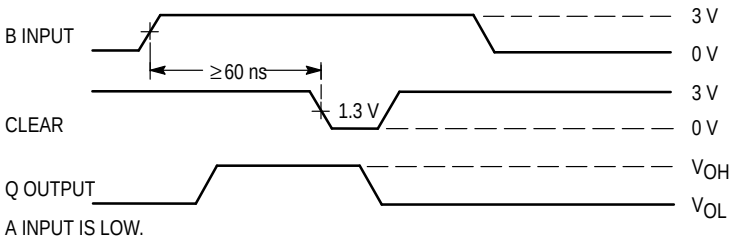
AC SETUP REQUIREMENTS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
dv/dt	Rate of Rise or Fall of Input Pulse	Schmitt, B	1.0			V/s
		Logic Input, A	1.0			V/μs
t_W	Input Pulse Width	A or B, $t_{W(in)}$	40			ns
		Clear, t_W (clear)	40			
t_s	Clear-Inactive-State Setup Time		15			ns
R_{ext}	External Timing Resistance	54	1.4		70	kΩ
		74	1.4		100	
C_{ext}	External Timing Capacitance		0		1000	μF
	Output Duty Cycle	RT = 2.0 kΩ			50	%
		R_T = MAX R_{ext}			90	

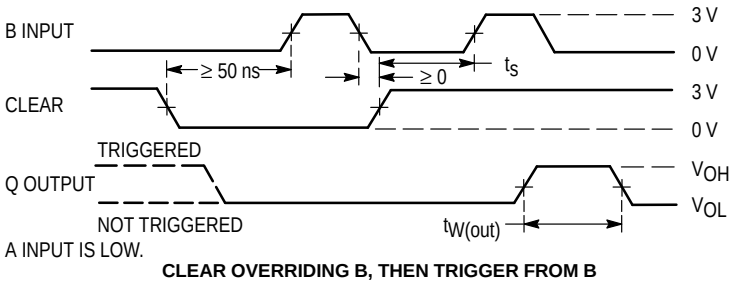
AC WAVEFORMS



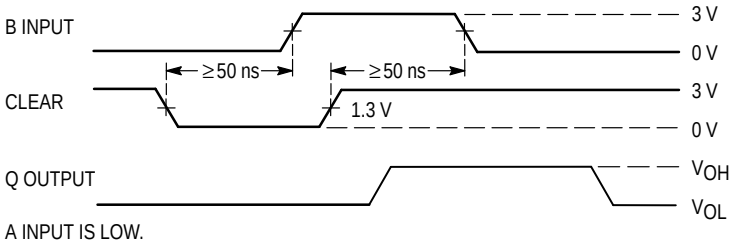
TRIGGER FROM B, THEN CLEAR — CONDITION 1



TRIGGER FROM B, THEN CLEAR — CONDITION 2



CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

Figure 1