TOSHIBA Bi-CMOS INTEGRATED CIRCUIT   SILICON MONOLITHIC
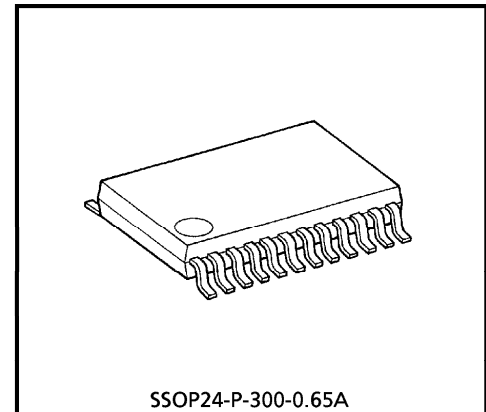
T B 2 1 1 0 F N

PLL FOR DTS

The TB2110FN is a high-speed PLL LSI built in a 2 modulus prescaler that can operate with a 1.5 V power supply.
Each function is controlled via three serial bus lines, allowing you to configure a high-performance digital tuning system.

FEATURES

- Due to a Bi-CMOS structure, the 1.5 V power supply is stepped up and stabilized by a bipolar circuit to drive the CMOS section. Therefore, this chip is best suited for digital tuning system in headphone stereos.

- Built in a prescaler, This IC can operate with TV : 50~250 MHz and FM : 40~150 MHz (2 modulus type) for the FM_{IN} input or at 0.5~40 MHz for the AM_{IN} input (2 modulus type or directly divided).

- Comes with a 20 bit programmable counter, two parallel output phase comparators, crystal oscillator, reference counter, and a DC/DC converter control circuit.

- The crystal oscillator (X'tal) used in this IC is a 75 kHz resonator.

- The reference frequency can be selected from seven frequencies available. (Ref = 1.0~25 kHz)

- A 20 bit general-purpose counter is built in that can measure the IF and other frequencies.

- All device operations are controlled via three serial bus lines.

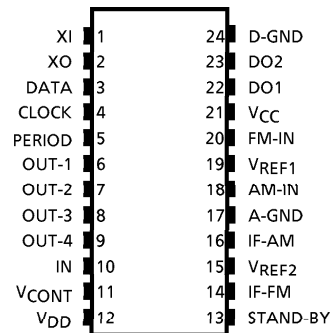- Operating voltage range : V_{CC} = 1.0~2.5 V (Ta = −20~75°C)

- Package is SSOP24pin.

SSOP24-P-300-0.65A

Weight : 0.31 g (Typ.)

PIN CONNECTION

XI	1	24	D-GND
XO	2	23	DO2
DATA	3	22	DO1
CLOCK	4	21	V_{CC}
PERIOD	5	20	FM-IN
OUT-1	6	19	V_{REF1}
OUT-2	7	18	AM-IN
OUT-3	8	17	A-GND
OUT-4	9	16	IF-AM
IN	10	15	V_{REF2}
V_{CONT}	11	14	IF-FM
V_{DD}	12	13	STAND-BY

(Note) This device is vulnerable to surge voltages. Take it into account when using this device in your system.

BLOCK DIAGRAM
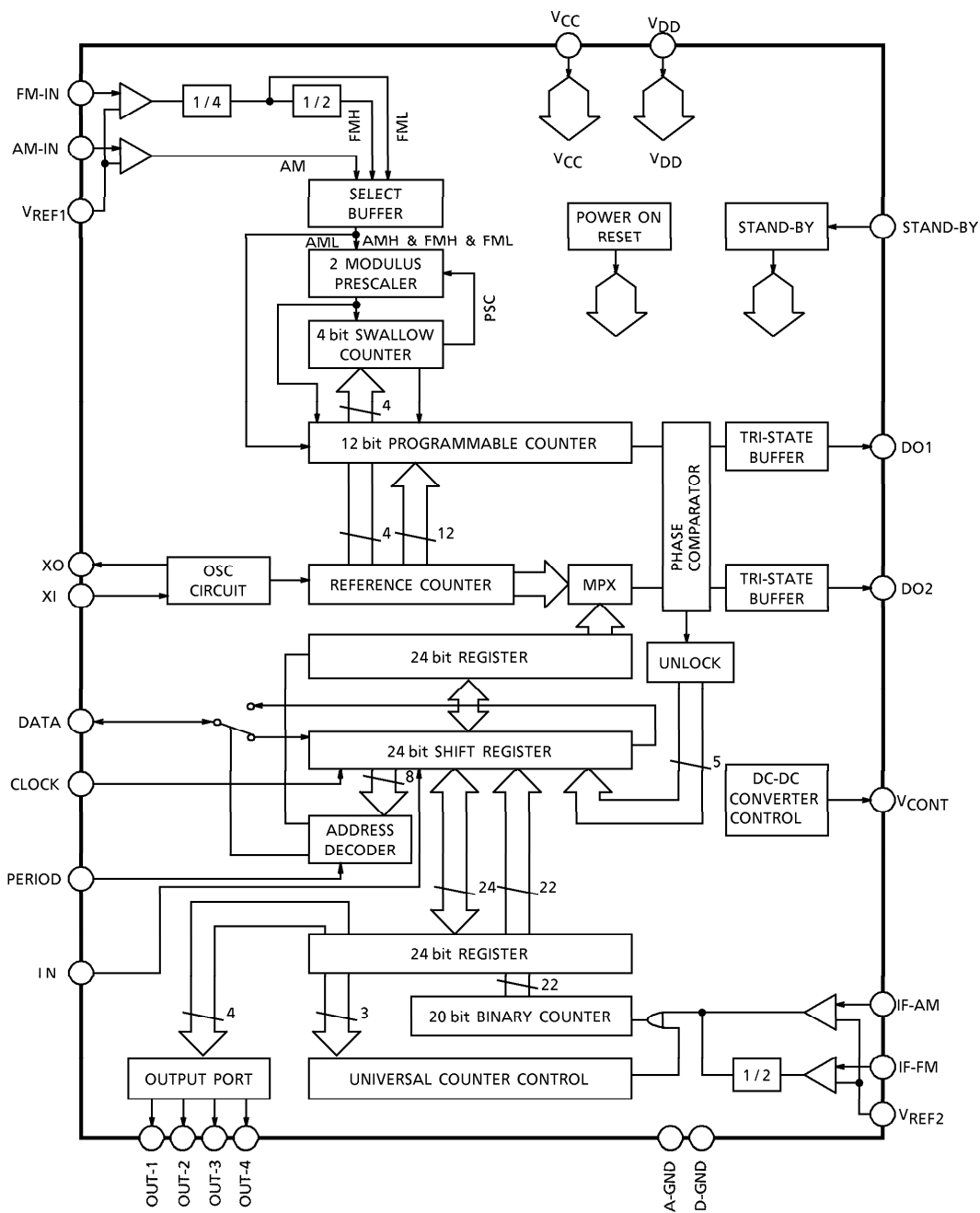
PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION	REMARKS
1 2	XI XO	Crystal oscillator pins	Connect a 75 kHz crystal oscillator for the reference frequency to these pins.	
3	DATA	Serial data input / output	Serial I/O port. Use this pin to set the divide ratio and divide method, as well as transfer data to and from the controller to control the general-purpose counter and general-purpose I/O port.	
4	CLOCK	Clock signal input		
5	PERIOD	Period signal input		
6 7 8 9	OUT-1 OUT-2 OUT-3 OUT-4	General-purpose output port	This is an open-collector output port. Use this port to output control signals.	
10	IN PORT	General-purpose input port	This port accepts the data to be fed to the output bit (OUT-5).	
11	V_{CONT}	DC / DC converter control pin	This pin controls the DC/DC converter.	
12	V_{DD}	CMOS section power supply	The V_{DD} power supply from the DC/DC converter is applied to this pin.	—
13	STAND-BY	Standby	The device is placed in standby mode when a "L" is input. The device is in active state when a "H" is input.	
14	IF-FM	General-purpose counter input	Use this pin for IF signal input on the FM side.	
15	V_{REF2}	Reference pin	Use this pin as the reference of the IF signal.	
16	IF-AM	General-purpose counter input	Use this pin for IF signal input on the AM side.	
17	A-GND	Bipolar section GND	—	—

PIN No.	SYMBOL	PIN NAME	FUNCTION	REMARKS
18	AM-IN	AM / SW signal input pin	Use this pin for AM / SW signal input.	FM-IN (Pin 20) AM-IN (Pin 18) Vref1 (Pin 19)
19	V_{REF1}	Reference pin	Use this pin as the reference of the AM / FM signal.	
20	FM-IN	FM / TV signal input pin	Use this pin for FM / TV signal input.	
21	V_{CC}	Bipolar section power supply	—	—
22 23	DO1 DO2	Phase comparator output	This is a tri-state output of the phase comparator. DO1~DO2 are parallel outputs.	V_{DD}
24	D-GND	MOS section GND	—	—

OPERATION

◯ Serial I / O port

The TB2110FN has two pairs of 24 bit registers, so it can set data to a total of 48 bits to control each function. Each data in these registers are transferred to and from the controller through a serial port using three pins : DATA, CLOCK, and PERIOD. A total of 32 bits consisting of 8 bit address and 24 data bits can be handled in one serial transfer.

Because all operations are controlled via register, this section describes mainly the function of 8 bit address and each register. The registers are configured in units of 24 bits, and are selected by an 8 bit address. The address mapping of each register is listed in the next page as "Register allocation."

REGISTER	ADDRESS	CONTENTS OF 24 BITS	No. OF BITS
Input Register 1	D0H	PLL dividend number setting Reference frequency setting PLL input and mode setting Not used	16 3 2 3 Total 24
Input Register 2	D2H	General-purpose counter control Test bit Output data Not used	7 1 4 12 Total 24
Output Register 1	D1H	General-purpose counter numeric data Not used	22 2 Total 24
Output Register 2	D3H	Data in register D2 Lock detection data Input data Not used	8 2 1 13 Total 24

The input data is latched into register 1 or register 2 at the falling edge of PERIOD to put each function to work.

The output data that comes in parallel is latched into the output register at the 9 th falling edge of CLOCK, and is serially output from the DATA pin.

(Note) Transmit dummy data at least once before transferring regular data to initialize the device's internal circuits after power-on.

REGISTER ALLOCATION
T−BUS format

Input register "D0"

LSB: "0" "0" "0" "0" "1" "1" "0" "1" "1"
T-bus = "0"   T-bus = "D"

bit	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15	R0	R1	R2		FM	MODE	⊠	⊠
(Note 3)	*	*	*	*	0	0	1	1	*	*	*	*	*	*	*	*	1	1	1	1	1	1	1	1

Pre-Set pulse swallow counter from P00 to P15; referece-counter; mode-control

Input register "D2"

LSB: "0" "1" "0" "0" "1" "1" "0" "1" "1"
T-bus = "2"   T-bus = "D"

| bit	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	G0	G1	⊠	⊠	DOHZ	RESETN	STARTN	TS	⊠	⊠	⊠	⊠	M8	M9	⊠	O1	O2	O3	O4					⊠
(Note 3)	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IF-counter-gate; control-signal; IF-counter-mode; output-data from OUT1 to OUT4

Output register "D1"

LSB: "1" "0" "0" "0" "1" "1" "1" "1"
T-bus = "1"   T-bus = "D"

bit	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	f00	f01	f02	f03	f04	f05	f06	f07	f08	f09	f10	f11	f12	f13	f14	f15	f16	f17	f18	f19	OVER	BUSY	OUT-5	■
(Note 3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IF-counter-out from f00 to f19, OVER, BUSY; OUT5

Output register "D3"

LSB: "1" "1" "0" "0" "1" "1" "1" "1"
T-bus = "3"   T-bus = "D"

bit	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	G0	G1	■	■	■	■	■	■	ENABLE	UNLOCK	■	■	M8	M9	■	O1	O2	O3	O4	OUT-5	OUT5	■	■
(Note 3)	0	0	0	0	0	0	0	0	*	*	0	0	0	0	0	0	0	0	0	*	*	0	0	0

IF-counter-gate; Phase-comp.; IF-counter-mode; output-data from OUT1 to OUT4; OUT5

(Note 1) ■ : GND output

(Note 2) ⊠ : Don't care

(Note 3) * : value is undecided when power on

◯ Serial transfer format
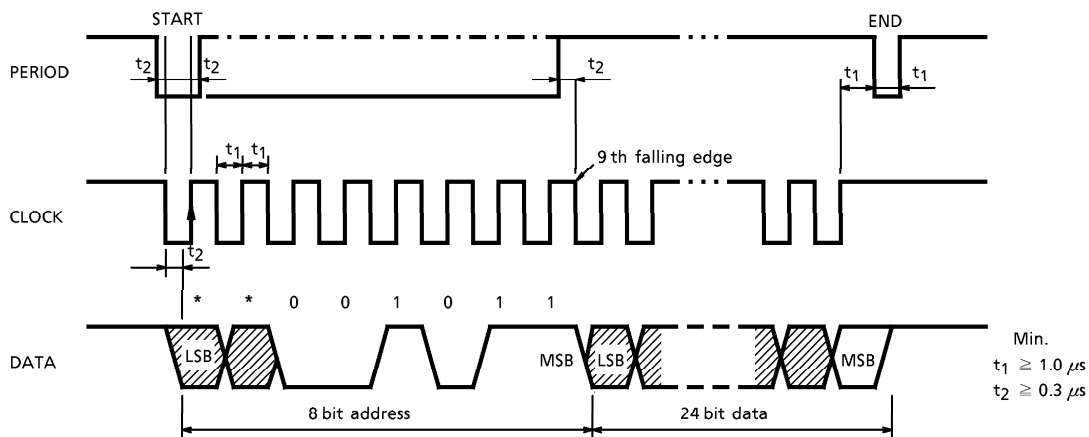
● The serial transfer format consists of 8 bit address and 24 bit data as shown above.
The addresses used here are D0H to D3H.

◯ Crystal oscillator connecting pins (XI, XO)

Connect a crystal oscillator and capacitors to these pins as shown in Figure 1 to generate the clock required for the device's internal operation. Use a 75 kHz crystal oscillator here.

C = 18 pF Typ.
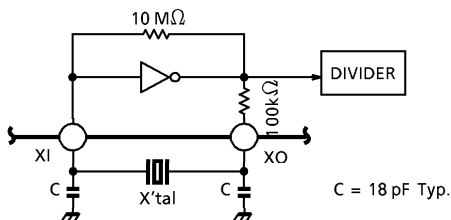
(Note) Choose a crystal oscillator that has a small CI value and good startup characteristics.

Figure 1

○ Programmable counter

The programmable counter section consists of 1 / 4 + 1 / 2 prescalers, 2 modulus prescaler, and 4bit + 12bit programmable binary counters.

1. Setting the programmable counter section

The programmable counter need to be set for the divisor (16 bits) and the dividing mode (2 bits).

(1) Setting the dividing mode

Use the FM and MODE bit to choose the input setting and the dividing mode (pulse swallow mode or direct dividing mode). Four mode are available as listed below. Choose the desired one according to the frequency bands used.
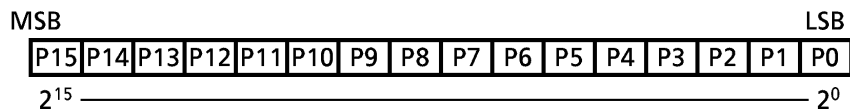
MODE	FM	MODE	DIVIDING MODE	TYPICAL RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT PIN	DIVISOR
AM	0	0	Direct dividing mode	LW, MW	0.5~10 MHz	AMIN	n
SW	0	1	Pulse swallow mode	SW	3~40 MHz		n
FM	1	0	1 / 4 + pulse swallow mode	FM	40~150 MHz	FMIN	4·n
TV	1	1	1 / 8 + pulse swallow mode	TV	50~250 MHz		8·n

(Note) 'n' denotes the set value.

(2) Setting the divisor

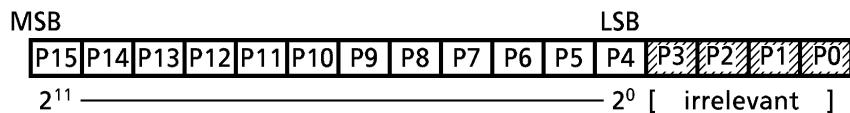To determine the programmable counter's divisor, set binary data to the P0~P15 bits.

● For the pulse swallow mode (16 bits, SW, FM, and TV BAND)

MSB   LSB

| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

2^{15} ————————————————————————————— 2^{0}

Range of divisor set (pulse swallow mode) n = 210 H~FFFFH (528~65535)

(Note) The actual divisor is 4 times the programmed number for the 1 / 4 + pulse swallow mode, and 8 times the programmed number for the 1 / 8 + pulse swallow mode.

● Direct divide method (12 bits)

MSB   LSB

| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

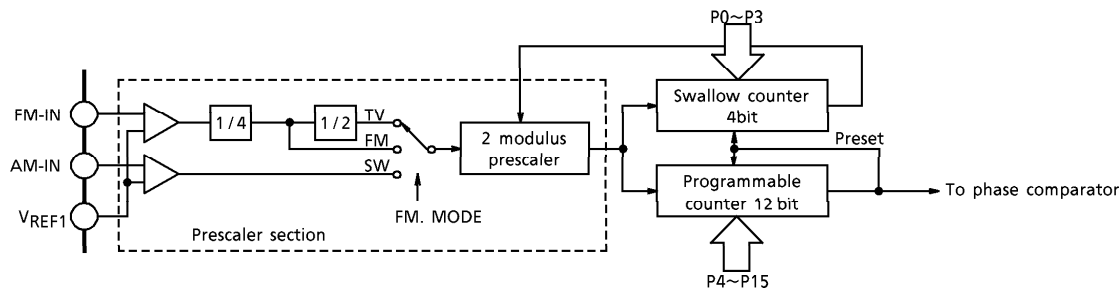2^{11} ————————————————————— 2^{0} [irrelevant   ]

Range of divisor set (direct divide mode) n = 10 H~FFFH (16~4095)

(Note) In the direct divide method, the data in P0~P3 becomes irrelevant and the P4 port becomes the LSB.

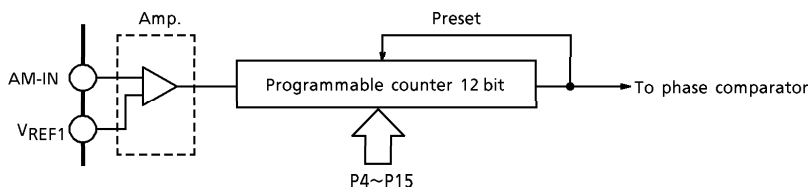2. Circuit configuration of prescaler and programmable counter
    (1) Circuit configuration in the pulse swallow mode

The circuit is configured with a 2 modulus prescaler, swallow counter (4 bits), and a programmable counter (12 bits).
In FM and TV modes, a 1 / 4 and a 1 / 8 prescaler are added in the front stage.

(2) Circuit configuration in the direct divide method

In the direct divide method, the prescaler section is passed through and the circuit consists of only a programmable counter (12 bits).

(3) The FM-IN and AM-IN inputs each have a built-in amp, and are therefore capable of capacitor-coupled, small-amplitude operation.

○ Reference counter (divider to generate the reference frequency)

The reference counter section is configured with a crystal oscillator and a counter. Using a 75 kHz crystal oscillator, this circuit can generate seven types of reference frequencies.

1. Setting the reference frequency

    Use the R0~R2 bits to set the reference frequency.

R2	R1	R0	REFERENCE FREQUENCY
0	0	0	1 kHz
0	0	1	3 kHz
0	1	0	3.125 kHz
0	1	1	5 kHz
1	0	0	6.25 kHz
1	0	1	12.5 kHz
1	1	0	25 kHz
1	1	1	Standby mode

● When REF code = 7 H (R0~R2 = 1), the device is placed in standby mode.

○ Phase comparator

The phase comparator compares the phase difference between the reference frequency signal fed from the reference frequency divider and the divided output from the programmable counter, and outputs the difference. In this way it controls the VCO through a low-pass filter to ensure that the frequencies and the phases of these two signals are matched to each other.

Because this phase comparator has two tri-state buffers DO1 and DO2 connected in parallel as its outputs, you can design the optimum filter cons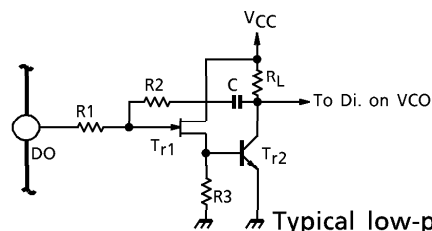tant for each of the FM and AM bands. Furthermore, you can use the DOHZ bit of register D2 to place the DO2 output in a high-impedance state as necessary.

DOHZ "1" : The DO2 pin is placed in the high-impedance state.
"0" : Nomal operation

DO output timing chart
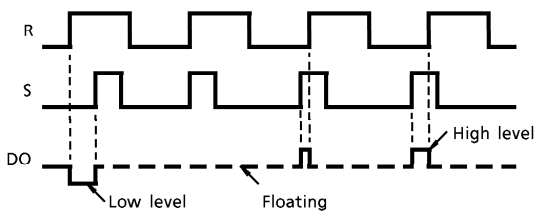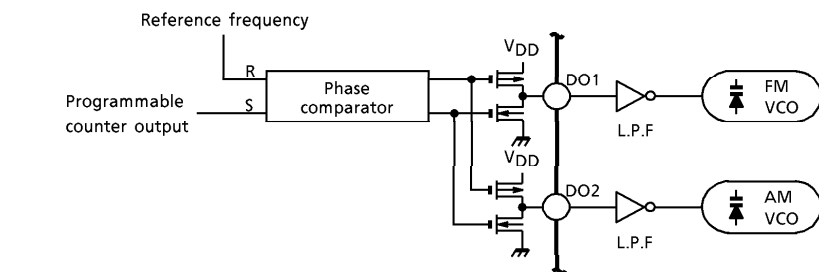
Example of an active low-pass filter circuit

Typ.
T_{r1} : 2SC1815
T_{r2} : 2SK246

Typical low-pass filter constant
(Reference value for FM band)
C = 0.33 μF
R1 = 10 kΩ
R2 = 8.2 kΩ
R3 = 330 Ω
R_L = 10 kΩ

Shown above is a DO output timing chart and a typical active low-pass filter circuit based on a Darlington connection of FET and bipolar transistors.

The filter circuit shown above is just one example. When designing the actual circuit, consider the band configuration and the desired characteristics of your system.

○ Unlock detection bit

This bit is used to detect an unlock condition of the PLL circuit. When not locked (i.e., the reference frequency and the programmable counter's divided output are not locked in phase), the phase comparator outputs a pulse to the unlock F/F synchronously with the period of the reference frequency. The unlock F/F is set by this pulse. The unlock F/F is reset each time the RESET bit of register 2 (unlock reset bit) is set to 1.

After the unlock F/F is reset in this way, you can access the unlock detection bit to see if the PLL circuit is in lock condition. Because the pulse is input synchronously with the period of the reference frequency, you must wait for a duration greater than the period of the reference frequency after resetting the unlock F/F before you can access the unlock detection bit (UNLOCK). If this duration is short, you cannot detect the correct lock condition.

To solve this problem, the device has a lock enable F/F. This F/F is reset each time the unlock reset bit is set to 1, and lock enable bit is set to 1 with the unlock detection timing. This means that you can detect the correct unlock condition when the lock enable bit (ENABLE) is 1.

ENABLE	UNLOCK	STATE
0	*	—
1	0	LOCK
	1	UNLOCK
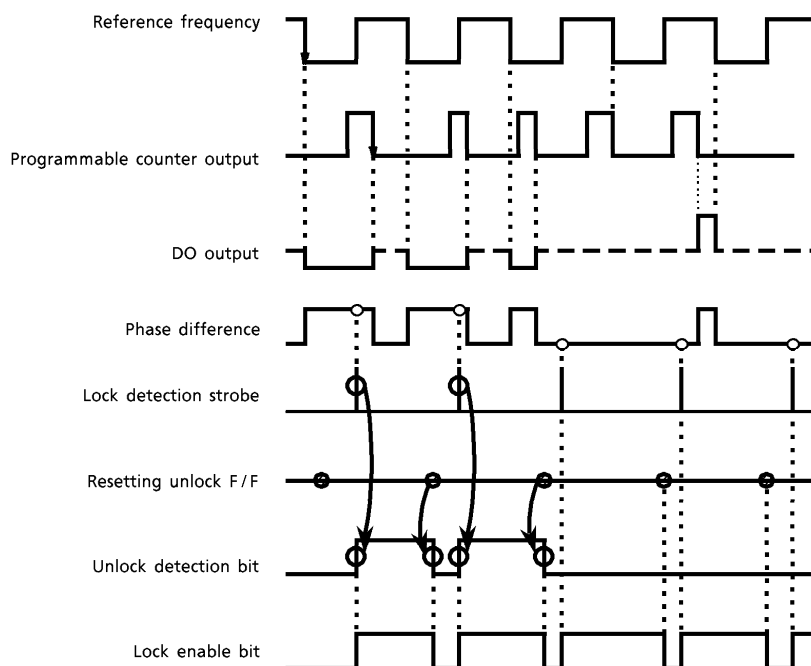
◯ General-purpose counter

The general-purpose counter is used to count frequencies such as the FM / AM band IF frequency to detect the auto stop signal during auto search tuning.

For this frequency counting, the general-purpose counter uses a frequency measurement (IF-AM, IF-FM input) method to count the number of pulses input to the counter during a certain duration of time (gate time).

1. General-purpose counter control bits

(1) G0, G1 bits   ⋯ These bits choose the general-purpose counter's gate time.

G0	G1	GATE TIME
0	0	1 ms
1	0	4 ms
0	1	16 ms
1	1	64 ms

(2) START bit   ⋯ Each time the START bit is set to 1, measurement is restarted after resetting the general-purpose counter.

(3) M8, M9 bits   ⋯ These bits choose the general-purpose counter's measurement mode and input pin.

M8	M9	PIN SELECTION	INPUT FREQUENCY RANGE	REMARKS
0	1	IF-AM	0.3~1.0 MHz	Direct input to IF counter
1	0	IF-FM	8~16 MHz	IF frequency divided by 2 input to IF counter

(Note) In the IF-FM mode, the general-purpose counter (20 bit binary counter) is preceded by an additionally inserted 1 / 2 prescaler. Therefore, the input signal from IF-FM is divided by 2 before being fed into the general-purpose counter.

2. General-purpose counter data output bits (f0~f19)

(1) General-purpose counter count data bits (f0~f19)

The resulting count of the general-purpose counter can be read in binary from the output registers f0 through f19.
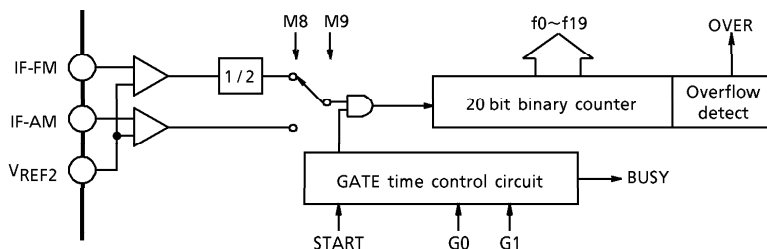
(2) General-purpose counter operation detect bits

OVER ⋯ General-purpose counter overflow bit ── "1" General-purpose counter is in overflow condition.
                                              └─ "0" General-purpose counter data is valid.

BUSY ⋯ General-purpose counter operation monitor ── "1" General-purpose counter is counting.
                                                    └─ "0" General-purpose counter has finished counting.

(Note) When using the general-purpose counter, check to see that the BUSY bit is 0 (finished counting) and that the OVER bit is 0 (valid data) before you reference the contents of the general-purpose counter data bits (f0~f19).

3. Circuit configuration of general-purpose counter

The general-purpose counter section is configured with an input amp., a gate time control circuit, and a 20 bit binary counter.

4. Measurement timing of general-purpose counter

Clock pulse of measured frequency
$0 < T_1 \leq 0.25$ (μs), $0 < T_2 \leq 1$ (ms)

Frequency measurement timing chart
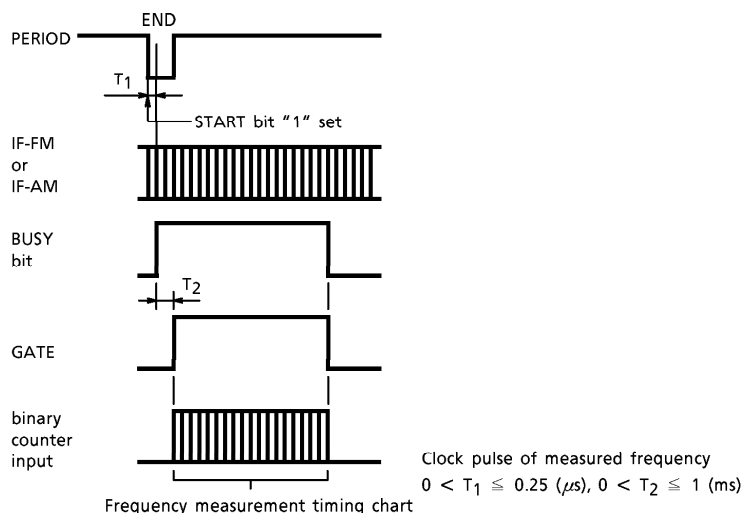
    (Note) IF-FM and IF-AM are capable of C-coupled, small-amplitude operation using a bipolar input.

○ General-purpose input / output ports

The device has general-purpose input / output ports controlled by serial port.

1. General-purpose output ports (OT-1~OT-4)

The data set to the O1~O4 bits of input register 2 are output in parallel from their dedicated output ports OT-1~OT-4.

2. General-purpose input port (IN)

The data input from the IN pin can be read out from the DATA pin as OUT-5 of the output register.

(Note) The output ports are set to "0" when the device is powered on. (Therefore, the general-purpose output ports are held Low at power-on.)

(Note) The TS bit of input register 2 must always be set to "0".

○ DC / DC converter

The TB2110FN uses a coil-type DC / DC converter (boosted voltage circuit) to allow for low-voltage operation.
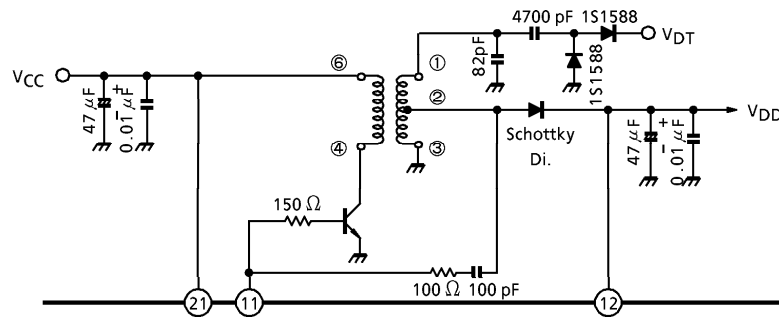
Coil : (SUMIDA ELECTRIC CO., LTD, CP-4LB)

TEST FREQUENCY	L (μH) 1-3	CO (pF)	QO	TURNS			WIRE (mmφ)
				1-2	2-3	6-4	
2.52 MHz	15.6 ± 3%	—	—	18T	14T	2T	0.08 UEW

BOTTOM VIEW

MAXIMUM RATINGS (Ta = 25°C)

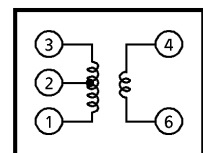| CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$-0.3 \sim 4.5$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	$-20 \sim 75$	°C
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, Ta = $-20 \sim 75$°C, V_{CC} = 1.0~2.5 V, V_{DD} = 2.4 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	Biplor Unit	V_{CC}	—	PLL operation (Normal operating)	1.2	1.5	2.5	V
	MOS Unit	V_{DD}		Step-up control circuit operating	2.2	2.4	3.6	
Operating Power Supply Current		I_{CC}	—	PLL operation (Normal operating), TV mode	—	18	40	mA
		I_{DD}	—	PLL operation (Normal operating), TV mode	—	1.5	7	

(Stand-by mode)

Operating Power Supply Current		I_{CS}	—	V_{CC} = 1.5 V	—	30	50	μA

(Operating frequency)

Crystal Oscillation Frequency		f_{XT}	—	Crystal oscillator connected to XI and XO pins.	—	75	—	kHz
TV in		f_{TV}	—	TV mode	50	~	250	MHz
FM in		f_{FM}	—	FM mode	40	~	150	MHz
SW in		f_{SW}	—	SW mode	3	~	40	MHz
AM in		f_{AM}	—	AM mode	0.5	~	10	MHz
IF-FM		f_{IF-FM}	—	IF-FM	8	~	16	MHz
IF-AM		f_{IF-AM}	—	IF-AM	0.3	~	1.0	MHz

(Input voltage)

TV in		V_{TVin}	—	TV mode				
FM in		V_{FMin}	—	FM mode				
SW in		V_{SWin}	—	SW mode	25	~	300	mV_{rms}
AM in		V_{AMin}	—	AM mode				
IF-FM		V_{IF-FM}	—	IF-FM				
IF-AM		V_{IF-AM}	—	IF-AM				

(OT-1~OT-4 open-collector output current)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"L" Level	I_{OL1}	—	$V_{OL} = 0.2\,V$	1.0	3.0	—	mA

(DATA, CLOCK, PERIOD, I/O)

CHARACTERISTIC		SYMBOL		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	—	1.7	~	V_{DD}	V
	"L" Level	V_{IL}	—	—	0.0	~	0.5	
Input Current	"H" Level	I_{IH}	—	$V_{IH} = 2.4\,V$	—	—	±0.5	μA
	"L" Level	I_{IL}	—	$V_{IL} = 0.0\,V$	—	—	±1.0	
Output Current	"H" Level	I_{OH2}	—	$V_{OH} = 2.0\,V$, Only DATA pin	−0.2	−1.0	—	mA
	"L" Level	I_{OL2}	—	$V_{OL} = 0.4\,V$, Only DATA pin	0.2	1.0	—	

(DO1, DO2)

CHARACTERISTIC		SYMBOL		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	I_{OH3}	—	$V_{OH} = 2.0\,V$	−0.2	−1.0	—	mA
	"L" Level	I_{OL3}	—	$V_{OL} = 0.4\,V$	0.2	1.0	—	
Tri-State Leak Current		I_{TL}	—	$V_{TLH} = 2.4\,V$, $V_{TLL} = 0.0\,V$	—	—	±0.1	μA

Auto Clear Voltage		V_{CL1}	—	Clear release voltage	—	—	1.9	V
		V_{CL2}	—	Clear voltage	1.4	—	—	

V_{CONT} Output Current		I_{CONT}	—	Boosting voltage transistor drive current $V_{CONT} = 0.8\,V$	100	150	—	μA
Standby Release		V_{STOFF}	—	Standby mode released	0.7	~	V_{CC}	V
Standby Mode		V_{STON}	—	Placed in standby mode	0.0	~	0.6	V

OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm

Weight : 0.31 g (Typ.)