SANYO

PRODUCT INFORMATION

Vol.51

Support for 2-million gate devices using a Sanyo-developed 3-metal layer technology

Orders for 0.35-µm ASICs Now Accepted

LC24000, LC27200 Series

Overview

In 1992, SANYO entered a technology sharing partnership for ASIC products with ASPEC Technology, Inc. (USA). The HDA (high-density architecture) technology resulting from that partnership achieves a 30% improvement in integration density over previous SANYO technology and the excellent cost-performance ratio provided by the HDA design rules have been well-received in the market. Thus SANYO ASSP and ASIC business has been growing briskly.

We have entered a new technology agreement concerning 0.35- and 0.25-µm ASICs and we are now accepting orders for the LC24000 Series (0.35-µm gate arrays) and the LC27200 Series (0.35-µm embedded arrays) products. Also, by inheriting earlier technologies, we can provide even faster mega-cells in analog/digital hybrid ASICs and can respond to our customers' diversifying needs.

These new ASIC series can contribute to the efficient implementation of superlative cost-performance ratio ICs for application areas that require larger scale circuits and improved speed. Application areas that can benefit from these ASIC series include office equipment, personal computer peripherals, portable equipment, and other information/communication areas as well as consumer products such as digital still cameras and digital TV and VCRs.

Furthermore, in addition to our existent CAD tool support system for achieving large-scale designs, we have adopted several new tools, including a static timing analysis tool (Motive*1), a test design that provides increased user choices in test design procedures, an accelerator tool that achieves increased speeds in logic design and an ECO that supports precise layout corrections. Thus we provide an environment in which design is even easier than before. In particular, this environment adopts both the AWE algorithm as a procedure for achieving high-precision delay calculations and local scaling factors with a wide variety of variation coefficients. These series also provide a full complement of personal computer interface macros, including IrDA, USB, ATAPI, SCSI, and IEEE 1394.

SANYO began accepting orders for these 0.35-µm ASIC series in November 1997, and plans to begin accepting orders for 0.25-µm ASICs in the later half of 1998.

Note: 1. Motive is a registered trademark of Viewlogic Systems, Inc.

SANYO Electric Co., Ltd. Semiconductor Business Headquarters Overseas Marketing Division
TOKYO OFFICE: Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

PRODUCT INFORMATION

Features

- Support for 2-million gate devices using a SANYO-developed 0.35-µm 3-metal layer technology.
- These 0.35-µm ASICs can interface with either 3.3-V or 5-V external signals without the use of any special external circuits even in a system where both 3.3-V and 5-V circuits are combined on the same board .
- An extensive lineup of megacells supports the development of large-scale system ICs.
- Our customers custom circuits and ASSPs designed using ASIC techniques can be integrated on a single chip.
- Power dissipation can be estimated precisely at simulation time using power simulator "A Power". Power dissipation is estimated precisely by referencing a library of current drain values that depend on the load capacitance and individual cell waveform distortions based on the Verilog*2 simulation file.
- The adoption of Quick Port, which is an inter-ASIC transplant tool that adopts the HDA concept, allows data migration between ASPEC libraries to be performed easily in the layout database.

  While it goes without saying that data migration can be performed easily in the layout database for data from the same vendor, this system also supports data migration between data from different vendors.
- FPGA designs can be easily converted to these ASIC products.
- Full scan is supported for test design.
- A high-level language (RTL) interface is supported.

Note: 2. Verilog is a registered trademark of Cadence Design Systems, Inc.

Specifications

- 0.35-µm 3-metal layer gate arrays

  Maximum number of gate devices incorporated: 2,000,000

  Maximum number of gate devices usable: 1,400,000

  Delay time: 100 ps (power gate, standard load)

  Power supply voltage: 3.3V
- 0.35-µm 3-metal layer embedded arrays

CPU core	8 bits	65C02S
	16 bits	65C816
	32-bit RISC	Original
CPU peripheral	82CXX Series	
Memory	SRAM (single, dual), DRAM, Line memory, FIFO, and ROM	
Analog blocks	6-, 8-, 10-bit A/D converters, 6-, 8-, 10-bit D/A converters, operational amplifiers, LCD drivers, and PLL	
PC interfaces	USB, ATAPI, SCSI, PCMCIA, IrDA, and IEEE1394 (under development)	

PRODUCT INFORMATION

Sample Availability

Samples of the LC24000, LC27200 Series are available in November 1997.

NOVEMBER7, 1997

SANYO Electric Co., Ltd. Semiconductor Business Headquarters Overseas Marketing Division

11498/51