NCP5210

Product Preview

3-In-1 PWM Dual Buck and Linear DDR Power Controller

The NCP5210, 3−In−1 PWM Dual Buck and Linear DDR Power Controller, is a complete power solution for MCH and DDR memory. This IC combines the efficiency of PWM controllers for the VDDQ supply and the MCH core supply voltage with the simplicity of linear regulator for the V_{TT} termination voltage.

This IC contains two synchronous PWM buck controller for driving four external NFETs to form the DDR memory supply voltage (VDDQ) and the MCH regulator. The DDR memory termination regulator (VTT) is designed to track at the half of the reference voltage with sourcing and sinking current.

Protective features include, soft−start circuitry, under−voltage monitoring of 5VDUAL, and BOOT voltage, and thermal shutdown. The IC is packaged in QFN−20.

Features

- Incorporates Synchronous PWM Buck Controllers for VDDQ and VMCH
- Integrated Power FETs with VTT Regulator Source/Sink up to 1.8 A
- All External Power MOSFETs are N−channel
- Adjustable VDDQ and VMCH by External Dividers
- VTT Tracks at Half the Reference Voltage
- Fixed Switching Frequency of 250 kHz for VDDQ and VMCH
- Doubled Switching Frequency (500 kHz) for VDDQ Controller in Standby Mode to Optimize Inductor Current Ripple and Efficiency
- Soft−start Protection for all Controllers
- Under−Voltage Monitor of Supply Voltages
- Over−Current Protections for DDQ and VTT Regulators
- Fully Complies with ACPI Power Sequencing Specifications
- Short Circuit Protection Prevents Damage to Power Supply Due to Reverse DIMM Insertion
- Thermal Shutdown
- 20−Lead 5x6 QFN Package

Typical Applications

- DDR I and DDR II Memory and MCH Power Supply

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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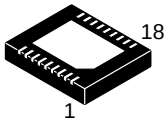
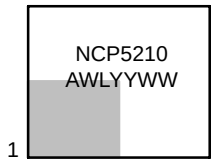


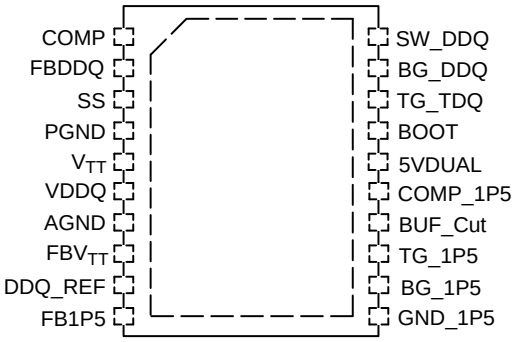
20−LEAD QFN
MN SUFFIX
CASE 505

MARKING DIAGRAMS



NCP5210 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NCP5210MN	20−Lead QFN*	Rail
NCP5210MNR2	20−Lead QFN*	Tape and Reel

*5 x 6 mm

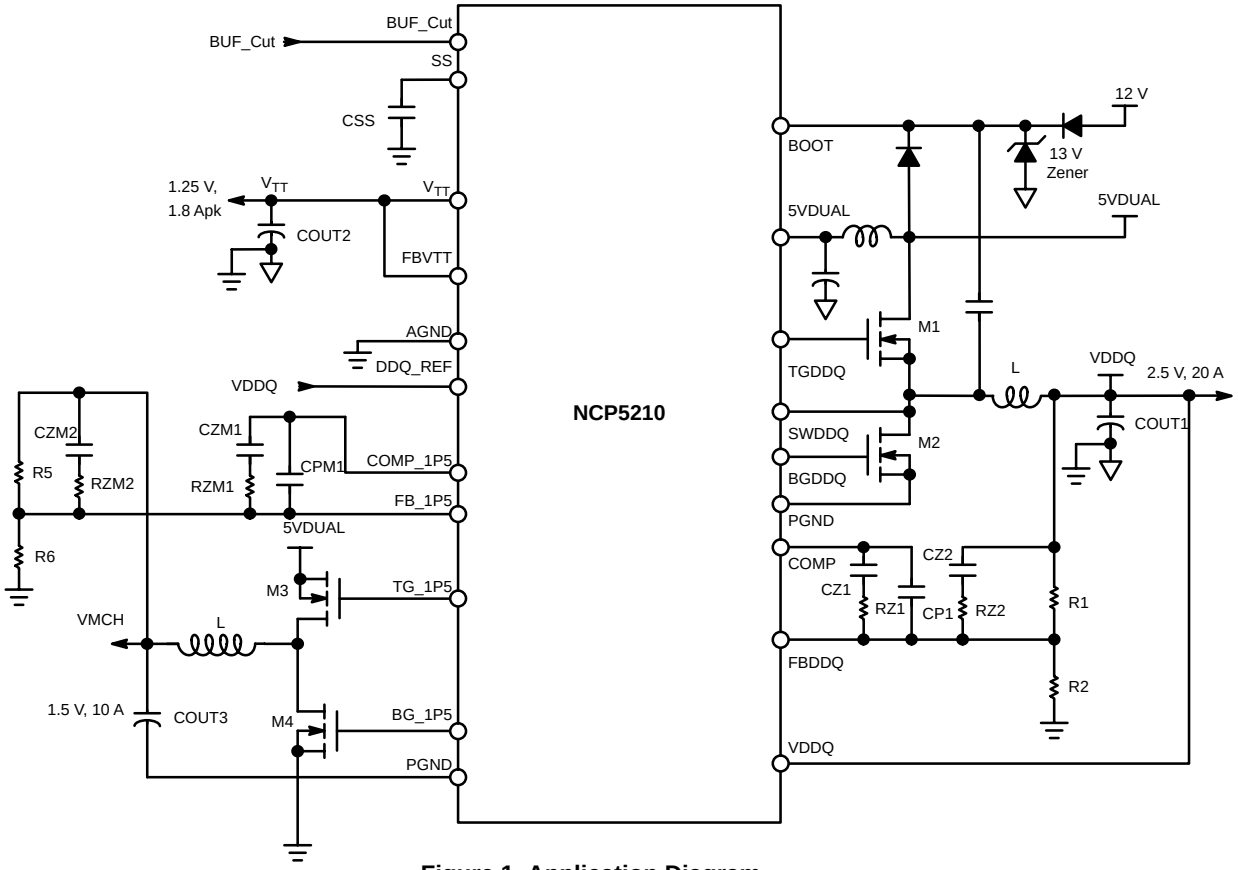


Figure 1. Application Diagram

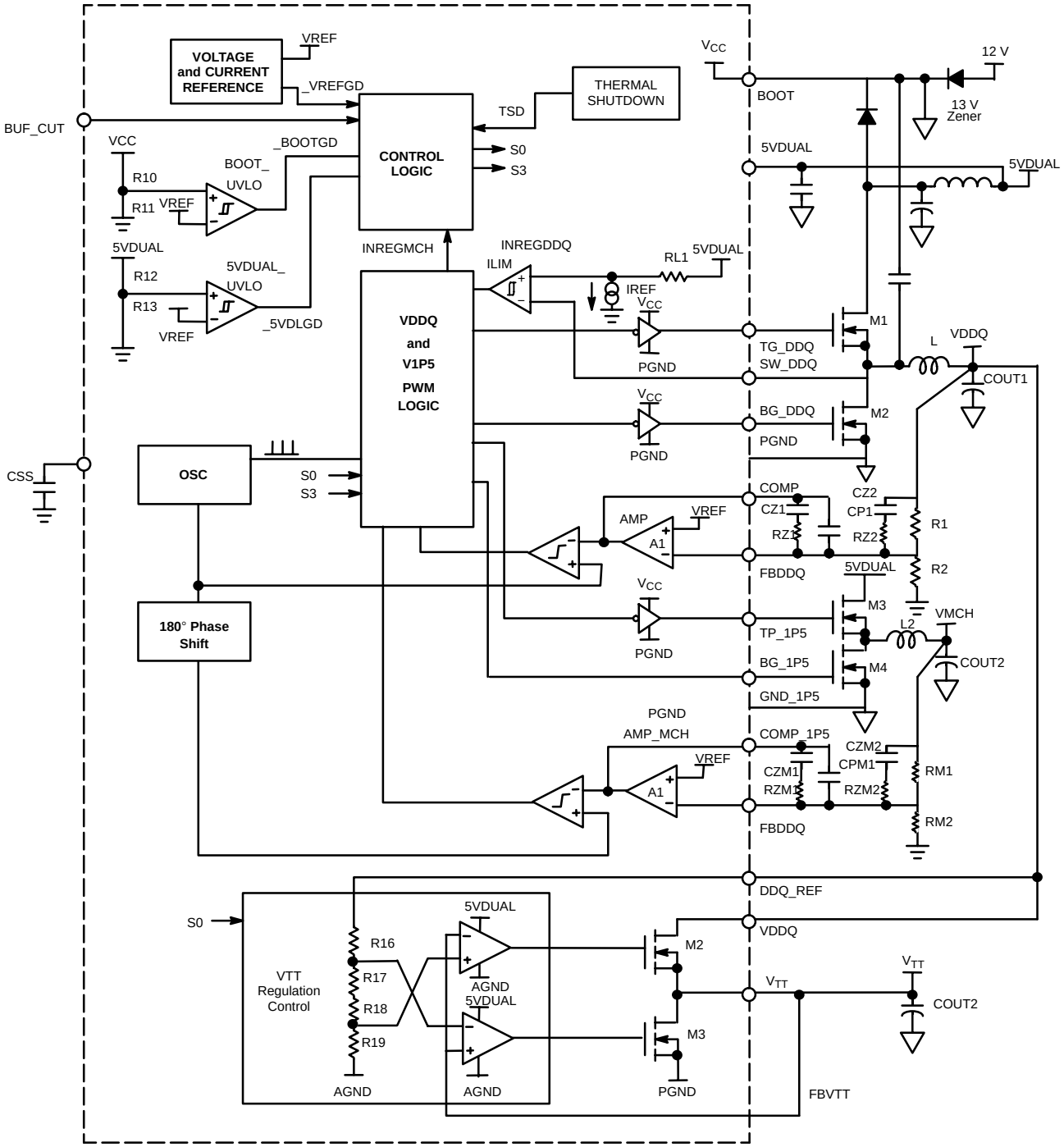


Figure 2. Internal Block Diagram

PIN DESCRIPTION

Pin	Symbol	Description
1	COMP	VDDQ error amplifier compensation node
2	FBDDQ	DDQ regulator feedback pin for closed loop regulation
3	SS	Soft−start pin of DDQ regulator connecting a capacitor
4	PGND	Power ground
5	VTT	VTT regulator output
6	VDDQ	Power input for VTT linear regulator
7	AGND	Analog ground connection and remote ground sense
8	FBVTT	VTT regulator feedback pin for closed loop regulation
9	DDQ_REF	Reference voltage input of VTT regulator
10	FB1P5	V1P5 Switching Regulator feedback pin for closed loop regulation
11	GND_1P5	Power ground for V1P5 regulator
12	BG_1P5	Gate driver output for V1P5 regulator low side N−Channel Power FET
13	TG_1P5	Gate driver output for V1P5 regulator high side N−Channel Power FET
14	BUF_Cut	Active High control signal to activate S3 Sleep State
15	COM_1P5	V1P5 error amplifier compensation node
16	5VDUAL	5V Dual supply input, which is monitored by under−voltage lock out circuitry
17	BOOT	Gate driver input supply, which is monitored by under−voltage lock out circuitry, and a boost capacitor connection between SWDDQ and this pin
18	TG_DDQ	Gate driver output for DDQ regulator high side N−Channel Power FET
19	BG_DDQ	Gate driver output for DDQ regulator low side N−Channel Power FET
20	SW_DDQ	DDQ regulator inductor driven node and current limit sense input

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 16) to AGND (Pin 7)	5VDUAL	−0.3, 6.0	V
Gate Drive Voltage (Pin 12, 13, 17−19) to AGND (PIN 7)	VCC, Vg	−0.3, 14	V
Input / Output Pins to AGND (Pin 7) Pin 1−6, 8−11, 14−16, 20	V_{IO}	−0.3, 6.0	V
Thermal Characteristics QFN−20 Plastic Package Thermal Resistance Junction to Air	$R_{\theta JA}$	35(TBD)	°C/W
Operating Junction Temperature Range	T_J	0 to + 150	°C
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	− 55 to +150	°C
Moisture Sensitivity Level	MSL	2	

1. This device series contains ESD protection and exceeds the following tests: Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22–A114. Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22–A115.
2. Latch–up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (5VDUAL = 5 V, BOOT = 12 V, 5VATX = 5 V, DDQ_REF = 2.5 V, T_A = 0°C to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = NA, CSS = 33 nF, RL1 = 200 kΩ, R1 = 2.166 kΩ, R2 = 2 kΩ, RZ1 = 20 kΩ, RZ2 = 8 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, RM1 = 2.166 kΩ, RM2 = 2 kΩ, RZM1 = 20 kΩ, RZM2 = 8 Ω, CPM1 = 10 nF, CZM1 = 6.8 nF, CZM2 = 100 nf for min/max values unless otherwise noted.) duplicate component values of MCH regulator from DDQ.

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
5VDUAL Operating Voltage		V5VDUAL	4.5	5.0	5.5	V
BOOT Operating Voltage		VBOOT	8.0	12.0	13.2	V
SUPPLY CURRENT						
S0 mode Supply Current from 5VDUAL	BUF_Cut = LOW, BOOT = 12 V	I5VDL_S0			6	mA
S3 mode Supply Current from 5VDUAL	BUF_Cut = HIGH	I5VDL_S3				mA
S5 mode Supply Current from 5VDUAL	BUF_Cut = LOW,	I5VDL_S5			1	mA
S0 mode Supply Current from BOOT	BUF_Cut = LOW, BOOT = 12 V, TGDDQ, BGDDQ , TG_1P5 and BG_1P5 Open	IBOOT_S0			20	mA
S3 mode Supply Current from BOOT	BUF_Cut=HIGH, TGDDQ, BGDDQ, TG_1P5 and BG_1P5 Open	IBOOT_S3			20	mA
UNDER−VOLTAGE−MONITOR						
5VDUAL UVLO Upper Threshold		V5VDLUV+			4.4	V
5VDUAL UVLO Hysteresis		V5VDLhys		300		mV
BOOT UVLO Upper Threshold		VBOOTUV+			10.2	V
BOOT UVLO Hysteresis		VBOOThys		1		V
THERMAL SHUTDOWN						
Thermal Shutdown		Tsd		150		°C
Thermal Shutdown Hysteresis		Tsdhys		25		°C
DDQ SWITCHING REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	Ta = 25°C Ta = 0°C to 70°C	VFBQ	1.188 1.176	1.200	1.212 1.224	V
Feedback Input Current	V(FBDDQ) = 1.3 V	IDDQfb			1	μA
Oscillator Frequency in S0 Mode		FDDQS0	225	250	275	KHz
Oscillator Frequency in S3 Mode		FDDQS3	450	500	550	KHz
Current Limit Blanking Time in S0 Mode		TDDQbk	400			nS
Minimum Duty Cycle		Dmin	0			%
Maximum Duty Cycle		Dmax			100	%
Soft−Start Pin Current for DDQ	V(SS) = 0.5 V	Iss1		4		μA
DDQ ERROR AMPLIFIER						
DC Gain		GAINDDQ		70		dB
Gain−Bandwidth Product	COMP PIN to GND = 220nF, 1 Ω in Series	GBWDDQ		TBD		MHz
Slew Rate	COMP PIN TO GND = 10 pF	SRDDQ		8		V/uS
VTT ACTIVE TERMINATION REGULATOR						
VTT tracking DDQ_REF/2 at S0 mode	IOUT= 0 to 1.8A (sink current)IOUT= 0 to –1.8A (source current)	dVTTS0	−30		30	mV
VTT Source Current Limit		ILIMVTsrc		2.4		A
VTT Sink Current Limit		ILIMVTsnk		2.4		A
DDQ_REF Input Resistance		DDQREF		50		Ω

ELECTRICAL CHARACTERISTICS (5VDUAL = 5 V, BOOT = 12 V, 5VATX = 5 V, DDQ_REF = 2.5 V, T_A = 0°C to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = NA, CSS = 33 nF, RL1 = 200 kΩ, R1 = 2.166 kΩ, R2 = 2 kΩ, RZ1 = 20 kΩ, RZ2 = 8 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, RM1 = 2.166 kΩ, RM2 = 2 kΩ, RZM1 = 20 kΩ, RZM2 = 8 Ω, CPM1 = 10 nF, CZM1 = 6.8 nF, CZM2 = 100 nf for min/max values unless otherwise noted.) duplicate component values of MCH regulator from DDQ.

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CONTROL SECTION						
BUF_Cut Input Logic HIGH		Logic_H	2.0			V
BUF_Cut Input Logic LOW		Logic_L			0.8	V
BUF_Cut Input Current		Ilogic			1	μA
GATE DRIVERS						
TGDDQ Gate pull−HIGH Resistance	VCC = 12 V, V(TGDDQ) = 11 V	RH_TG		3		Ω
TGDDQ Gate pull−LOW Resistance	VCC = 12 V, V(TGDDQ) = 1 V	RL_TG		2.5		Ω
BGDDQ Gate pull−HIGH Resistance	VCC = 12 V, V(BGDDQ) = 11 V	RH_BG		3		Ω
BGDDQ Gate pull−LOW Resistance	VCC = 12 V, V(BGDDQ) = 1 V	RL_BG		1.3		Ω
TG1P5 Gate pull−HIGH Resistance	VCC = 12 V, V(TG1P5) = 11 V	RH_TPG		3		Ω
TG1P5 Gate pull−LOW Resistance	VCC = 12 V, V(TG1P5) = 1 V	RL_TPG		2.5		Ω
BG1P5 Gate pull−HIGH Resistance	VCC = 12 V, V(BG1P5) = 11 V	RH_BPG		3		Ω
BG1P5 Gate pull−LOW Resistance	VCC = 12 V, V(BG1P5) = 1 V	RL_BPG		1.3		Ω
MCH SWITCHING REGULATOR						
VFB1P5 Feedback Voltage, control loop in regulation	Ta = 0°C to 70°C	VFB1P5	0.784	0.8	0.816	V
Feedback Input Current		I1P5FB			1	μA
Oscillator Frequency		F1P5	225	250	275	KHz
Minimum Duty Cycle		Dmin_1P5	0			%
Maximum Duty Cycle		Dmax_1P5			100	%
Soft−start Pin Current for V1P5 regulator		ISS2		8		μA

DETAILED OPERATION DESCRIPTIONS

General

The NCP5210 3−In−1 PWM Dual Buck Linear DDR Power Controller contains two high efficiency PWM controllers and an integrated two−quadrant linear regulator.

The VDDQ supply is produced by a PWM switching controller with two external NFETs. The VTT termination voltage is an integrated linear regulator with sourcing and sinking current capability which tracks at 1/2 VDDQ. The MCH core voltage is created by the secondary switching controller.

The inclusion of soft−start, supply under−voltage monitors, short circuit protection and thermal shutdown, makes this device a total power solution for the MCH and DDR memory system. This device is packaged in a QFN−20.

ACPI Control Logic

The ACPI control logic is powered by the 5VDUAL supply. It accepts external control at the BUF_CUT input, and internal supply voltage monitoring signals from two UVLOs to decode the operating mode in accordance with state transition diagram in Figure 3.

These UVLOs monitor the external supplies, 5VDUAL and 12VATX, through 5VDUAL and BOOT pins respectively. Two control signals, _5VDUALGD and _BOOTGD, are asserted when the supply voltages are good.

The device powers up initially in the S5 shutdown mode to minimize the power consumption. When all three supply voltages are good and BUF_CUT is LOW, the device enters the S0 normal operating mode. When BUF_CUT transitions from LOW to HIGH in S0 mode the device goes into the S3 sleep mode. In S3 mode the 12VATX supply collapses. On transition of BUF_CUT from HIGH to LOW, the device returns to S0 mode. The IC re−enters S5 mode if one of the supplies is removed during S0 mode. Transitions from S3 to S5 or vice versa are not allowed. A timing diagram is shown in Figure 3.

Table 1 summarizes the operating states of all the regulators, as well as the conditions of output pins.

S5 To S0 Mode Power Up Sequence

An internal bandgap reference is generated whenever 5VDUAL exceeds 2.7 V. Once this bandgap reference is in regulation, an internal signal _VREFGD is asserted.

The ACPI control logic is enabled by the assertion of _VREFGD. Once the ACPI control is activated, the power up sequence starts by waking up the 5VDUAL voltage monitor block. If the 5VDUAL supply is within the preset levels, the BOOT under voltage monitor block is then enabled. After the BOOT UVLO is asserted HIGH, the ACPI control triggers this device from S5 shutdown mode into S0 normal operating mode by activating the soft−start of DDQ switching regulator, providing BUF_CUT remaining LOW.

Once the DDQ regulator is in regulation and the soft−start interval is completed, the _InRegDDQ signal is asserted HIGH to enable the VTT regulator as well as the V1P5 switching regulator.

DDQ Switching Regulator

In S0 mode the DDQ regulator is a switching synchronous rectification buck controller driving two external power NFETs to supply up to 20 A. It employs voltage mode fixed frequency PWM control with external compensation switching at 250kHz ± 10%. As shown in Figure 2, the VDDQ output voltage is divided down and fed back to the inverting input of an internal amplifier through the FBDDQ pin to close the loop at VDDQ = VFBQ × (1 + R2/R1). This amplifier compares the feedback voltage with an internal reference voltage of 1.200 V to generate an error signal for the PWM comparator. This error signal is compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. The PWM signal drives the external NFETs via the TG_DDQ and BG_DDQ pins. External inductor L and capacitor COUT1 filter the output waveform. When the IC leaves the S5 state, the VDDQ output voltage ramps up at a soft−start rate controlled by the capacitor at the SS pin. When the regulation of VDDQ is detected in S0 mode, _INREGDDQ goes HIGH to notify the control block.

In S3 standby mode, the switching frequency is doubled to reduce the conduction loss in the external NFETs.

Table 1. Mode, Operation and Output Pin Condition

MODE	OPERATING CONDITIONS		OUTPUT PIN CONDITIONS			
	DDQ	VTT	TGDDQ	BGDDQ	TP_1P5	BG_1P5
S0	Normal	Normal	Normal	Normal	Normal	Normal
S3	Standby	H−Z	Standby	Standby	Low	Low
S5	H−Z	H−Z	Low	Low	Low	Low

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive non−overlap timing control of the complementary gate drive output signals is provided to reduce shoot−through current that degrades efficiency.

Tolerance of VDDQ

Both the tolerance of VFBQ and the ratio of the external resistor divider R2/R1 impact the precision of VDDQ. With the control loop in regulation, VDDQ = VFBQ × (1 + R2/R1). With a worst case (for all valid operating conditions) VFBQ tolerance of ±1.5%, a worst case range of ±2% for VDDQ will be assured if the ratio R2/R1 is specified as 0.9455 ±1%.

Fault Protection of VDDQ Regulator

In S0 mode, an internal voltage (VOCP) = 5VDUAL – 0.8 sets the current limit for the high−side switch. The voltage VOCP pin is compared to the voltage at SWDDQ pin when the high−side gate drive is turned on after a fixed period of blanking time to avoid false current limit triggering. When the voltage at SWDDQ is lower than VOCP, an over−current condition occurs and all regulators are latched off to protect against over−current. The IC can be powered up again if one of the supply voltages, 5VDUAL or 12VATX, is recycled.

In S3 mode, this over−current protection feature is disabled.

Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 2.

VTT Active Terminator

The VTT active terminator is a 2 quadrant linear regulator with two internal NFETs to provide current sink and source capability up to 1.8A. It is activated only when the DDQ regulator is in regulation in S0 mode. It draws power from VDDQ with the internal gate drive power derived from 5VDUAL. While VTT output is connecting to the FBVTT pin directly, VTT voltage is designed to automatically track at the half of DDQ_REF. This regulator is stable with any value of output capacitor greater than 470 μF, and is insensitive to ESR ranging from 1−mΩ to 400 mΩ.

Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, bi−directional current limit preset at 2.4 A magnitude is implemented. This current limit is also used as constant current source during VTT startup.

MCH Switching Regulator

The secondary switching regulator is identical to the DDQ regulator except the output is 10 A, no fault protection is implemented and the soft−start timing is twice as fast with respect to CSS.

BOOT Pin Supply Voltage

In typical application, a flying capacitor is connected between SWDDQ and BOOT pins. In S0 mode, 12VATX is tied to BOOT pin through a Schottky diode as well. A 13−V Zener clamp circuit must clamp this boot strapping voltage produced by the flying capacitor in S0 mode.

In S3 mode the 12VATX is collapsed and the BOOT voltage is created by the Schottky diode between 5VDUAL and BOOT pins as well as the flying capacitor.

Thermal Consideration

Assuming an ambient temperature of 50°C, the maximum allowed dissipated power of QFN−20 is 2.8 W, which is enough to handle the internal power dissipation in S0 mode. To take full advantage of the thermal capability of this package, the exposed pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact.

Thermal Shutdown

When the junction temperature of the IC exceeds 150°C, the entire IC is shutdown. When the junction temperature drops below 115°C, the chip resumes normal operation.

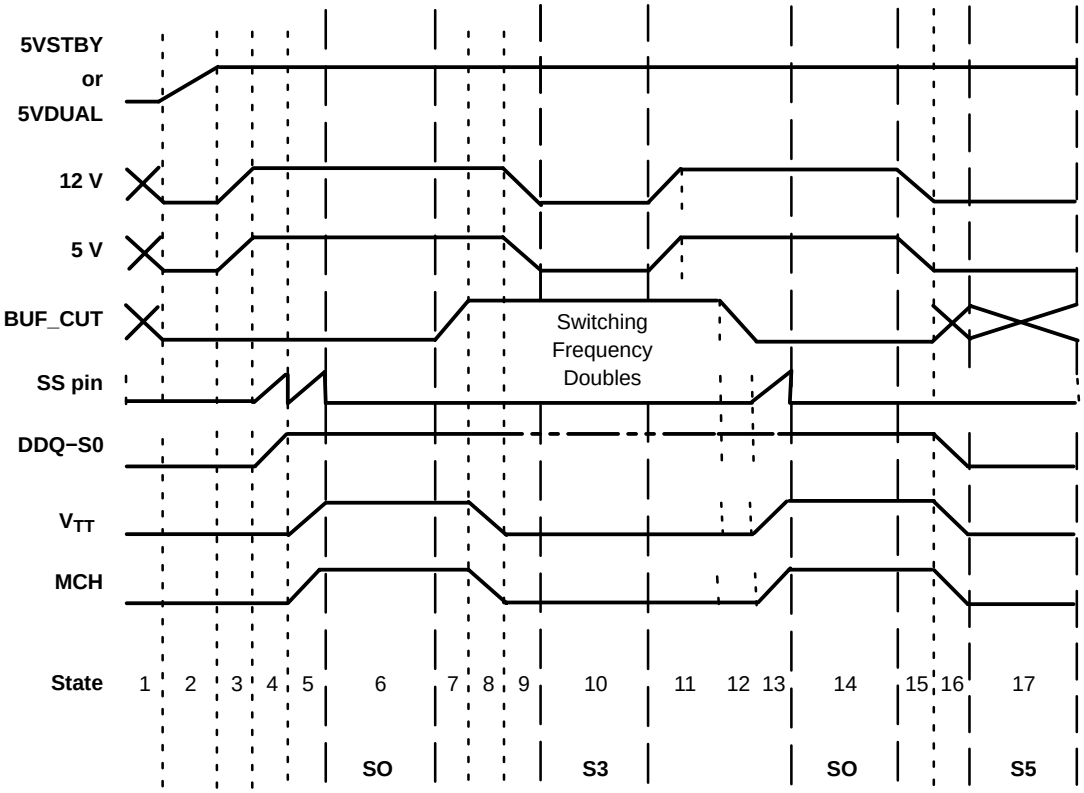


Figure 3. NCP5210 Power−up and Power−down

2. 5VSTBY or 5VSTB is the Ultimate Chip Enable. This supply has to be up first to ensure gates are in known state.
3. 12 V and 5 V supplies can ramp in either order.
4. DDQ will ramp with the tracking of SS pin, timing is 1.2 * C_{SS} / 4 μ (sec).
5. DDQ SS is completed, then SS pin is released from DDQ. SS pin is shorted to ground.
5. MCH ramps with the tracking of SS pin ramp, timing is 1.2 * C_{SS} / 8 μ (sec). V_{TT} rises.
6. MCH SS is completed, then SS pin is released from MCH. SS pin is shorted to ground. S0 Mode.
7. S3 MODE − BUF_CUT = H
8. VTT and MCH will be turned off.
9. 12 V and 5 V ramps to 0 V.
10. Standard S3 State
11. 12 V and 5 V ramps back to regulation.
12. BUF_CUT goes LOW
13. 12 V UVLO = L and BUF_CUT = L. MCH ramps with SS pin, timing is 1.2 * C_{SS} / 8 μ (sec). V_{TT} rises.
14. S0 Mode
15. S5 Mode − BUF_CUT = L, and 12VUVLO = H or 5VUVLO = H
16. DDQ, V_{TT}, and MCH Turned OFF
17. S5 Mode

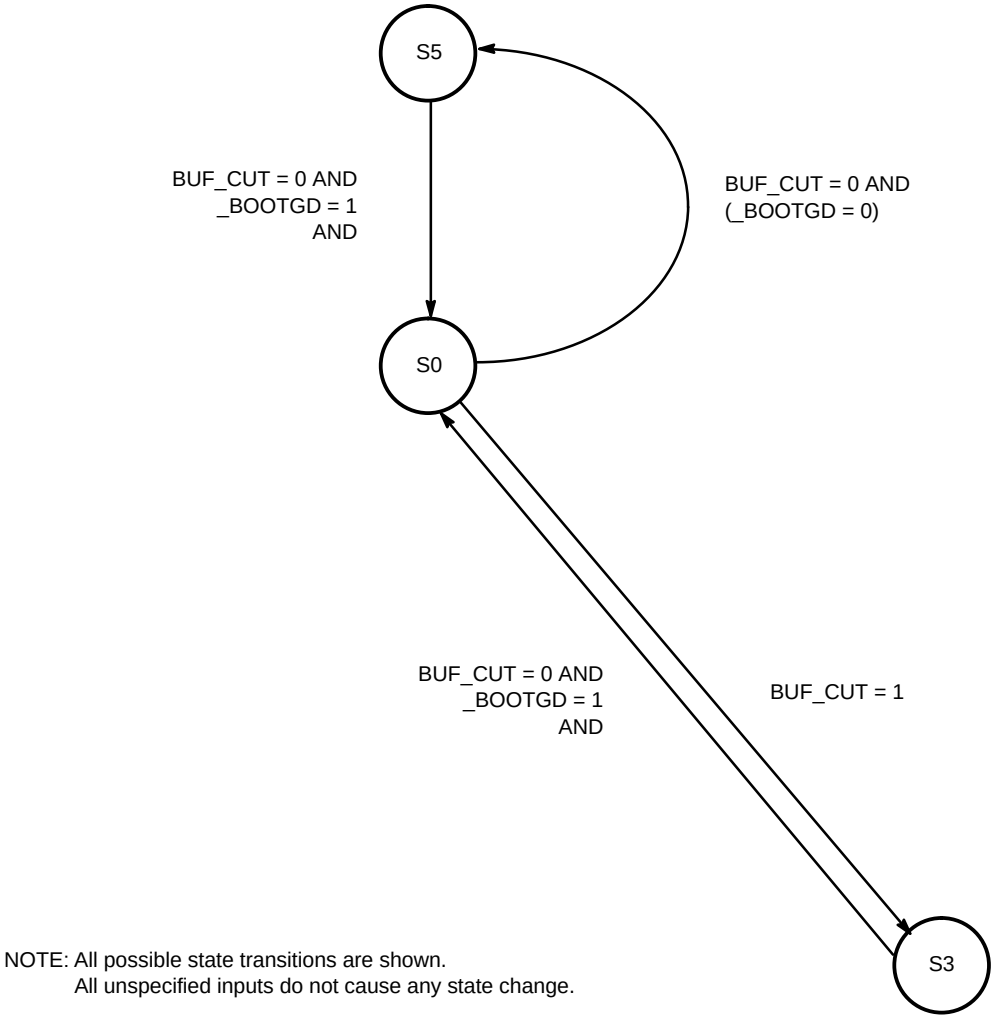
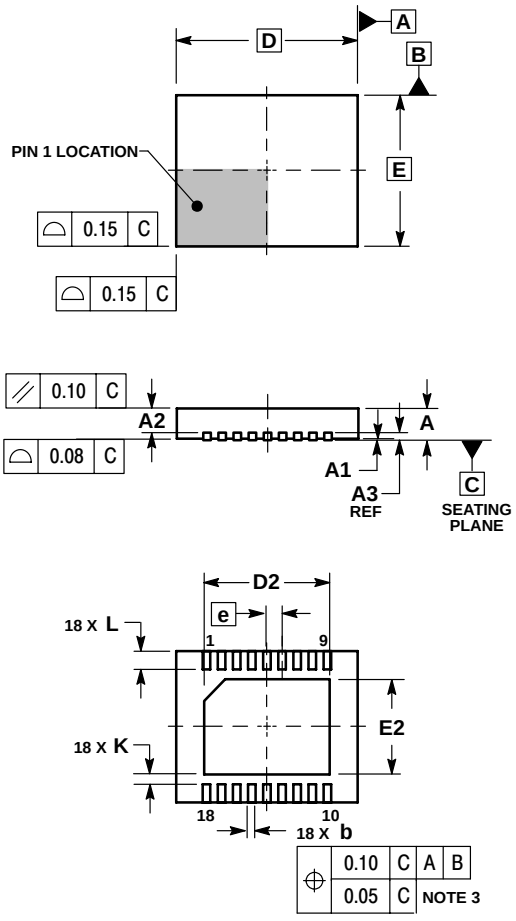


Figure 4. Transitions State Diagram of NCP5210

PACKAGE DIMENSIONS

QFN
MN SUFFIX
CASE 505−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.23	0.28
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

PUBLICATION ORDERING INFORMATION

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