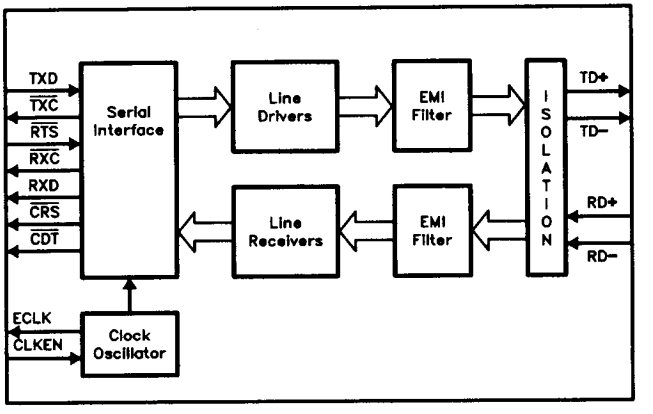
82521TA
TWISTED PAIR ETHERNET* SERIAL SUPERCOMPONENT

- **Provides Complete Serial and Analog Twisted Pair Ethernet Interface**
  - **— Analog Filters**
  - **— Serial Interface and Transceiver**
  - **— Manchester Decoder**
  - **— Isolation Transformers**
  - **— Protection Circuitry**
  - **— Line Drivers and Receivers**
- **10 Mb/s Operation**
- **Compatible with AT&T Multiport Repeater**
- **Directly Interfaces Intel Ethernet LAN Controllers**
  - **— 82586**
  - **— 82590**
  - **— 82592**
  - **— 82596SX, 82596DX, 82596CA**
- **No Configuration or Adjustment Required**
- **Satisfies FCC Class A Standards (FCC 47CFR, Part 15, Subpart J)**
- **All Circuitry Is in a Single, 36-Pin, Sealed Package**

The Twisted Pair Ethernet Serial Supercomponent (SSC) provides the complete serial interface and analog required to connect the Ethernet LAN controller directly to the twisted pair wire connector. It is designed for node applications using 10 Mb/s Manchester coded data; for example, PCs, workstations, and fileservers. The SSC includes the serial interface/transceiver, Manchester decoder, line drivers and receivers, analog filters, protection circuitry, and isolation transformers in a single, sealed package. It provides all required analog circuitry—giving the LAN designer immediate access to the twisted pair Ethernet environment. Existing Ethernet/Cheapernet designs can be easily modified to take advantage of cost-effective twisted pair wire. The SSC can be soldered or socketed onto a host adapter card or motherboard without any adjustments or configuration. It is compatible with the existing AT&T STARLAN**10 Multiport Repeater and can be used with non-Intel LAN controllers. The SSC satisfies FCC class A test requirements and is designed to meet all standard host-system size and power requirements.

82521TA Block Diagram



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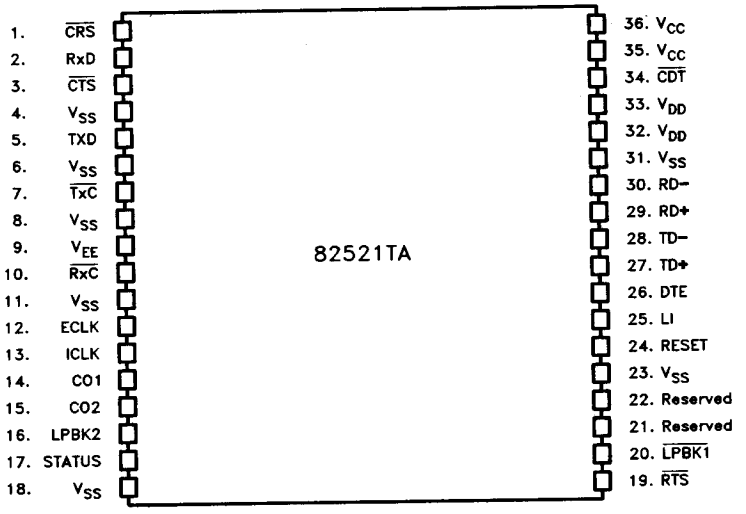
**STARLAN is a registered trademark of AT&T.

October 1989
Order Number: 290221-001

82521TA Pin Configuration



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PIN DESCRIPTION

Pin	Symbol	Type	Name and Function
1	$\overline{CRS}$	O	**CARRIER SENSE.** Active low output that alerts the 82586 (or other Ethernet controller) activity exists on the twisted pair link. This pin is directly connected to the $\overline{CRS}$ input of the controller.
2	RxD	O	**RECEIVE DATA.** NRZ data passed to the Ethernet controller. This pin is directly connected to the RxD pin on the controller.
3	$\overline{CTS}$	O	**CLEAR TO SEND.** Active low output that alerts the Ethernet Controller the device is ready to accept data. Implementation of this function is optional. This pin can be tied directly to the $\overline{CTS}$ pin of the controller. Internally, the pin is tied to V_{SS}.
4	V_{SS}	—	**GROUND**
5	TxD	I	**TRANSMIT DATA.** Manchester encoded serial data from the Ethernet controller. This pin is directly connected to the TxD pin of the controller.
6	V_{SS}	—	**GROUND**
7	$\overline{TxC}$	O	**TRANSMIT CLOCK.** A 10-MHz clock output tied directly to the $\overline{TxC}$ pin of the Ethernet controller.
8	V_{SS}	—	**GROUND**
9	V_{EE}	—	**V_{EE}.** A −5-V ±10% power supply.
10	$\overline{RxC}$	O	**RECEIVE CLOCK.** A 10-MHz clock connected directly to the $\overline{RxC}$ input of the Ethernet controller. This clock is the recovered clock from the data on the twisted pair.
11	V_{SS}	—	**GROUND**
12	ECLK	O	**EXTERNAL CLOCK.** A 20-MHz ±0.01%, TTL-level input clock with a 40/60 duty cycle. ECLK attaches to ICLK for normal asynchronous operation. ECLK can be used for synchronous operation of interface circuitry.
13	ICLK	I	**INTERNAL CLOCK.** A 20-MHz ±0.01%, TTL-level output clock with 40/60 duty cycle. For normal, asynchronous operation this pin is directly connected to ECLK. Operation of the host can be made synchronous by connecting ICLK.
14	CO1	I	**COMPATIBILITY OPTION 1.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions to enable compatibility mode with current product. If not connected, or strapped low, the future device will be in 10BASE-T compliant mode. Intel recommends that the input to this pin be programmable.
15	CO2	I	**COMPATIBILITY OPTION 2.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions to enable compatibility mode with current product. If not connected, or strapped low, the future device will be in 10BASE-T compliant mode. Intel recommends that the input to this pin be programmable.
16	LPBK2	I	**LOOPBACK 2.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions. An active high signal that will cause a loopback of the transmitted signal. The twisted pair medium will be removed from the circuit.

PIN DESCRIPTION (Continued)

Pin	Symbol	Type	Name and Function
17	STATUS	O	**Status.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions. An active high output which will indicate fault conditions in the supercomponent.
18	V_{SS}	—	**GROUND**
19	$\overline{RTS}$	I	**REQUEST TO SEND.** Active low signal synchronous to $\overline{TxC}$, it enables data transmission on the twisted pair link segment.
20	$\overline{LPBK1}$	I	**LOOPBACK 1.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions. An active low signal that will cause the transmitted signal to be looped back to the receive circuit before the twisted pair drivers and receivers. The twisted pair medium will be removed from the circuit.
21	Reserved	—	This pin is reserved; it should be left floating.
22	Reserved	—	This pin is reserved; it should be left floating.
23	V_{SS}	—	**GROUND**
24	RESET	I	**RESET.** Active high input asserted to bring the device into a known state. Must be asserted for 1 ms while the clock is running.
25	LI	O	**LINK INTEGRITY.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions. An active high output used to indicate the presence of link integrity faults.
26	DTE	I	**DATA TERMINAL EQUIPMENT.** Not connected, reserved for future use. It will be used on 10BASE-T compliant versions. If not connected or strapped high, the future device will be in DTE mode. If strapped low the pin will be in repeater mode.
27	TD+	I	**TWISTED PAIR TRANSMIT DATA COMPLEMENT.** This pin transmits outgoing Manchester data to the twisted pair link segment. It is connected directly to the Medium Dependent Interface Connector (RJ-45) pin 1.
28	TD−	I	**TWISTED PAIR TRANSMIT DATA COMPLEMENT.** This pin transmits outgoing Manchester data to the twisted pair link segment. It is connected directly to the Medium Dependent Interface Connector (RJ-45) pin 2.
29	RD+	I	**TWISTED PAIR RECEIVE DATA.** This pin receives incoming Manchester data from the twisted pair link segment. It is connected directly to the Medium Dependent Interface Connector (RJ-45) pin 3.
30	RD−	I	**TWISTED PAIR RECEIVE DATA COMPLEMENT.** This pin receives incoming Manchester data from the twisted pair link segment. It is connected directly to the Medium Dependent Interface Connector (RJ-45) pin 6.
31	V_{SS}	—	**GROUND**
32, 33	V_{DD}	—	**V_{DD}.** A +12-V ±10% power supply. Not required for this device, but may be required for future versions. Intel recommends connecting this power supply.
34	$\overline{CDT}$	O	**COLLISION DETECT.** An Active low signal which indicates the presence of a collision to the controller.
35, 36	V_{CC}	—	**V_{CC}:** A 5-V ±10% power supply.

FUNCTIONAL DESCRIPTION

Overview

The 82521TA provides the functions required for operating Data Terminal Equipment on a 10-Mb/s, CSMA/CD Local Area Network that uses standard telephone building wiring. These networks fully comply with the ANSI/IEEE 802.3-1985 standard (Ethernet) at the Physical layer and at the Medium Access Control sublayer (MAC) of the Data Link layer—and they can integrate with existing LANs. The 82521TA has been designed in parallel with the ongoing work of the IEEE 802.3 10BASE-T Task Force.

CLOCK GENERATION

The 82521TA supports both internal and external sources for the precision clock (20 MHz ±0.01%) required for operation in an Ethernet environment. The clock is used to retime the transmitted Manchester data, to generate the 10-MHz $\overline{TxC}$ signal, and to provide a precise reference for Manchester decoding and clock recovery of received data.

If ICLK is strapped to ECLK, an on-board clock oscillator generates the precision clock. This clock can be used for synchronous operation of circuits on the host board; however, care must be taken to minimize the load on the clock. Synchronous operation of the supercomponent and the baseboard can be achieved by providing ECLK with a 20-MHz ±0.01% clock with TTL levels and a duty cycle of 40/60 or better.

Transmit Section

The transmit section of the 82521TA is controlled by the $\overline{RTS}$ signal generated by the Ethernet LAN controller; e.g., Intel's 82586 or 82592. When $\overline{RTS}$ asserts, the 82521TA begins clocking in Manchester data from the controller over the TXD input. The TXD level is sampled on every transition of the 10-MHz TXC signal. The serial data is then retimed by the precision 20-MHz clock and sent to the twisted pair line drivers.

The line drivers begin transmitting the serial Manchester bit stream—two bit times after $\overline{RTS}$ is asserted. The line drivers use a predistortion algorithm to improve jitter performance on the twisted pair. The line drivers reduce their drive level during the second half of "fat" (100 ns) Manchester pulses, and maintain a full drive level during all "thin" (50 ns) pulses. This reduces line overcharging during "fat" pulses, a major source of jitter. Figure 1 shows the differences between the familiar coax cable waveform and the predistorted waveform generated by the 82521TA. The line drivers maintain a characteristic impedance of 96Ω (typical) throughout transmission of data packets.

The predistorted line driver output is then passed through the transmit EMI filter to reduce the high-frequency harmonics of the transmitted signal. This reduces noise, near-end crosstalk in bundled twisted pairs, and unwanted radio frequency (RF) interference. The filter maintains the characteristic 96Ω (typical) impedance. The filtered signal then passes through an isolation transformer and a common-mode choke. These provide high-voltage protection, dc isolation, and common-mode noise rejection. The output of the common-mode choke is directly connected to the TD+ and TD− pair of output pins. These pins can be directly connected to pins 1 and 2 of an RJ-45 connector.

Receive Section

The receive section of the 82521TA processes incoming Manchester data from the twisted pair link segment, converts it to NRZ data, and recovers the embedded clock. It contains a squelch circuit that distinguishes noise from incoming data. Valid data passes through the 82521s' input protection and common-mode rejection circuitry, and then receive EMI filter, then it trips the squelch circuit. The twisted pair line receiver is then enabled and converts the signal to digital voltage levels.

The signal passes to the Manchester decoder and clock recovery circuit. Within two bit times after the data packet arrives, $\overline{RxC}$ changes from its free running state to its locked state. The $\overline{CRS}$ signal will assert after $\overline{RxC}$ acquires lock to prevent any problems with the $\overline{RxC}$ frequency/phase change. The decoded NRZ data is sent to the LAN controller on the RxD line along with the recovered clock signal $\overline{RxC}$.

The 82521TA detects the IDL signal at the end of a packet. After three bit times, $\overline{CRS}$ will be synchronously deasserted with $\overline{RxC}$, then $\overline{RxC}$ returns to its free running state.

Collision Detection

Collision detection in the twisted pair environment is indicated by simultaneous transmission and reception on the twisted pair link segment. The $\overline{CDT}$ signal is asserted for the duration of both $\overline{RTS}$ and the presence of received data. $\overline{CRS}$ is asserted for the duration of either $\overline{RTS}$ or the presence of received data.

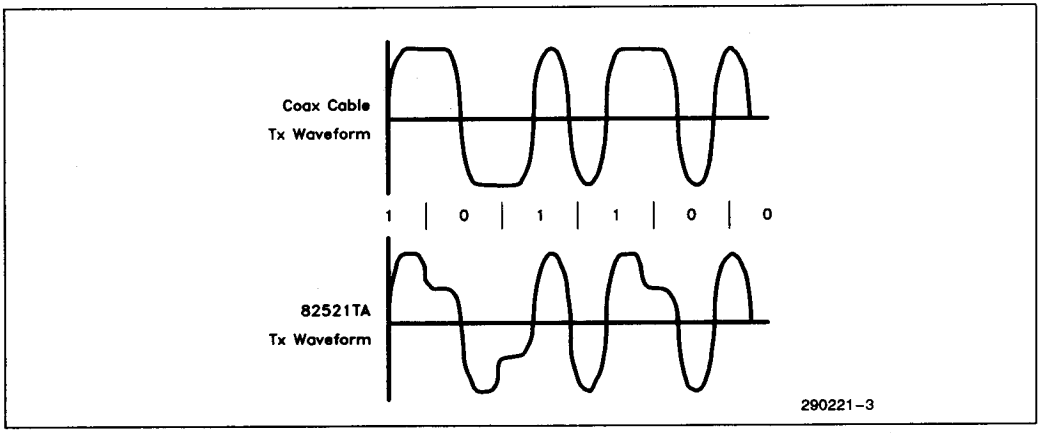


Figure 1. Effects of Predistortion

A.C. CHARACTERISTICS

D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.6	V	—
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.5	V	—
V_{OL}	Output Low Voltage	—	0.5	V	I_{OL} = 25 mA
V_{OH}	Output High Voltage	3.5	—	V	I_{OH} = −10 μA
I_{CC}	Power Supply Current	—	400	mA	V_{CC} = 5.0V
I_{LI}	Input Leakage Current	—	10	μA	V_{IH} = 5.5V
PD	Power Dissipation	—	2	W	V_{CC} = 5.0V
tr tf	Output Rise and Fall Time	—	5 5	ns ns	C_{LOAD} = 20 pF C_{LOAD} = 20 pF

ANALOG CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} ±10%

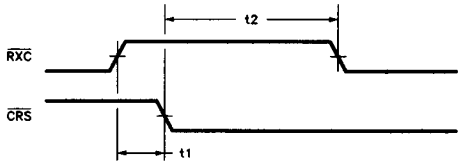
Symbol	Parameter	Min	Max	Units
Zo	Characteristic Impedance (I/O) Return Loss (5 MHz–10 MHz) Squelch Reject Level Squelch Accept Level Common Mode Rejection	77 15 450 TBD	115 300 	Ω dB mV mV mV
Vodf1	Output Differential Voltage (before distortion)	2.2	2.8	V
Vodf2	Output Differential Voltage (after distortion)	700	1500	mV
Vodf3	Output Differential Voltage (40-bit times after transmission)	±50		mV
	Maximum Signal Undershoot		2.8	V
	Transmitter Impedance Balance (@ 10 MHz)	29		dB
Vocm	Output Common Mode Voltage (> 30 kHz)		50	mV

DECODER TIMING CHARACTERISTICS

(Measurements are from 50% points, unless otherwise noted)

Symbol	Parameter	Min	Max	Units
t1	$\overline{RxC}$ High to $\overline{CRS}$ Asserted	3	19	ns
t2	$\overline{CRS}$ Asserted to $\overline{RxC}$ Low	17	40	ns
t3	$\overline{RxC}$ High to $\overline{CRS}$ Deasserted	3	19	ns
t4	$\overline{CRS}$ Deasserted to $\overline{RxC}$ Low	20	65	ns
t5	$\overline{CRS}$ Deasserted to $\overline{RxC}$ High	195	345	ns
t6	$\overline{RxC}$ High Pulse Width as Captured Data Clock	36	45	ns
t7	$\overline{RxC}$ Low Pulse Width as Captured Data Clock	38	80	ns
t8	$\overline{RxC}$ Period as Captured Data Clock	78	124	ns
t9	$\overline{RxC}$ High Pulse Width as Free Oscillating Clock	43	73	ns
t10	$\overline{RxC}$ Low Pulse Width as Free Oscillating Clock	172	276	ns
t11	$\overline{RxC}$ Period as Free Oscillating Clock	215	349	ns
t12	$\overline{RxD}$ Transition to $\overline{RxC}$ High	−5	5	ns
t13	$\overline{RxC}$ Low to $\overline{RxD}$ Transition	30	85	ns
t14	$\overline{RxD}$ Transition to $\overline{RxC}$ Low	30	50	ns
t15	RD Pair Midbit Transition to $\overline{RxC}$ Low	86	160	ns
t16	RD Pair Preamble Transition to $\overline{CRS}$ Asserted	53	150	ns
t17	Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 0) Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 1)	230 280	370 440	ns ns
t18	Midbit to Midbit Transition on RD Pair	80	120	ns
t19	Boundary to Midbit Transition on RD Pair	30	70	ns

Negative-Transition $\overline{CRS}$ Timing Relative to $\overline{RxC}$



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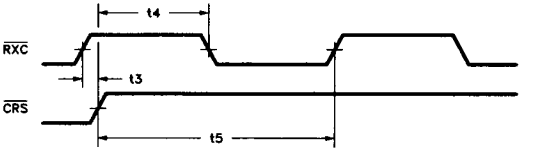
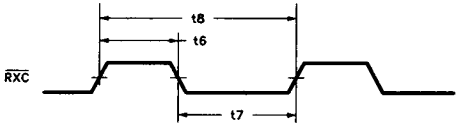
DTE Positive-Transition $\overline{CRS}$ Timing Relative to $\overline{RxC}$



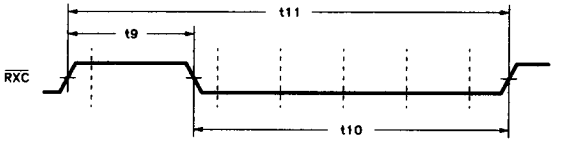
290221-5

$\overline{RxC}$ Timing Measurements (Captured Data Clock)



290221-6

$\overline{RxC}$ Timing Measurements (Free Oscillating Clock)



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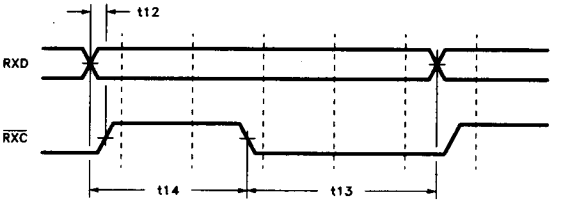
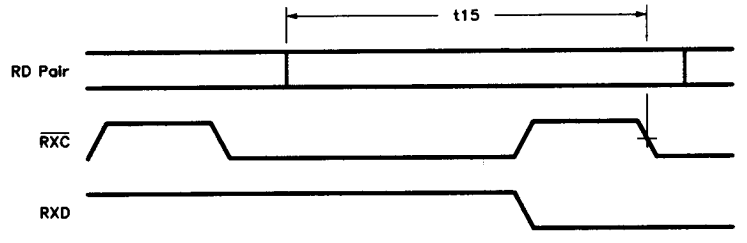
RxD Timing Relative to $\overline{RxC}$



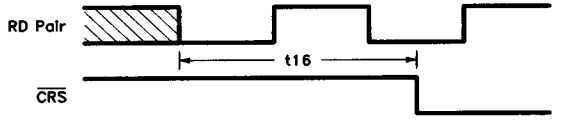
290221-8

Latency-Definition Timing Measurements



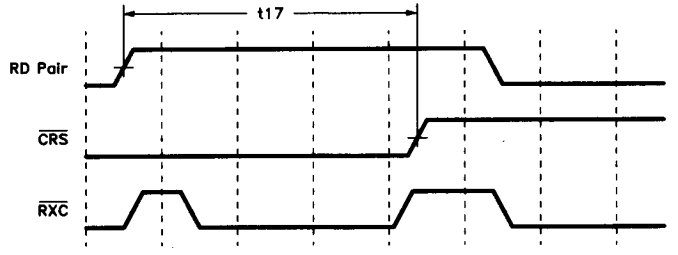
290221-9

Start of Packet Delay



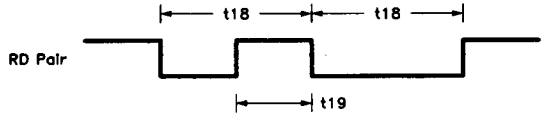
290221-10

End-of-Normal-Packet Timing Measurements



290221-11

Input Jitter



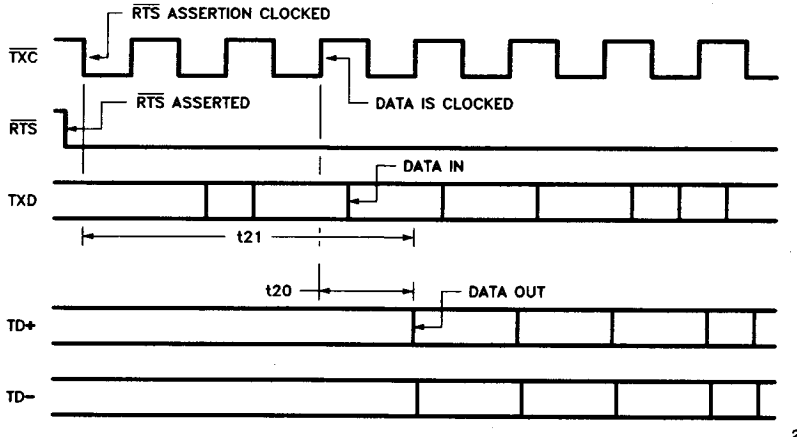
290221-12

Encoder Timing Characteristics

Measurements are from 50% points, unless otherwise noted. The input duty cycle requirement for CLK is 60%/40%.

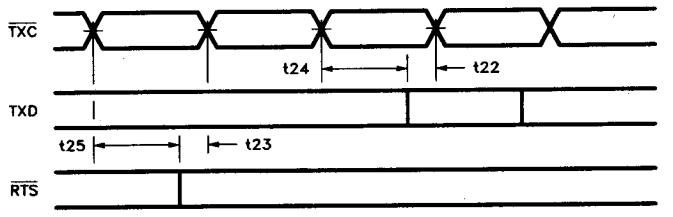
Symbol	Parameter	Min	Max	Units
t20	Data Clocked to TxD to Data at Output TP Pair (Latency)	100	220	ns
t21	$\overline{RTS}$ Assertion Clocked to TP Pair Enabled	340	470	ns
t22	TxD Setup Time with Respect to $\overline{TxC}$ Transition	10	—	ns
t23	$\overline{RTS}$ Setup Time with Respect to $\overline{TxC}$ Transition	10	—	ns
t24	TxD Hold Time with Respect to $\overline{TxC}$ Transition	0	—	ns
t25	$\overline{RTS}$ Hold Time with Respect to $\overline{TxC}$ Transition	0	—	ns
t26	$\overline{RTS}$ Deassertion Clocked to TP Pair Disabled	340	470	ns
OUTPUT CHARACTERISTICS				
t27	Maximum Deviation from the Ideal 50 ns Strobe Point for TP Pair	—	2.5	ns
t28–t29	TP Pair Worst Case Duty Cycle Mismatch, 10 pF Load	−5	5	ns
t30	$\overline{TxC}$ High Time	40	60	ns
t31	$\overline{TxC}$ Low Time	40	60	ns

Start-of-Packet



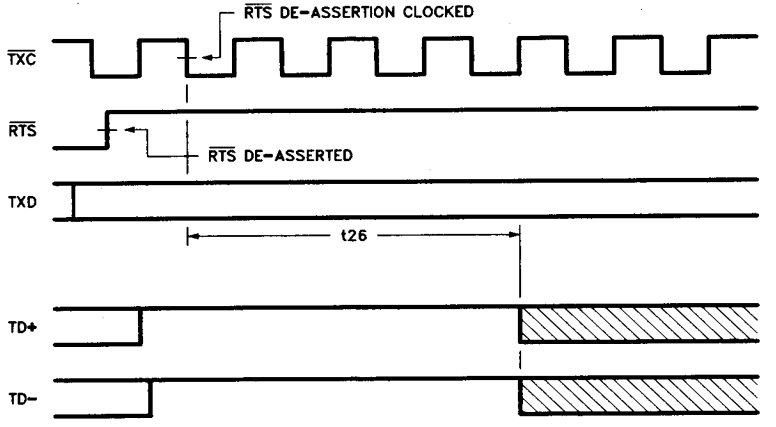
290221-13

TxD and $\overline{RTS}$ Setup Time



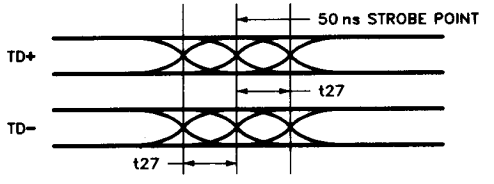
290221-14

End-of-Packet



290221-15

Maximum Deviation from Ideal 50 ns Strobe Point



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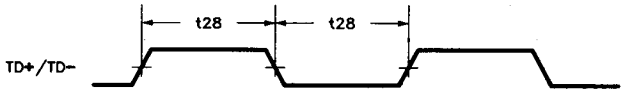
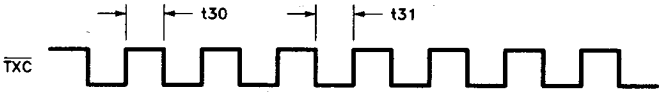
Worst-Case Duty Cycle Mismatch



290221-17

$\overline{\text{TxC}}$ Pulse Width



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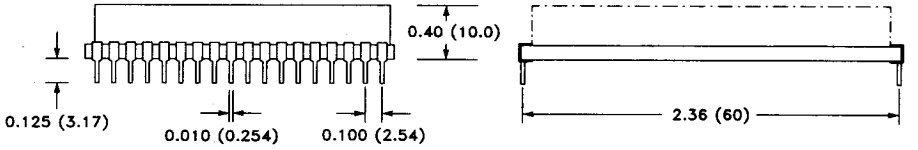
82521TA Form Factor



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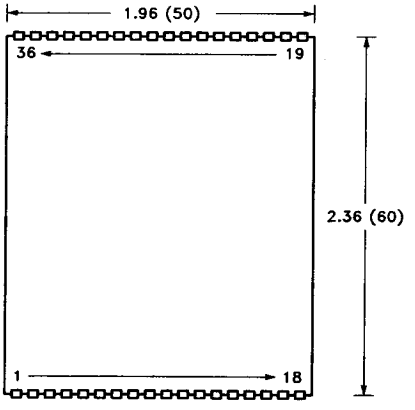

290221-19