

1.0 MoBL-USB TX2[™] Features

- UTMI-compliant/USB-2.0-certified for device operation
- Operates in both USB 2.0 high-speed (HS), 480 Mbits/second, and full-speed (FS), 12 Mbits/second
- Optimized for seamless interface with Intel[®] Monahans Applications Processors
- · Serial-to-parallel and parallel-to-serial conversions
- 8-bit unidirectional, 8-bit bidirectional, or 16-bit bidirectional external data interface
- Synchronous field and EOP detection on receive packets
- Synchronous field and EOP generation on transmit packets
- Data and clock recovery from the USB serial stream
- · Bit stuffing/unstuffing; bit stuff error detection
- Staging register to manage data rate variation due to bit stuffing/unstuffing
- 16-bit 30-MHz, and 8-bit 60-MHz parallel interface
- Ability to switch between FS and HS terminations and signaling
- · Supports detection of USB reset, suspend, and resume
- Supports HS identification and detection as defined by the USB 2.0 Specification

- Supports transmission of resume signaling
- 3.3V operation
- Two package options—56-pin QFN and 56-pin VFBGA
- All required terminations, including 1.5-Kohm pull-up on DPLUS, are internal to chip
- Supports USB 2.0 test modes

The Cypress MoBL-USB TX2™ is a Universal Serial Bus transceiver. (USB) specification revision 2.0 serial/deserializer, to a parallel interface of either 16 bits at 30 MHz or eight bits at 60 MHz. The MoBL-USB TX2 provides a high-speed physical layer interface that operates at the maximum allowable USB 2.0 bandwidth. This allows the system designer to keep the complex high-speed analog USB components external to the digital ASIC which decreases development time and associated risk. A standard interface is provided that is USB 2.0-certified and is compliant with Transceiver Macrocell Interface (UTMI) specification version 1.05 dated 3/29/01.

This product is also optimized to seamlessly interface with Monahans -P & -L applications processors. It has been characterized by Intel and is recommended as the USB 2.0 UTMI transceiver of choice for its Monahans processors.

Two packages are defined for the family: 56-pin QFN and 56-pin VFBGA.

The functional block diagram is shown in Figure 1-1.



Figure 1-1. Block Diagram



ADVANCE INFORMATION

2.0 Applications

Mobile Applications

- Smart Phones
- PDA Phones
- Gaming Phones
- Portable Media Players (PMP)
- GPS Tracking Devices

Consumer Applications

- Cameras
- Scanners
- MP3 players
- DSL Modems
- Memory Card Readers

Non-Consumer Applications

- Networking
- Wireless LAN
- Home PNA
- DataBus16_8 Reserved Uni_bidi TXValid ValidH V_{cc} GND CLK V CC D2 D3 **P**4 В Ó 56 55 TXReady GND 42 О Suspend D5 41 Reset Reserved 40 3 AV_{CC} 4 D6 39 **XTALOUT** D7 38 5 **XTALIN** D8 6 37 CY7C68000A AGND D9 7 36 56-pin QFN Reserved AV_{CC} 8 35 DPLUS 9 34 D10 D11 DMINUS 10 33 AGND 11 32 V_{CC} D12 XcvrSelect 31 12 TermSelect GND 13 30 29 D13 OpMode0 14 24 25 6 OpMode1 V_{CC} RXValid D15 GND V_{CC} D14 Reserved RXActive Reserved LineState0 LineState RXError



3.0 Pin Assignments





Figure 3-2. 56-pin VFBGA Pin Assignments

4.0 Ordering Information

Table 4-1. Ordering Information

Ordering Code	Package Type
CY7C68000A-56LFXC	56 QFN
CY7C68000A-56BAXC	56 VFBGA
CY3683	MoBL-USB TX2 Development Board

Contact your Cypress sales representative for detailed data sheet and additional information.

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Document History Page

Document Title: CY7C68000A MoBL-USB TX2™ USB 2.0 UTMI Transceiver Advance Information Document Number: 001-07074				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	430244	See ECN	TEH	New data sheet