

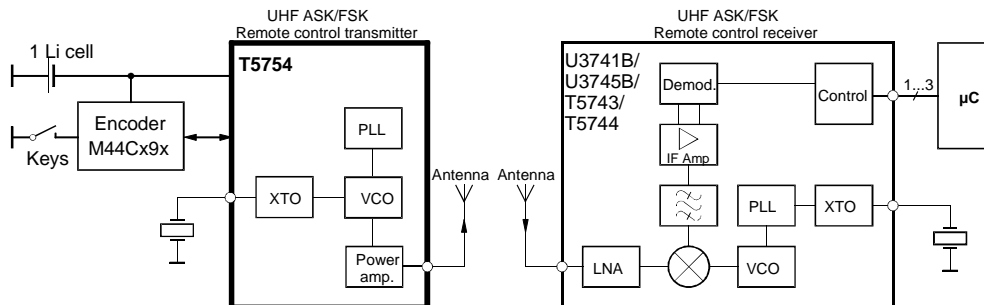
Features

- Integrated PLL Loop Filter
- ESD Protection (4 kV HBM/ 200 V MM; Except Pin 2: 4 kV HBM/ 100 V MM) also at ANT1/ANT2
- High Output Power (7.5 dBm) with Low Supply Current (9.0 mA)
- Modulation Scheme ASK/ FSK
 - FSK Modulation is Achieved by Connecting an Additional Capacitor Between the XTAL Load Capacitor and the Open Drain Output of the Modulating Microcontroller
- Easy to Design-in Due to Excellent Isolation of the PLL from the PA and Power Supply
- Single Li-cell for Power Supply
- Supply Voltage 2.0 V to 4.0 V in the Temperature Range of -40°C to 85°C/125°C
- Package TSSOP8L
- Single-ended Antenna Output with High Efficient Power Amplifier
- CLK Output for Clocking the Microcontroller
- One-chip Solution with Minimum External Circuitry
- 125°C Operation for Tire Pressure Systems

Description

The T5754 is a PLL transmitter IC which has been developed for the demands of RF low-cost transmission systems at data rates up to 32 kBaud. The transmitting frequency range is 429 MHz to 439 MHz. It can be used in both FSK and ASK systems.

Figure 1. System Block Diagram



UHF ASK/FSK Transmitter

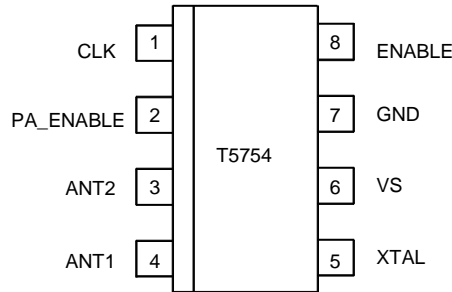
T5754

Preliminary



Pin Configuration

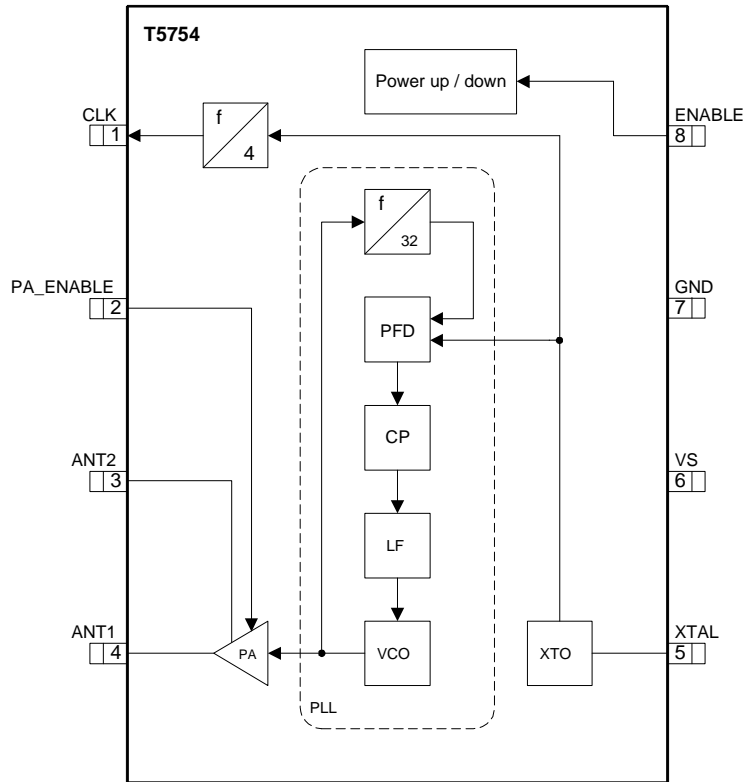
Figure 2. Pinning TSSOP8L



Pin Description

| Pin | Symbol | Function | Configuration |
|-----|-----------|---|---|
| 1 | CLK | Clock output signal for microcontroller The clock output frequency is set by the crystal to $f_{XTAL} / 4$ | |
| 2 | PA_ENABLE | Switches on power amplifier, used for ASK modulation | |
| 3 | ANT2 | Emitter of antenna output stage | |
| 4 | ANT1 | Open collector antenna output | |
| 5 | XTAL | Connection for crystal | |
| 6 | VS | Supply voltage | See ESD protection circuitry (see Figure 8) |
| 7 | GND | Ground | See ESD protection circuitry (see Figure 8) |
| 8 | ENABLE | Enable input | |

Figure 3. Block Diagram



General Description

This fully integrated PLL transmitter allows particularly simple, low-cost RF miniature transmitters to be assembled. The VCO is locked to $32 f_{XTAL}$ hence a 13.56 MHz crystal is needed for a 433.92 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL needs typically <1 ms until the PLL is locked and the CLK output is stable. There is a wait time of ≥ 1 ms until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance. The delivered output power is hence controllable via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50Ω . A high power efficiency of $\eta = P_{out}/(I_{S,PA} V_S)$ of 36% for the power amplifier results when an optimized load impedance of $Z_{Load} = (166 + j223) \Omega$ is used at 3 V supply voltage.

Functional Description

If ENABLE = L and the PA_ENABLE = L, the circuit is in standby mode consuming only a very small amount of current so that a lithium cell used as power supply can work for several years.

With ENABLE = H the XTO, PLL and the CLK driver are switched on. If PA_ENABLE remains L only the PLL and the XTO is running and the CLK signal is delivered to the microcontroller. The VCO locks to 32 times the XTO frequency.

With ENABLE = H and PA_ENABLE = H the PLL, XTO, CLK driver and the power amplifier are on. With PA_ENABLE the power amplifier can be switched on and off, which is used to perform the ASK modulation.

ASK Transmission

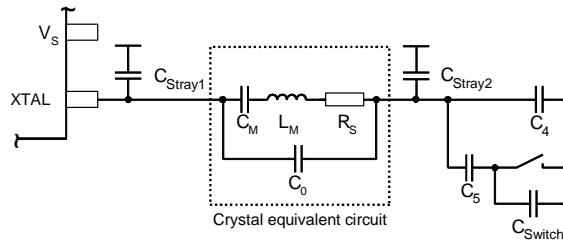
The T5754 is activated by ENABLE = H. PA_ENABLE must remain L for $t \geq 1$ ms, then the CLK signal can be taken to clock the microcontroller and the output power can be modulated by means of Pin PA_ENABLE. After transmission PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The T5754 is switched back to standby mode with ENABLE = L.

FSK Transmission

The T5754 is activated by ENABLE = H. PA_ENABLE must remain L for $t \geq 1$ ms, then the CLK signal can be taken to clock the microcontroller and the power amplifier is switched on with PA_ENABLE = H. The chip is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The T5754 is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about $\pm 25\%$ when the following tolerances are considered.

Figure 4. Tolerances of Frequency Modulation



Using $C_4 = 9.2 \text{ pF} \pm 2\%$, $C_5 = 6.8 \text{ pF} \pm 5\%$, a switch port with $C_{S_{\text{witch}}} = 3 \text{ pF} \pm 10\%$, stray capacitances on each side of the crystal of $C_{\text{Stray1}} = C_{\text{Stray2}} = 1 \text{ pF} \pm 10\%$, a parallel capacitance of the crystal of $C_0 = 3.2 \text{ pF} \pm 10\%$ and a crystal with $C_M = 13 \text{ fF} \pm 10\%$, an FSK deviation of $\pm 21 \text{ kHz}$ typical with worst case tolerances of $\pm 16.3 \text{ kHz}$ to $\pm 28.8 \text{ kHz}$ results.

CLK Output

An output CLK signal is provided for a connected microcontroller, the delivered signal is CMOS compatible if the load capacitance is lower than 10 pF.

Clock Pulse Take-over

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel's M4xCx9x has the special feature of starting with an integrated RC-oscillator to switch on the T5754 with ENABLE = H, and after 1 ms to assume the clock signal of the transmission IC, so that the message can be sent with crystal accuracy.

Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load,opt} = (166 + j223) \Omega$. There must be a low resistive path to V_S to deliver the DC current.

The delivered current pulse of the power amplifier is 9 mA and the maximum output power is delivered to a resistive load of 465Ω if the 1.0 pF output capacitance of the power amplifier is compensated by the load impedance.

An optimum load impedance of:

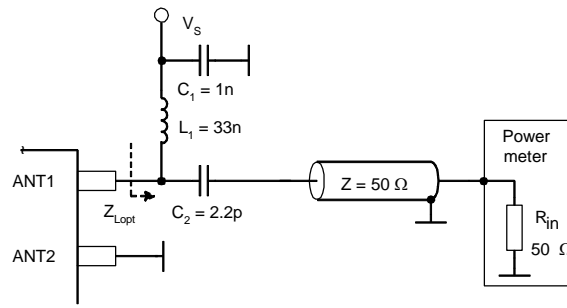
$Z_{Load} = 465 \Omega \parallel j/(2 \times \pi \times 1.0 \text{ pF}) = (166 + j223) \Omega$ thus results for the maximum output power of 7.5 dBm.

The load impedance is defined as the impedance seen from the T5754's ANT1, ANT2 into the matching network. Do not confuse this large signal load impedance with a small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for a power amplifier.

Less output power is achieved by lowering the real parallel part of 465Ω where the parallel imaginary part should be kept constant.

Output power measurement can be done with the circuit of Figure 5. Note that the component values must be changed to compensate the individual board parasitics until the T5754 has the right load impedance $Z_{Load,opt} = (166 + j223) \Omega$. Also the damping of the cable used to measure the output power must be calibrated out.

Figure 5. Output Power Measurement



Application Circuit

For the supply-voltage blocking capacitor C_3 a value of 68 nF/X7R is recommended (see Figure 6 and Figure 7). C_1 and C_2 are used to match the loop antenna to the power amplifier where C_1 typically is 8.2 pF/NP0 and C_2 is 6 pF/NP0 (10 pF + 15 pF in series); for C_2 two capacitors in series should be used to achieve a better tolerance value and to have the possibility to realize the $Z_{Load,opt}$ by using standard valued capacitors.

C_1 forms together with the pins of T5754 and the PCB board wires a series resonance loop that suppresses the 1st harmonic, hence the position of C_1 on the PCB is important. Normally the best suppression is achieved when C_1 is placed as close as possible to the Pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

L_1 ([50 nH to 100 nH) can be printed on PCB. C_4 should be selected that the XTO runs on the load resonance frequency of the crystal. Normally, a value of 12 pF results for a 15 pF load-capacitance crystal.

Figure 6. ASK Application Circuit

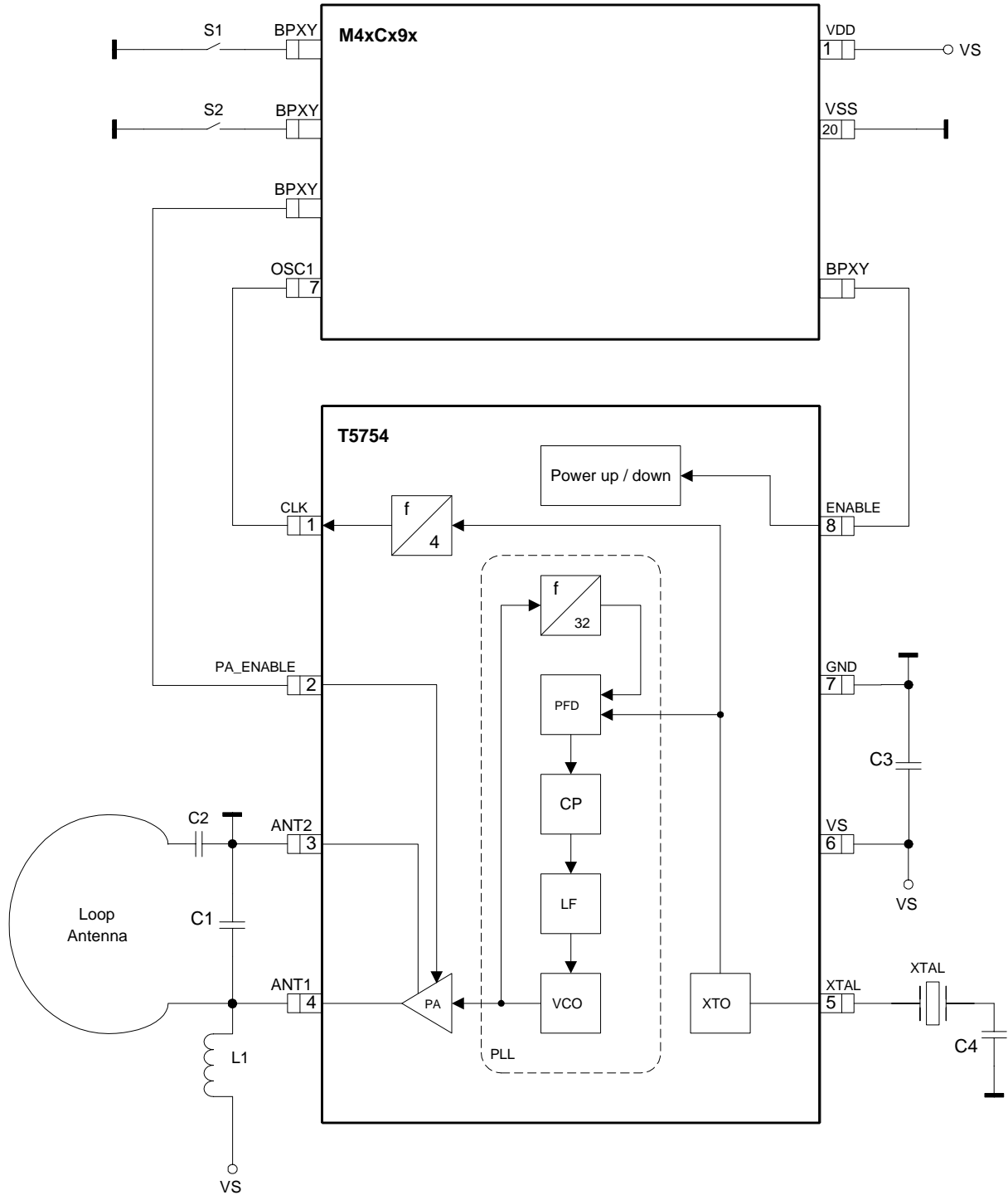


Figure 7. FSK Application Circuit

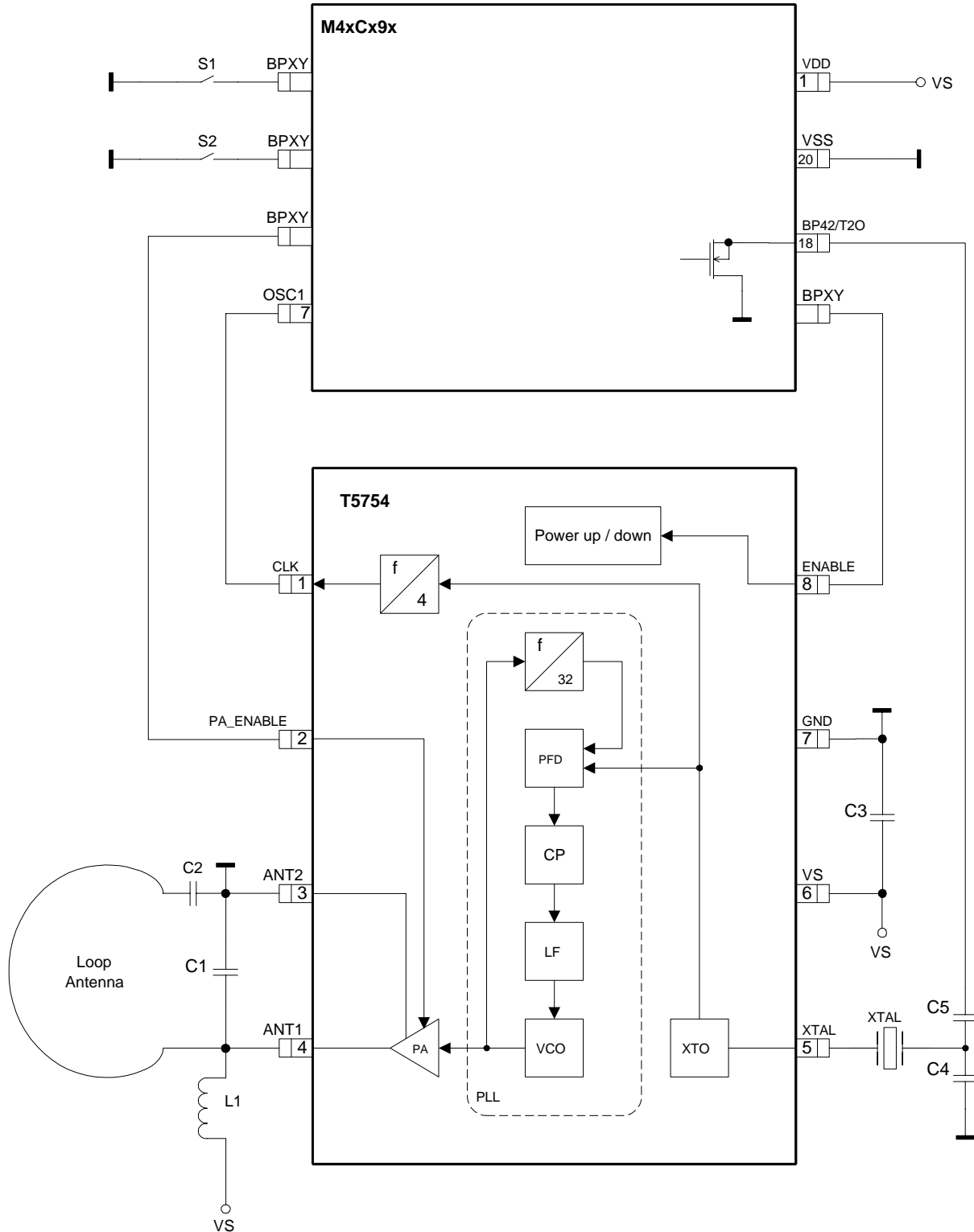
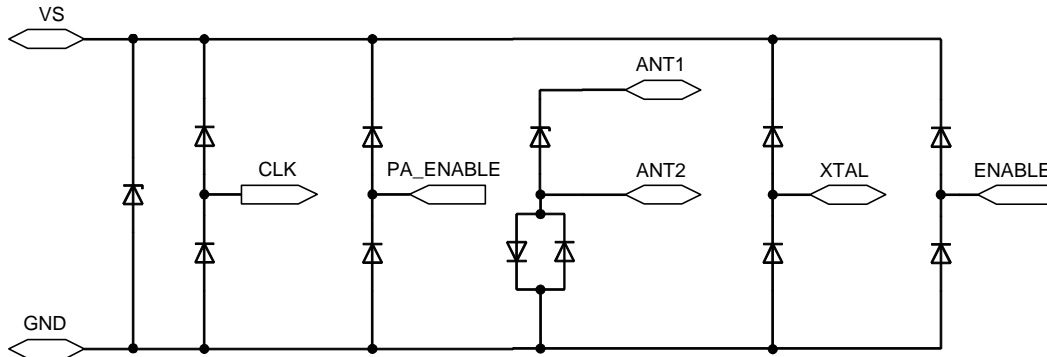


Figure 8. ESD Protection Circuit



Absolute Maximum Ratings

| Parameters | Symbol | Minimum | Maximum | Unit |
|----------------------|-----------|---------|---------|------|
| Supply voltage | V_S | | 5 | V |
| Power dissipation | P_{tot} | | 100 | mW |
| Junction temperature | T_j | | 150 | °C |
| Storage temperature | T_{stg} | -55 | 125 | °C |
| Ambient temperature | T_{amb} | -55 | 125 | °C |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|------------------|------------|-------|------|
| Junction ambient | R_{thJA} | 170 | K/W |

Electrical Characteristics

$V_S = 2.0\text{ V to }4.0\text{ V}$, $T_{amb} = -40^\circ\text{C to }125^\circ\text{C}$ unless otherwise specified.

Typical values are given at $V_S = 3.0\text{ V}$ and $T_{amb} = 25^\circ\text{C}$. All parameters are referred to GND (Pin 7).

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|----------------|---|-------------------|------|------|----------|---------------------------|
| Supply current | Power down, $V_{ENABLE} < 0.25\text{ V}$, $-40^\circ\text{C to }85^\circ\text{C}$ $V_{PA-ENABLE} < 0.25\text{ V}$, $-85^\circ\text{C to }+125^\circ\text{C}$ $V_{PA-ENABLE} < 0.25\text{ V}$, 25°C (100% correlation tested) | I_{S_Off} | | <10 | 350 7 | nA μA nA |
| Supply current | Power up, PA off, $V_S = 3\text{ V}$, $V_{ENABLE} > 1.7\text{ V}$, $V_{PA-ENABLE} < 0.25\text{ V}$ | I_S | | 3.7 | 4.8 | mA |
| Supply current | Power up, $V_S = 3.0\text{ V}$, $V_{ENABLE} > 1.7\text{ V}$, $V_{PA-ENABLE} > 1.7\text{ V}$ | $I_{S_Transmit}$ | | 9 | 11.6 | mA |
| Output power | $V_S = 3.0\text{ V}$, $T_{amb} = 25^\circ\text{C}$, $f = 433.92\text{ MHz}$, $Z_{Load} = (166 + j233)\ \Omega$ | P_{Ref} | 5.5 | 7.5 | 10 | dBm |

Electrical Characteristics (Continued)

$V_S = 2.0\text{ V to }4.0\text{ V}$, $T_{\text{amb}} = -40^\circ\text{C to }125^\circ\text{C}$ unless otherwise specified.

Typical values are given at $V_S = 3.0\text{ V}$ and $T_{\text{amb}} = 25^\circ\text{C}$. All parameters are referred to GND (Pin 7).

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--|---|--|------------------|-------------------|------------------|-------------------------|
| Output power variation for the full temperature range | $T_{\text{amb}} = -40^\circ\text{C to }+85^\circ\text{C}$, $V_S = 3.0\text{ V}$ $V_S = 2.0\text{ V}$ | ΔP_{Ref} ΔP_{Ref} | | | -1.5 -4.0 | dB dB |
| Output power variation for the full temperature range | $T_{\text{amb}} = -40^\circ\text{C to }+125^\circ\text{C}$, $V_S = 3.0\text{ V}$ $V_S = 2.0\text{ V}$, $P_{\text{Out}} = P_{\text{Ref}} + \Delta P_{\text{Ref}}$ | ΔP_{Ref} ΔP_{Ref} | | | -2.0 -4.5 | dB dB |
| Achievable output-power range | Selectable by load impedance | $P_{\text{Out_typ}}$ | 0 | | 7.5 | dBm |
| Spurious emission | $f_{\text{CLK}} = f_0/128$ Load capacitance at Pin CLK = 10 pF $f_0 \pm 1 \times f_{\text{CLK}}$ $f_0 \pm 4 \times f_{\text{CLK}}$ other spurious are lower | | | -55 -52 | | dBc dBc |
| Oscillator frequency XTO (= phase comparator frequency) | $f_{\text{XTO}} = f_0/32$ f_{XTAL} = resonant frequency of the XTAL, $C_M \leq 10\text{ fF}$, load capacitance selected accordingly $T_{\text{amb}} = -40^\circ\text{C to }+85^\circ\text{C}$, $T_{\text{amb}} = -40^\circ\text{C to }+125^\circ\text{C}$ | f_{XTO} | -30 -40 | f_{XTAL} | +30 +40 | ppm ppm |
| PLL loop bandwidth | | | | 250 | | kHz |
| Phase noise of phase comparator | Referred to $f_{\text{PC}} = f_{\text{XTO}}$, 25 kHz distance to carrier | | | -116 | -110 | dBc/Hz |
| In loop phase noise PLL | 25 kHz distance to carrier | | | -86 | -80 | dBc/Hz |
| Phase noise VCO | at 1 MHz at 36 MHz | | | -94 -125 | -90 -121 | dBc/Hz dBc/Hz |
| Frequency range of VCO | | f_{VCO} | 429 | | 439 | MHz |
| Clock output frequency (CMOS microcontroller compatible) | | | | $f_0/128$ | | MHz |
| Voltage swing at Pin CLK | $C_{\text{Load}} \leq 10\text{ pF}$ | V_{0h} V_{0l} | $V_S \times 0.8$ | | $V_S \times 0.2$ | V V |
| Series resonance R of the crystal | | R_s | | | 110 | Ω |
| Capacitive load at Pin XTO | | | | | 7 | pF |
| FSK modulation frequency rate | Duty cycle of the modulation signal = 50% | | 0 | | 32 | kHz |
| ASK modulation frequency rate | Duty cycle of the modulation signal = 50% | | 0 | | 32 | kHz |
| ENABLE input | Low level input voltage High level input voltage Input current high | V_{ll} V_{lh} I_{in} | 1.7 | | 0.25 20 | V V μA |
| PA_ENABLE input | Low level input voltage High level input voltage Input current high | V_{ll} V_{lh} I_{in} | 1.7 | | 0.25 5 | V V μA |

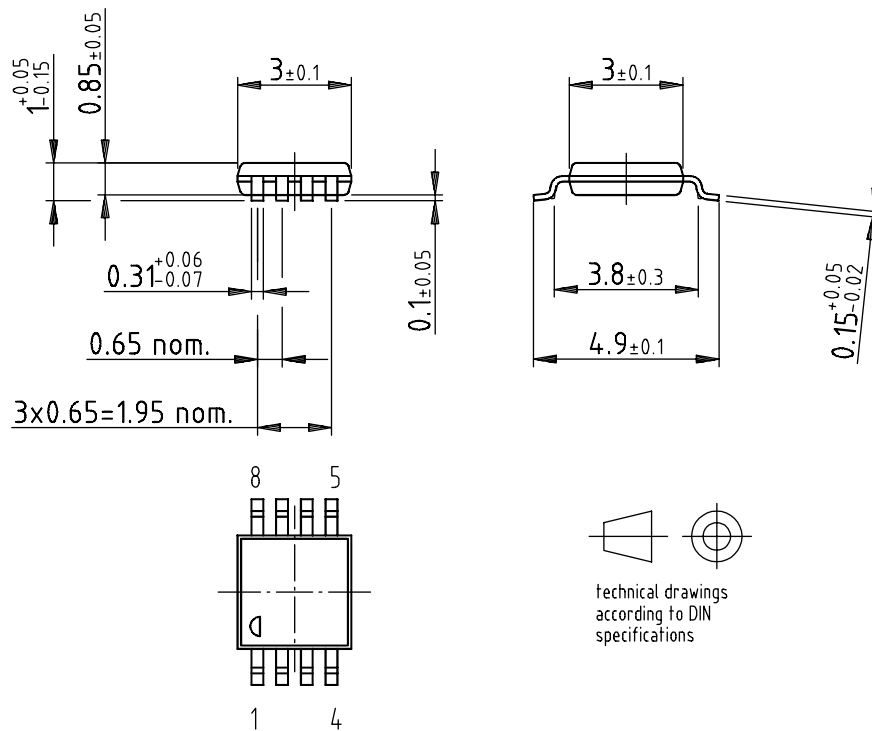
Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|---------|------------------|
| T5754-6AQ | TSSOP8L | Taped and reeled |

Package Information

Package: TSSOP 8L

Dimensions in mm



Drawing-No.: 6.543-5083.01-4

Issue: 1; 08.01.02



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

© Atmel Corporation 2002.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Atmel® is the registered trademark of Atmel.

Other terms and product names may be the trademarks of others.



Printed on recycled paper.