

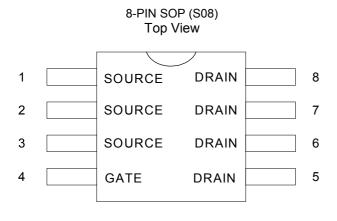
STRUCTURE

♦ Silicon N-channel MOSFET

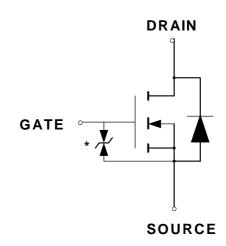
FEATURES

- ◆ Low Qg
- ◆ Low on-resistance
- ◆ Excellent resistance to damage from static electricity

PIN CONFIGURATION



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT4410	8-PIN SOP (S08)

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	30	V
Drain to Current − Continuous (at 25°C)	I _D	10	Α
- Pulsed*	I _{DP}	40	
Reverse Drain to Current − Continuous (at 25°C)	I _R	10	Α
Pulsed*	I _{DRP}	40	
Source Current (Body Diode) − Continuous (at 25°C)	Is	1.3	Α
Pulsed*	I _{SP}	5.2	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
Total Power Dissipation (T _C = 25°C)	P _D	2.0	W
Storage Temperature Range	T _{STG}	-55 to 150	$^{\circ}\!\mathbb{C}$
Channel Temperature	T _{ch}	150	$^{\circ}\!\mathbb{C}$

^{*} Pw≤10ms, Duty cycle≤1%

^{*} Gate Protection Diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use a protection circuit when the fixed voltage are exceeded.



THERMAL RESISTANCE (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth(ch-A)	62.5	°C /W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_a = 25^{\circ}C$.

			CMT4410			
Cha	aracteristic	Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V _{(BR)DSS}	30			V
$(V_{GS} = 0 \text{ V}, I_D = 1\text{mA})$						
Zero Gate Voltage Drain Current		I _{DSS}			10	μ A
$(V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V})$						
Gate-Source Leakage Current		I_{GSS}			±10	μ A
$(V_{gs} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage		$V_{GS(th)}$	1.0		2.5	V
$(V_{DS} = 10V, I_{D} = 1mA)$						
Static Drain-Source On-Resistance		R _{DS(on)}				mΩ
$(V_{GS} = 10 \text{ V}, I_D = 10\text{A})$	$(V_{GS} = 10 \text{ V}, I_D = 10\text{A})$			9	12	
$(V_{GS} = 4.5 \text{ V}, I_D = 10\text{A})$ $(V_{GS} = 4.0 \text{ V}, I_D = 10\text{A})$				13	18	
				15	20	
Forward Transfer Admittance (V _{DS} =	10V, I _D = 10A) *	Y _{FS}	10			mhos
Input Capacitance	0/ - 10 \/ f - 1MI -	C_{iss}		1750		pF
Output Capacitance	$V_{DS} = 10 \text{ V, } f = 1 \text{MHz,}$ $V_{GS} = 0 \text{ V)*}$	C_{oss}		950		pF
Reverse Transfer Capacitance		C_{rss}		450		pF
Turn-On Delay Time	0/ 45)/ 1 5 4	$t_{d(on)}$		20		ns
Rise Time	$(V_{DD} = 15 \text{ V}, I_D = 5 \text{ A},$ $V_{GS} = 10 \text{ V},$ $R_L = 3\Omega, R_{GS} = 10\Omega)$ *	t _r		55		ns
Turn-Off Delay Time		t _{d(off)}		100		ns
Fall Time		t _f		70		ns
Source-Drain Reverse Recovery	L 0.04 IV.II. 4000	t _{fr}		50	80	ns
Time **	$I_F = 2.3A$, di/dt = 100A/ μ s					
Total Gate Charge	0/ -45 // -40 A	Q_g		44.8	89.6	nC
Gate-Source Charge	$(V_{DD} = 15 \text{ V}, I_D = 10 \text{ A},$	Q_gs		5.9		nC
Gate-Drain Charge	rain Charge V _{GS} = 10 V)*			12.2	_	nC

^{*} Pulsed

BODY DIODE CHARACTERISTICS (SOURCE-DRAIN)

Unless otherwise specified, $T_a = 25^{\circ}C$.

				CMT4410		
Cha	racteristic	Symbol	Min	Тур	Max	Units
Forward Voltage		V_{SD}			1.5	V
$(V_{GS} = 0 \text{ V}, I_S = 5.2\text{A})^*$						
Reverse Recovery Time	$(V_{GS} = 0V, I_{DR} = 5.2 A,$	t _{rr}		240		ns
Reverse Recovery Charge	di/dt = 100A/µs)*	Q _{rr}		310		nC



TYPICAL ELECTRICAL CHARACTERISTICS

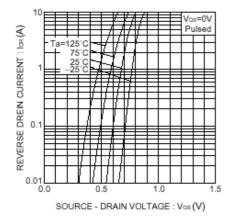


Fig.1 Reverse Drein Current vs. Source - Drain Voltage

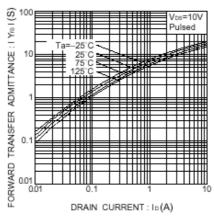


Fig.2 Forward Transfer Admittance vs. Drain Current

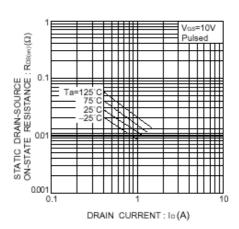


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (1)

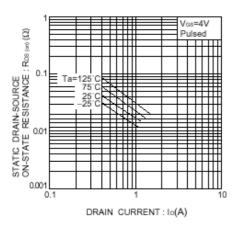


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (II)

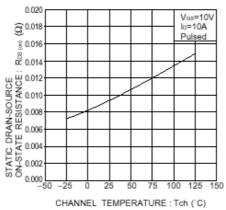


Fig.5 Static Drain-Source On-State Resistance vs. Channel Temperature

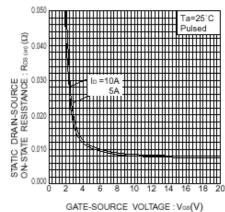


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

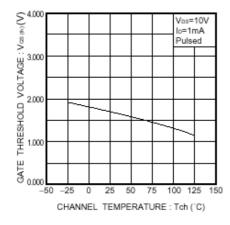


Fig.7 Gate Threshold Voltage vs. Channel Temperature

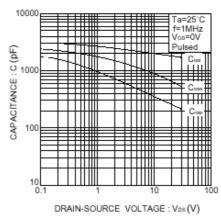


Fig.8 Typical Capacitance vs. Drain-Source Voltage

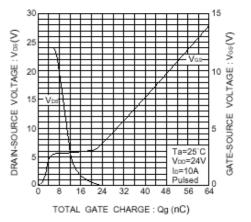
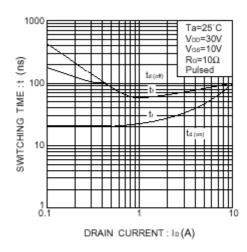


Fig.9 Dynamic Input Characteristics



TYPICAL ELECTRICAL CHARACTERISTICS (Conti.)



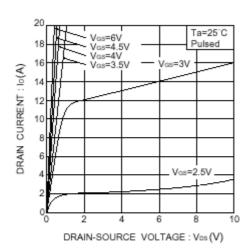


Fig.10 Switching Characteristics

Fig.11 Typical Output Characteristics

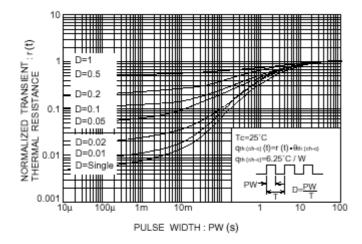
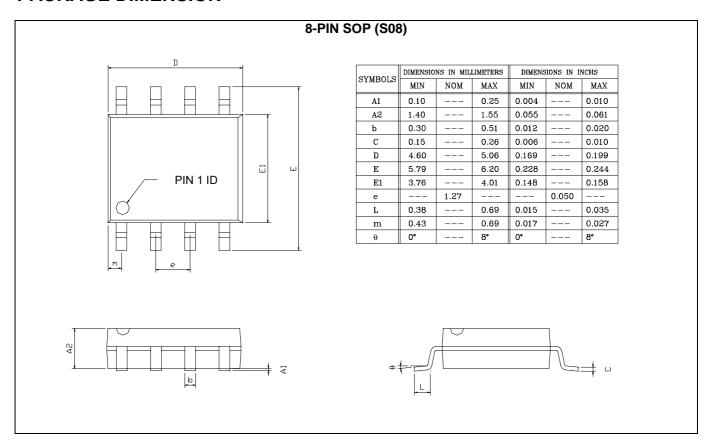


Fig.12 Normalized Transient Thermal Resistance vs. Pulse Width



PACKAGE DIMENSION





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