100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum and USB for Desktop PCs

Features

- **Mixed 2.5V and 3.3V operation**
- **Clock Generator for Pentium® II, and other similar processor-based motherboards**
  - **— Two 2.5V CPU clocks at 66.6 or 100 MHz**
  - **— Seven 3.3V synch. PCI clocks, one free-running**
  - **— Two 3.3V 48 MHz USB clocks**
  - **— One 3.3V REF clock at 14.318 MHz**
  - **— One 2.5V APIC clock at 14.318 MHz or PCI/2**
- **Spread spectrum clocking for EMI control (CY2282-11S only)**
- **Factory-EPROM programmable output drive and slew rate for EMI optimization**
- **Low skew outputs, ≤ 175 ps between CPU clocks**
- **Available in space-saving 28-pin SOIC package**

Functional Description

The CY2282 is a clock synthesizer/driver for a Pentium II, or other similar processor-based PC requiring 100-MHz support. The CY2282-1 outputs two CPU clocks at 2.5V. There are seven PCI clocks, running at one-half or one-third the CPU clock frequency of 66.6 MHz and 100 MHz respectively. One of the PCI clocks is free-running. Additionally, the part outputs two 3.3V USB clocks at 48 MHz, one 3.3V reference clock at 14.318 MHz, and one 2.5V APIC clock at 14.318 MHz.

The CY2282-11S provides the same outputs as the CY2282-1 but also incorporates the Intel®-defined spread spectrum features. It provides a 0.5% downspread on the CPU and PCI clocks, which can improve EMI in certain high-speed systems. A summary of clock outputs for both devices is shown below.

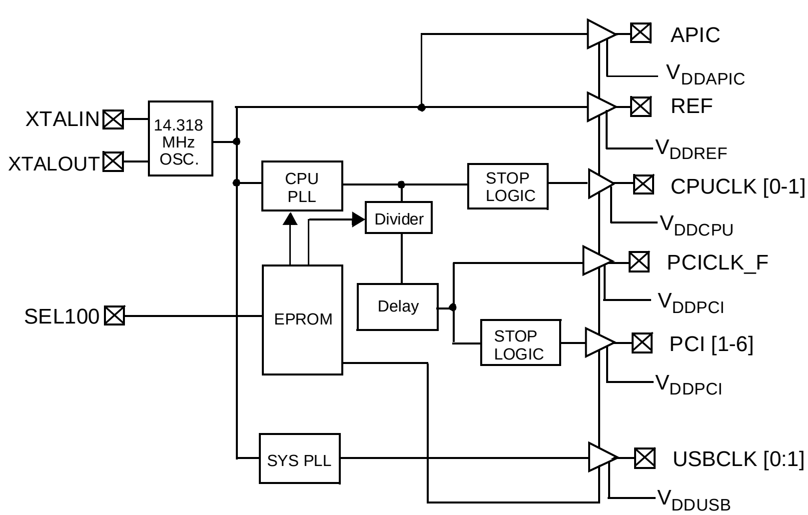
The CY2282 outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

CY2282 Selector Guide

Clock Outputs	CY2282-1	CY2282-11S
CPU (66.6, 100 MHz)	2	2
PCI (CPU/2, CPU/3 MHz)	7[1]	7[1]
USB (48 MHz)	2	2
APIC (14.318 MHz)	1	1
REF (14.318 MHz)	1	1
CPU-PCI delay	1.5–4.0 ns	1.5–4.0 ns
Spread Spectrum	None	–0.5%

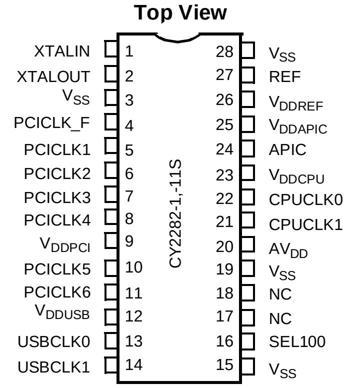
Note:
1. One free-running PCI clock.

Logic Block Diagram



Pin Configuration

SOIC
Top View



Pin Summary

Name	Pins	Description
V_{DDPCI}	9	3.3V Digital voltage supply for PCI clocks
V_{DDUSB}	12	3.3V Digital voltage supply for USB clocks
V_{DDREF}	26	3.3V Digital voltage supply for REF clocks
V_{DDAPIC}	25	2.5V Digital voltage supply for APIC clocks
V_{DDCPU}	23	2.5V Digital voltage supply for CPU clocks
AV_{DD}	20	3.3V Analog voltage supply
V_{SS}	3, 15, 19, 28	Ground
XTALIN[2]	1	Reference crystal input
XTALOUT[2]	2	Reference crystal feedback
N/C	17, 18	No Connect. Can be driven HIGH or LOW.
SEL100	16	CPU frequency select input, selects between 100 MHz and 66.6 MHz (see table below) Internal pull-up to V_{DD}
CPUCLK[0:1]	21, 22	CPU clock outputs
PCICLK[1:6]	5, 6, 7, 8, 10, 11	PCI clock outputs, at one-half or one-third the CPU frequency of 66.6 MHz or 100 MHz respectively
PCICLK_F	4	Free-running PCI clock output
APIC	24	APIC clock outputs
REF	27	3.3V Reference clock outputs
USBCLK[0:1]	13, 14	USB clock outputs

Function Table

SEL100	CPU/PCI Ratio	CPUCLK	PCICLK_F PCICLK	REF	APIC	USBCLK
0	2	66.66 MHz	33.33 MHz	14.318 MHz	14.318 MHz	48 MHz
1	3	100 MHz	33.33 MHz	14.318 MHz	14.318 MHz	48 MHz

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195
CPUCLK	100	99.77	–2346
USBCLK	48.0	48.008	167

Note:

2. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ....–0.5 to +7.0V

Input Voltage ....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ....>2000V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDPCI}, V_{DDUSB}, V_{DDREF}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.625	V
V_{DDAPIC}	APIC Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK APIC, REF USB		 20 30 20 20	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs[4]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs[4]				0.8	V
V_{OH}	High-level Output Voltage	V_{DDCPU} = V_{DDAPIC} = 2.375V	I_{OH} = 12 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	APIC			
V_{OL}	Low-level Output Voltage	V_{DDCPU} = V_{DDAPIC} = 2.375V	I_{OL} = 12 mA	CPUCLK		0.4	V
			I_{OL} = 18 mA	APIC			
V_{OH}	High-level Output Voltage	V_{DDPCI}, AV_{DD}, $V_{DDREF,}$ V_{DDUSB} = 3.135V	I_{OH} = 14.5 mA	PCICLK	2.4		V
			I_{OH} = 16 mA	USBCLK			
			I_{OH} = 16 mA	REF			
V_{OL}	Low-level Output Voltage	V_{DDPCI}, AV_{DD}, $V_{DDREF,}$ V_{DDUSB}= 3.135V	I_{OL} = 9.4 mA	PCICLK		0.4V	V
			I_{OL} = 9 mA	USBCLK			
			I_{OL} = 9 mA	REF			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–10	+10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				10	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD25}	Power Supply Current for 2.5V clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 66.6 MHz				70	mA
I_{DD25}	Power Supply Current for 2.5V clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 100 MHz				100	mA
I_{DD33}	Power Supply Current for 3.3V clocks	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs				170	mA

Notes:

3. Electrical parameters are guaranteed with these operating conditions.
4. Crystal Inputs have CMOS thresholds.

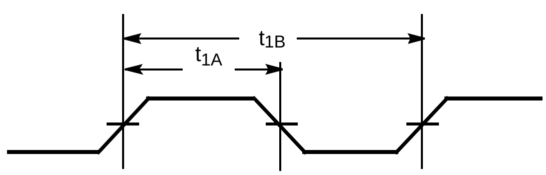
Switching Characteristics[5] Over the Operating Range

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[6]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK, APIC	CPU and APIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	USBCLK, REF	USB, REF Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V	0.4		1.8	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V		100	175	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew [7]	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.5		4.0	ns
t_7	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t_8	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V		200	250	ps
t_9	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V		250	500	ps
t_{10}	CPUCLK, PCICLK	Power-up Time	CPU, PCI clock stabilization from power-up			3	ms

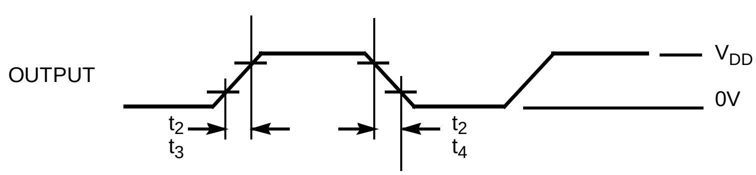
Notes:
5. All parameters specified with loaded outputs.
6. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
7. PCI lags CPU.

Switching Waveforms

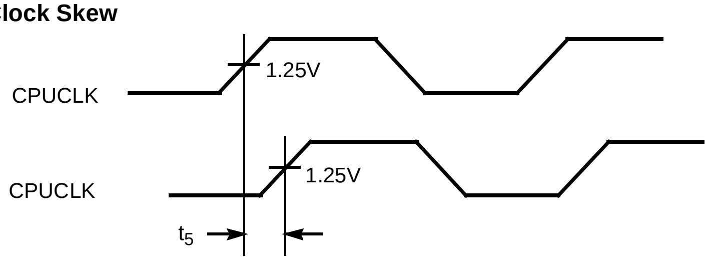
Duty Cycle Timing



All Outputs Rise/Fall Time

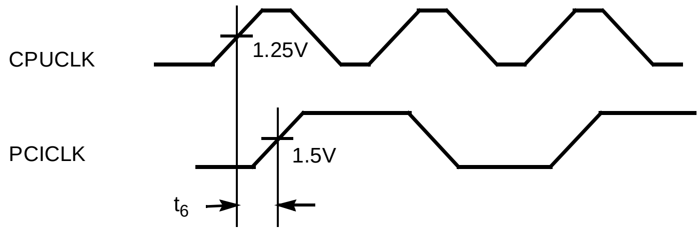


CPU-CPU Clock Skew

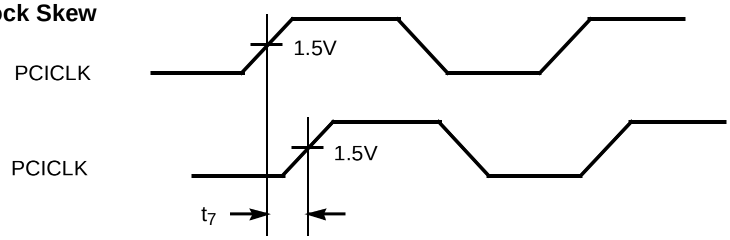


Switching Waveforms (continued)

CPU-PCI Clock Skew



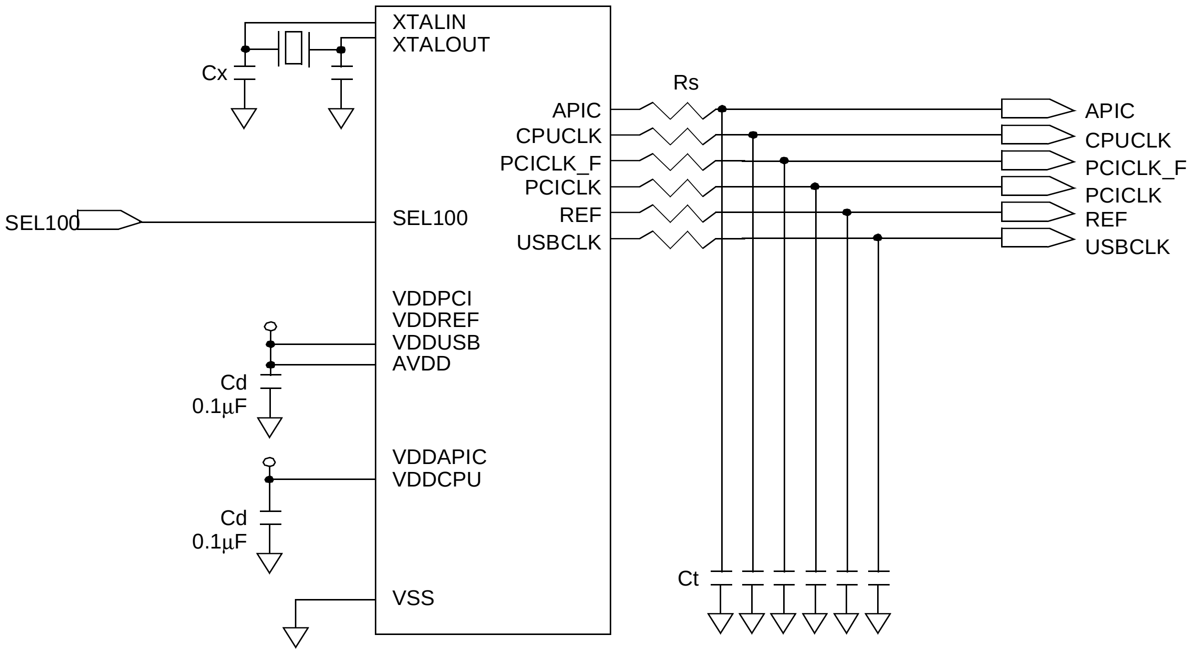
PCI-PCI Clock Skew



Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



CY2282-1,-11S 28 PIN SOIC

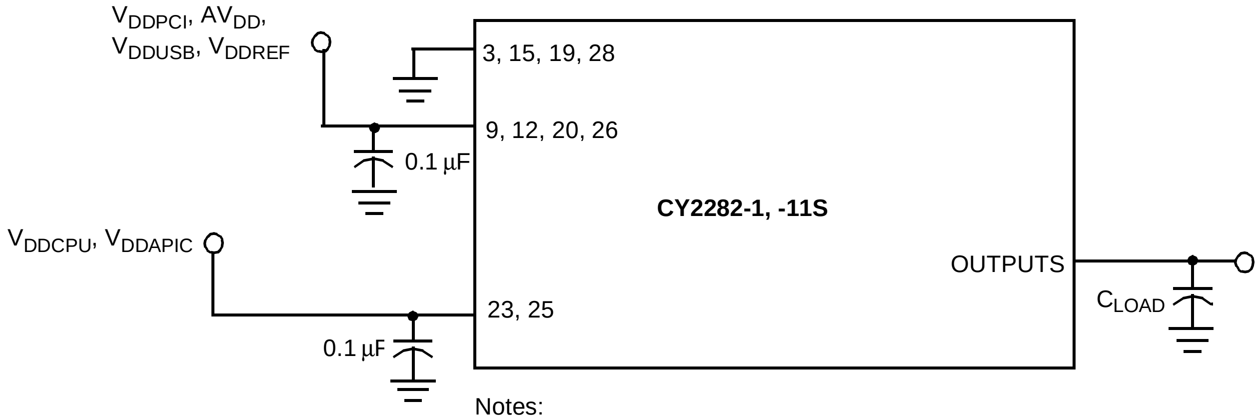
Cd = DECOUPLING CAPACITORS
Ct = OPTIONAL EM-REDUCING CAPACITORS
Cx = OPTIONAL LOAD MATCHING CAPACITOR
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and CLOAD of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different CLOAD is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the clock generator (specified in the data sheet), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board VDD from the clock generator VDD island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 µF–22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Notes:
Each supply pin must have an individual decoupling capacitor
All capacitors must be placed as close to the pins as is possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2282SC–1	S21	28-Pin SOIC	Commercial
CY2282SC–11S	S21	28-Pin SOIC	Commercial

Document #: 38–00693–A

Package Diagram

28-Lead (300-Mil) Molded SOIC S21