Data Sheet, Rev. 1.00, Feb. 2006

HYS72T64000HP–[3S/3.7]–A
HYS72T1280x0HP–[3S/3.7]–A
HYS72T256x20HP–[3S/3.7]–A
HYS72T256040HP–[3S/3.7]–A

240-Pin Registered DDR2 SDRAM Modules with parity

DDR2 SDRAM
RDIMM SDRAM
RoHs Compliant

Memory Products

infineon

Never stop thinking

Edition 2006-02

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1 Overview

This chapter gives an overview of the 240-pin Registered DDR2 SDRAM Modules with parity product family and describes its main characteristics.

1.1 Features

- 240-pin PC2-5300 and PC2-4200 DDR2 SDRAM memory modules
- One rank 64M x 72, 128M x 72, two ranks 128M × 72, 256M × 72, and four ranks 256M × 72 module organization and 64M × 8, 128M × 4 chip organization
- 512 MByte, 1GByte and 2GByte module built with 512-Mbit DDR2 SDRAMs in P-TFBGA-60 chipsize packages.
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- All speed grades faster than DDR2-400 comply with DDR2-400 timing specifications as well.
- Registered DIMM Parity bit for address and control bus
- Programmable CAS Latencies (3, 4 & 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- Based on standard reference layouts Raw Card “A-F”, “C-H”, “B-G”, “J“, “L“ and “N”
- RDIMM with parity Dimensions (nominal): 30.00 mm high, 133.35 mm wide
- RoHS compliant products[1)]

Table 1 Performance for PC2–5300–555

Product Type Speed Code			**–3S**	**Unit**
Speed Grade			**PC2–5300 5–5–5**	**—**
max. Clock Frequency	@CL5	f_{CK5}	333	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 2 Performance for PC2–4200–444

Product Type Speed Code			–3.7	Unit
Speed Grade			**PC2–4200 4–4–4**	**—**
max. Clock Frequency	@CL5	f_{CK5}	266	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns

Table 3 Performance for PC2–3200–333

Product Type Speed Code			–5	Units
Speed Grade			**PC2–3200 3–3–3**	**—**
max. Clock Frequency	@CL5	f_{CK5}	200	MHz
	@CL4	f_{CK4}	200	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	40	ns
min. Row Cycle Time		t_{RC}	55	ns

1.2 Description

The INFINEON HYS72T[64/128/256]xx0]HP–[3S/3.7]–A module family are Registered DIMM (RDIMM with parity) with 30.00 mm height based on DDR2 technology. DIMMs are available as ECC modules in 64M x 72 (512 MByte), 128M x 72 (1 GByte) and 256M x 72 (2 GByte) organization and density, intended for mounting into 240-Pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 4 Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-5300			
HYS72T64000HP–3S–A	512 MB 1R×8 PC2–5300P–555–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS72T128000HP–3S–A	1 GB 1R×4 PC2–5300P–555–12–H0	1 Rank, ECC	512 Mbit (×4)
HYS72T128020HP–3S–A	1 GB 2R×8 PC2–5300P–555–12–G0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256020HP–3S–A	2 GB 2R×4 PC2–5300P–555-12–L0	2 Ranks, ECC	512 Mbit (×4)
HYS72T256220HP–3S–A	2 GB 2R×4 PC2–5300P–555-12–J1	2 Ranks, ECC	512 Mbit (×4)
HYS72T256040HP–3S–A	2 GB 4R×8 PC2–5300P–555-12–N0	4 Ranks, ECC	512 Mbit (×8)
PC2-4200			
HYS72T64000HP–3.7–A	512 MB 1R×8 PC2–4200P–444–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS72T128000HP–3.7–A	1 GB 1R×4 PC2–4200P–444–12–H0	1 Rank, ECC	512 Mbit (×4)
HYS72T128020HP–3.7–A	1 GB 2R×8 PC2–4200P–444–12–G0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HP–3.7–A	2 GB 2R×4 PC2–4200P–444–12–J1	2 Ranks, ECC	512 Mbit (×4)
HYS72T256040HP–3.7–A	2 GB 4R×8 PC2–4200P–444–12–N0	4 Ranks, ECC	512 Mbit (×8)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS72T128000HP–3.7–A, indicating Rev. “A” dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see **Chapter 6** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200P–444–12–H0”, where 4200P means Registered DIMM parity modules with 4.26 GB/sec Module Bandwidth and “444-12” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card “H”

Table 5 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
512 MB	64M × 72	1	ECC	9	14/2/10	A-F
1 GB	128M × 72	1	ECC	18	14/2/10	C-H
1 GB	128M × 72	2	ECC	18	14/2/10	B-G
2 GB	256M × 72	2	ECC	36	14/2/10	J, L
2 GB	256M × 72	4	ECC	36	14/2/10	N

Table 6 Components on Modules [1)]

Product Type[2)]	DRAM Components[2)]	DRAM Density	DRAM Organization
HYS72T64000HP	HYB18T512800AF	512 Mbit	64M × 8
HYS72T128000HP	HYB18T512400AF	512 Mbit	128M × 4
HYS72T128020HP	HYB18T512800AF	512 Mbit	64M × 8
HYS72T256020HP	HYB18T512400AF	512 Mbit	128M × 4
HYS72T256220HP	HYB18T512400AF	512 Mbit	128M × 4
HYS72T256040HP	HYB18T512800AF	512 Mbit	64M × 8

1) For a detailed description of all available functions of the DRAM components on these modules see the component data sheet.

2) Green Product

2 Pin Configuration and Block Diagrams

2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in Table 7 (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in Table 8 and Table 9 respectively. The pin numbering is depicted in Figure 1.

Table 7 Pin Configuration of RDIMM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signal CK0, Complementary Clock Signal $\overline{CK0}$** The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
186	$\overline{CK0}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enables 1:0** Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode. *Note: 2-Ranks module*
171	CKE1	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
Control Signals				
193	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0** Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When $\overline{S}$ is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state. *Note: 2-Ranks module*
76	$\overline{S1}$	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
192	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)** When sampled at the cross point of the rising edge of CK, and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
74	$\overline{CAS}$	I	SSTL	
73	$\overline{WE}$	I	SSTL	

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
18	$\overline{\text{RESET}}$	I	CMOS	**Register Reset** The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When LOW, all register outputs will be driven LOW and the PLL clocks to the DRAMs and the register(s) will be set to low-level. The PLL will remain synchronized with the input clock.
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0** Selects internal SDRAM memory bank
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	**Not Connected** Less than 1Gb DDR2 SDRAMS
188	A0	I	SSTL	**Address Bus 12:0, Address Signal 10/AutoPrecharge** During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[*1*:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[*1*:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[*1*:0] inputs. If AP is LOW, then BA[*1*:0] are used to define which bank to precharge.
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13**
	NC	NC	—	**Not Connected** *Note: Non CA parity modules based on 256 Mbit component*
174	A14	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module*
173	A15	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module*

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	Data Input/Output pins
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
206	DQ39	I/O	SSTL	**Data Bus 63:0**
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bits				
42	CB0	I/O	SSTL	**Check Bits 7:0** Check Bit Input / Output pins *Note: NC on Non-ECC module*
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobes 17:0** The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately. *Note: See block diagram for corresponding DQ signals*
6	$\overline{\text{DQS0}}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
125	DQS9	I/O	SSTL	
126	$\overline{\text{DQS9}}$	I/O	SSTL	
134	DQS10	I/O	SSTL	
135	$\overline{\text{DQS10}}$	I/O	SSTL	
146	DQS11	I/O	SSTL	
147	$\overline{\text{DQS11}}$	I/O	SSTL	
155	DQS12	I/O	SSTL	
156	$\overline{\text{DQS12}}$	I/O	SSTL	
202	DQS13	I/O	SSTL	
203	$\overline{\text{DQS13}}$	I/O	SSTL	
211	DQS14	I/O	SSTL	
212	$\overline{\text{DQS14}}$	I/O	SSTL	
223	DQS15	I/O	SSTL	
224	$\overline{\text{DQS15}}$	I/O	SSTL	
232	DQS16	I/O	SSTL	
233	$\overline{\text{DQS16}}$	I/O	SSTL	
164	DQS17	I/O	SSTL	
165	$\overline{\text{DQS17}}$	I/O	SSTL	

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Mask				
125	DM0	I	SSTL	**Data Masks 8:0** The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect. *Note: x8 based module*
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock** This signal is used to clock data into and out of the SPD EEPROM.
119	SDA	I/O	OD	**Serial Bus Data** This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
239	SA0	I	CMOS	**Serial Address Select Bus 2:0** These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Parity				
55	$\overline{\text{ERR\_OUT}}$	O	CMOS	**Parity bits** *Note: Only for modules with parity bit for address and control bus. Not connected on non-parity registered modules.*
	PAR_IN	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage** Reference voltage for the SSTL-18 inputs.
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply** Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
51, 56, 62, 72, 75, 78, 170, 175,, 181, 191, 194	V_{DDQ}	PWR	—	**I/O Driver Power Supply** Power and ground for the DDR SDRAM
53, 59, 64, 67, 69, 172, 178, 184,, 187, 189, 197	V_{DD}	PWR	—	**Power Supply** Power and ground for the DDR SDRAM

Table 7 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	—	**Ground Plane** Power and ground for the DDR SDRAM
Other Pins				
19, 55, 68, 102, 137, 138, 173, 220, 221	NC	NC	—	**Not connected** Pins not connected on Infineon RDIMM's
195	ODT0	I	SSTL	**On-Die Termination Control 1:0** Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. *Note: 2-Ranks module*
77	ODT1	I	SSTL	
	NC	NC	—	*Note: 1-Rank modules*

Table 8 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Table 9 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

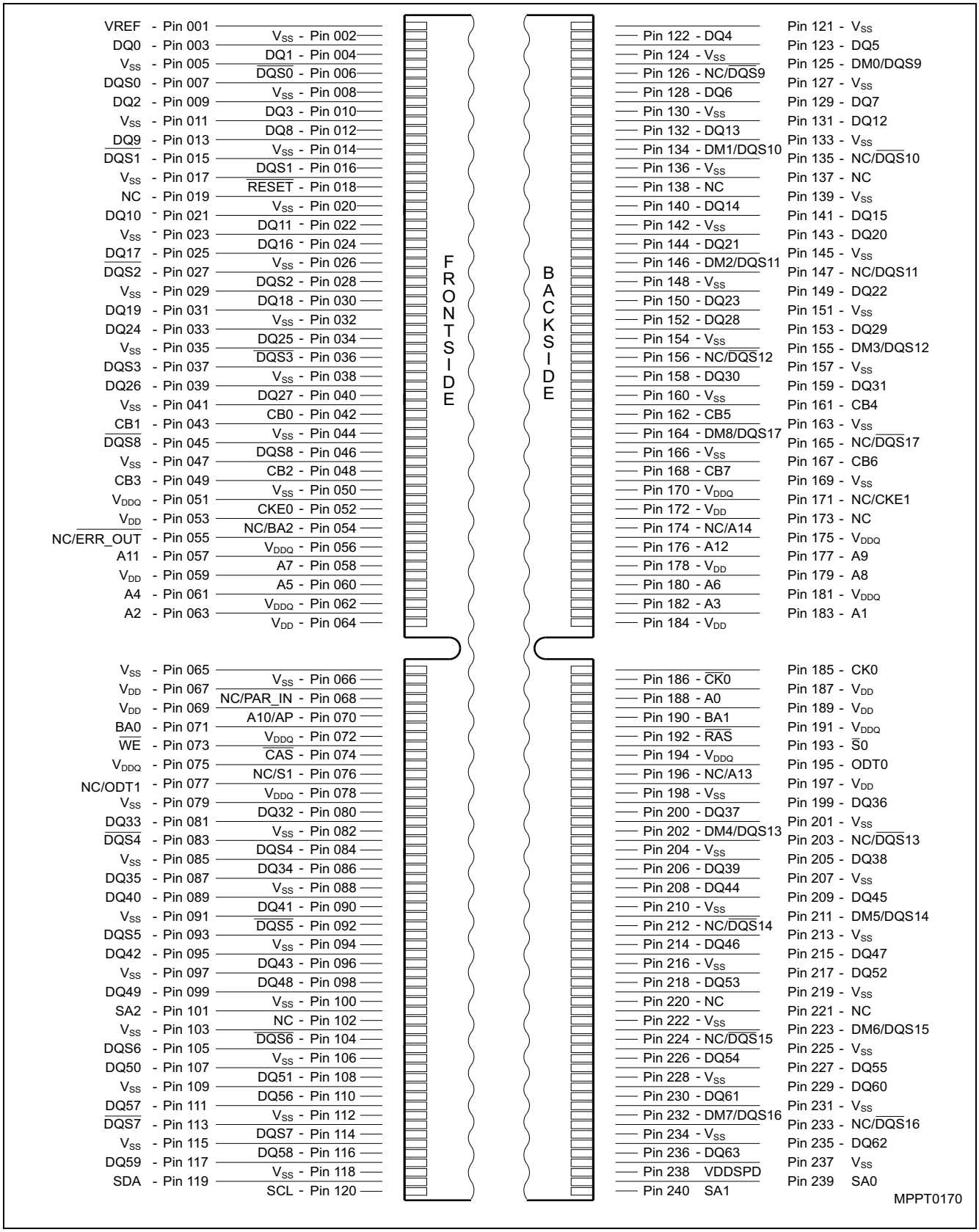

Figure 1 Pin Configuration for RDIMM (240 pins)

2.2 Block Diagram

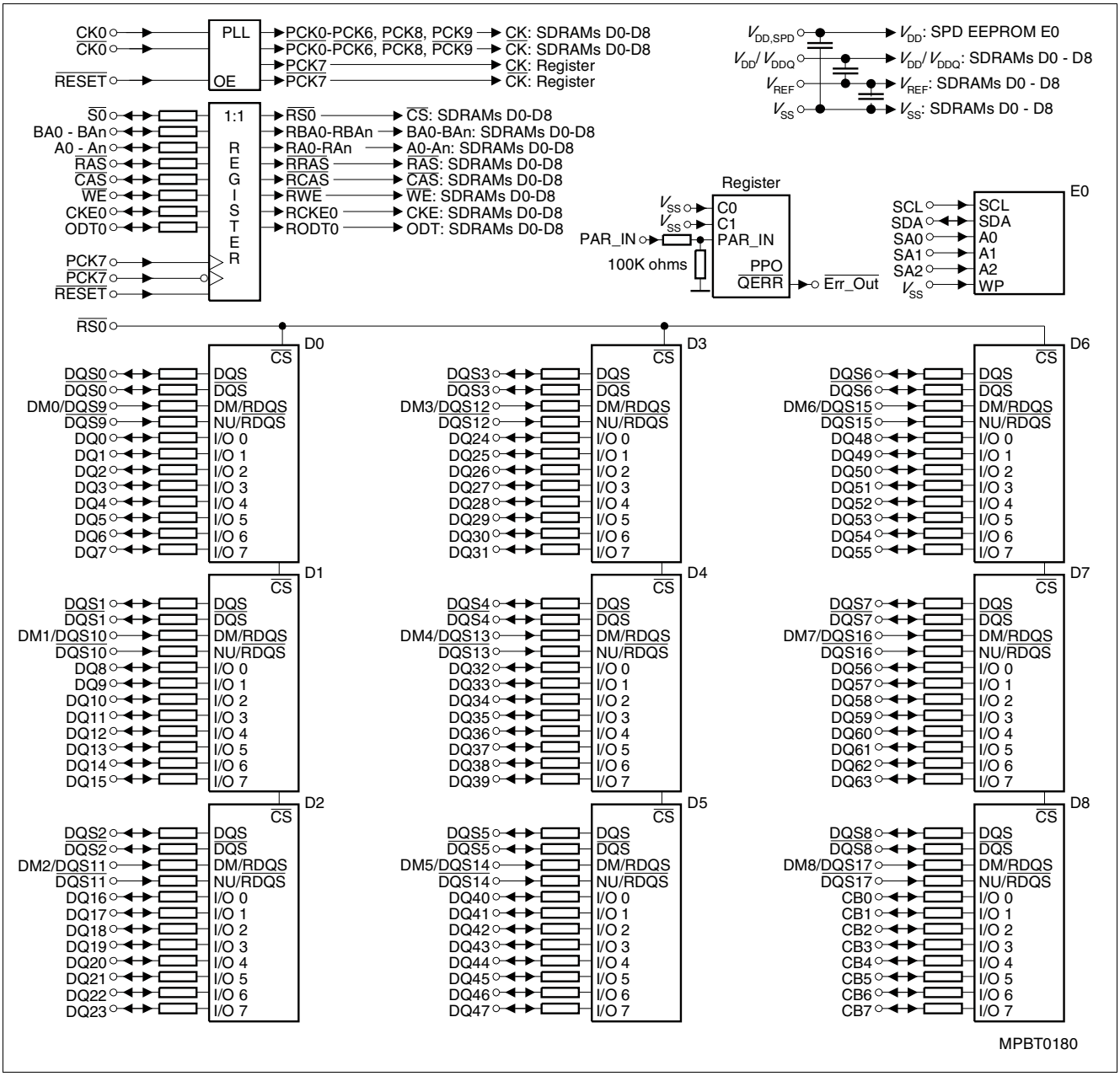

Figure 2 Block Diagram Raw Card A-F RDIMM (x72, 1Rank, x8)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *$\overline{S0}$ connects to $\overline{DCS}$ of register1 and $\overline{CSR}$ of register2.*
3. *$\overline{CSR}$ of register1 and $\overline{DCS}$ of register2 connects to V_{DD}*
4. *$\overline{RESET}$, PCK7 and $\overline{PCK7}$ connect to both registers.*

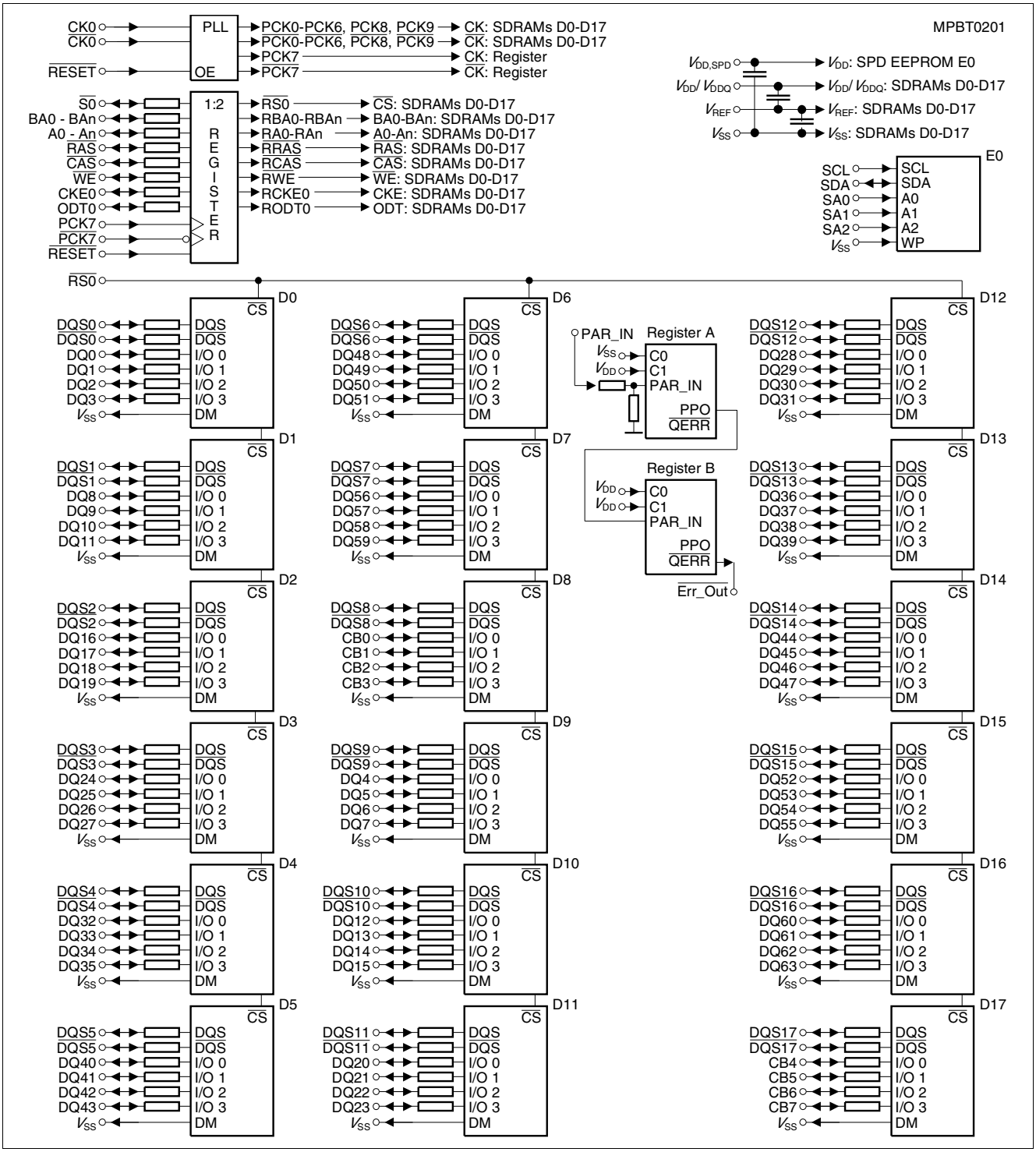

Figure 3 Block Diagram Raw Card C-H RDIMM (x72, 1Rank, x4)

Notes

1. Unless otherwise noted, resistors are 22 $\Omega \pm 5$ %
2. *S0* connects to *DCS* of register1 and *CSR* of register2.
3. *CSR* of register1 and *DCS* of register2 connects to V_{DD}.
4. *RESET, PCK7 and PCK7 connect to both registers.*

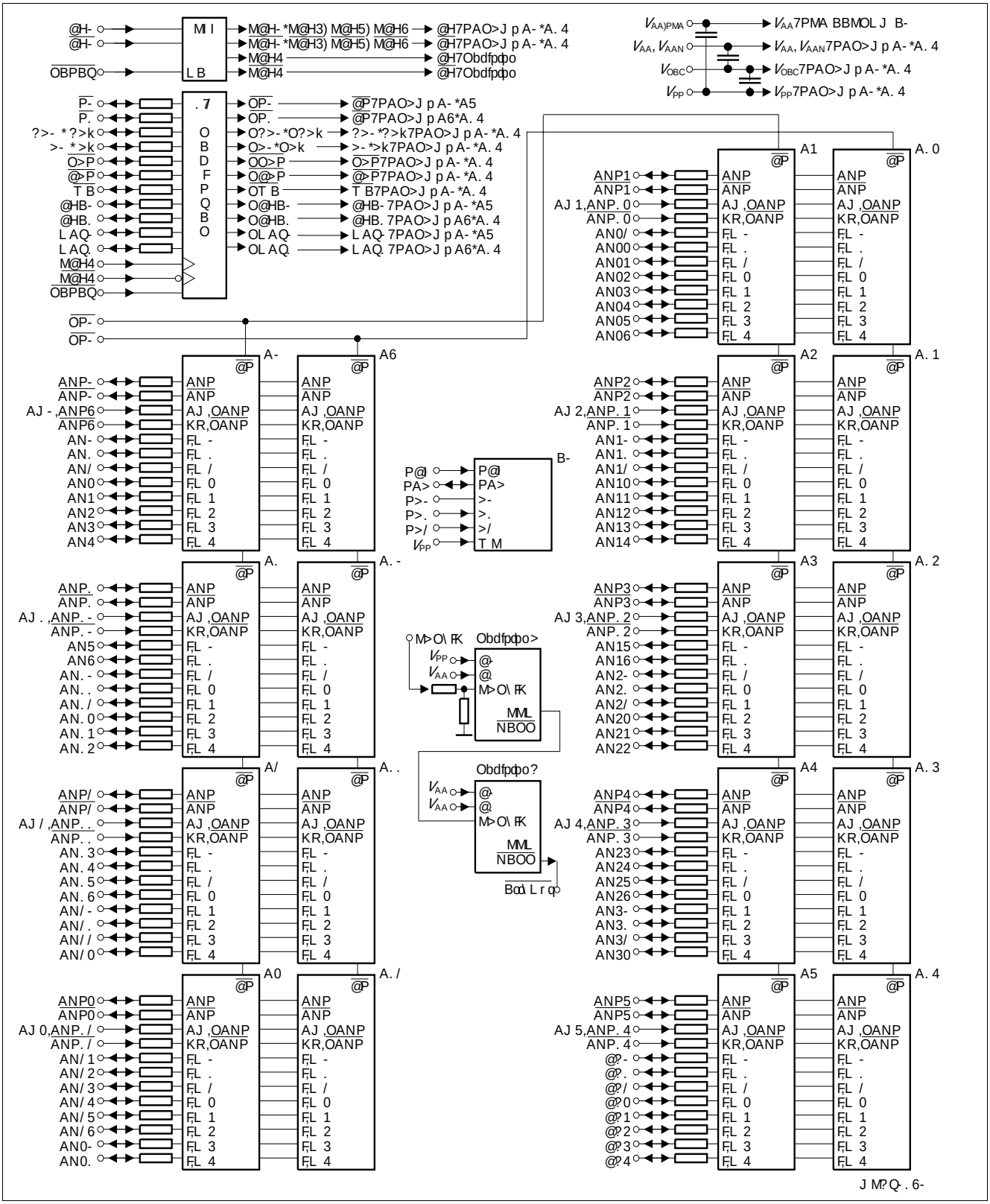

Figure 4 Block Diagram Raw Card B-G RDIMM (x72, 2Ranks, x8)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *$\overline{RS0}$ and $\overline{RS1}$ alternate between the back and front sides of the DIMM.*

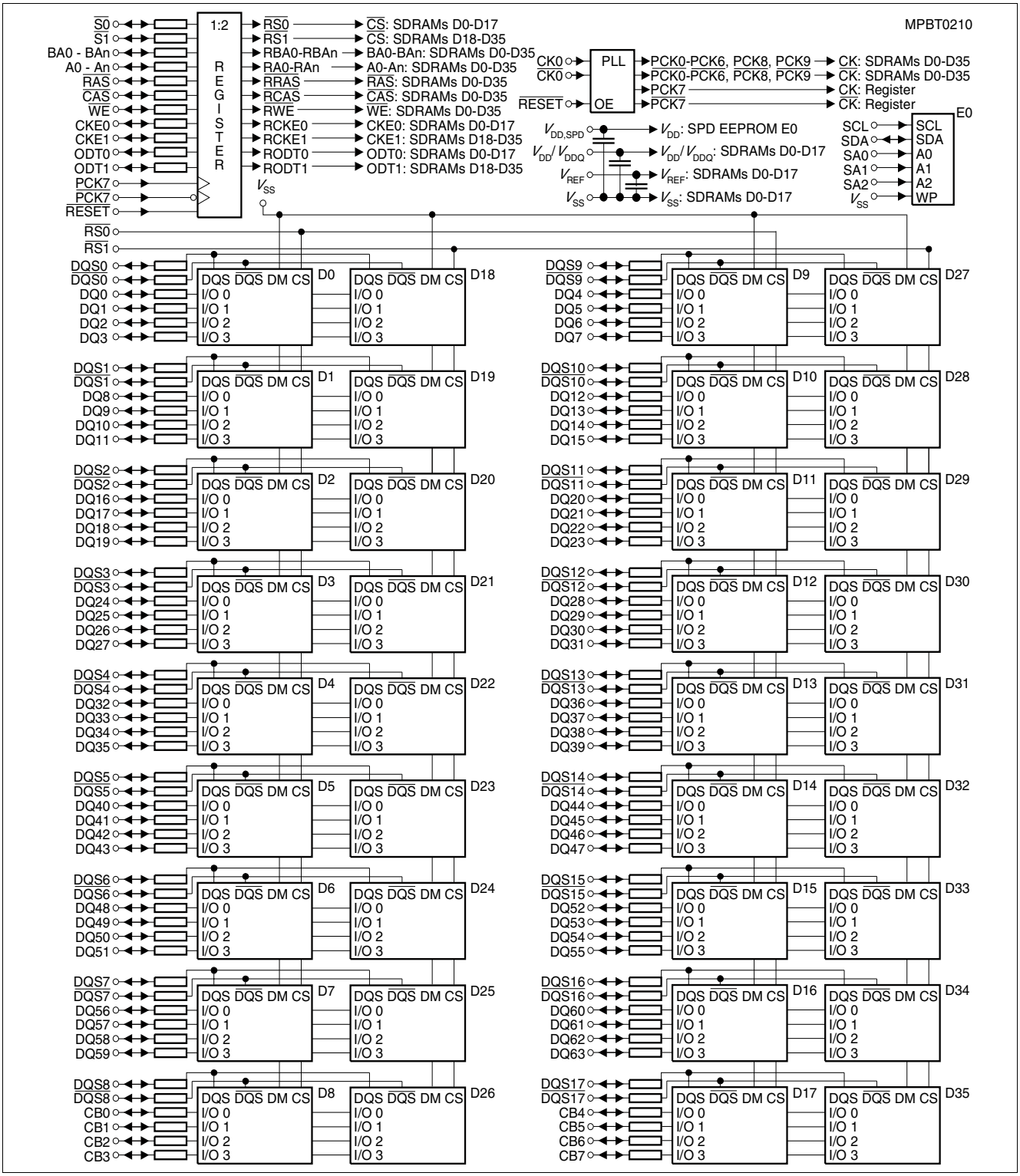

Figure 5 Block Diagram Raw Card J RDIMM (x72, 2Ranks, x4)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *$\overline{RS0}$ and $\overline{RS1}$ alternate between the bottom and surface sides of the DIMM.*
3. *$\overline{S0}$ connects to $\overline{DCS}$ and $\overline{S1}$ Connects to $\overline{CSR}$ on a pair of registers. $\overline{S1}$ connects to $\overline{DCS}$ and $\overline{S0}$ connects to $\overline{CSR}$ on another pair of registers.*
4. *$\overline{RESET}$, PCK7 and $\overline{PCK7}$ connect to all registers.*

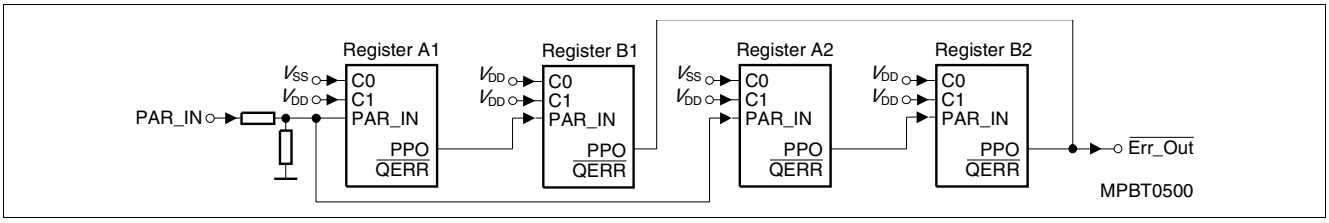

Figure 6 Block Diagram Raw Card J Signal for Address and Command Parity Function

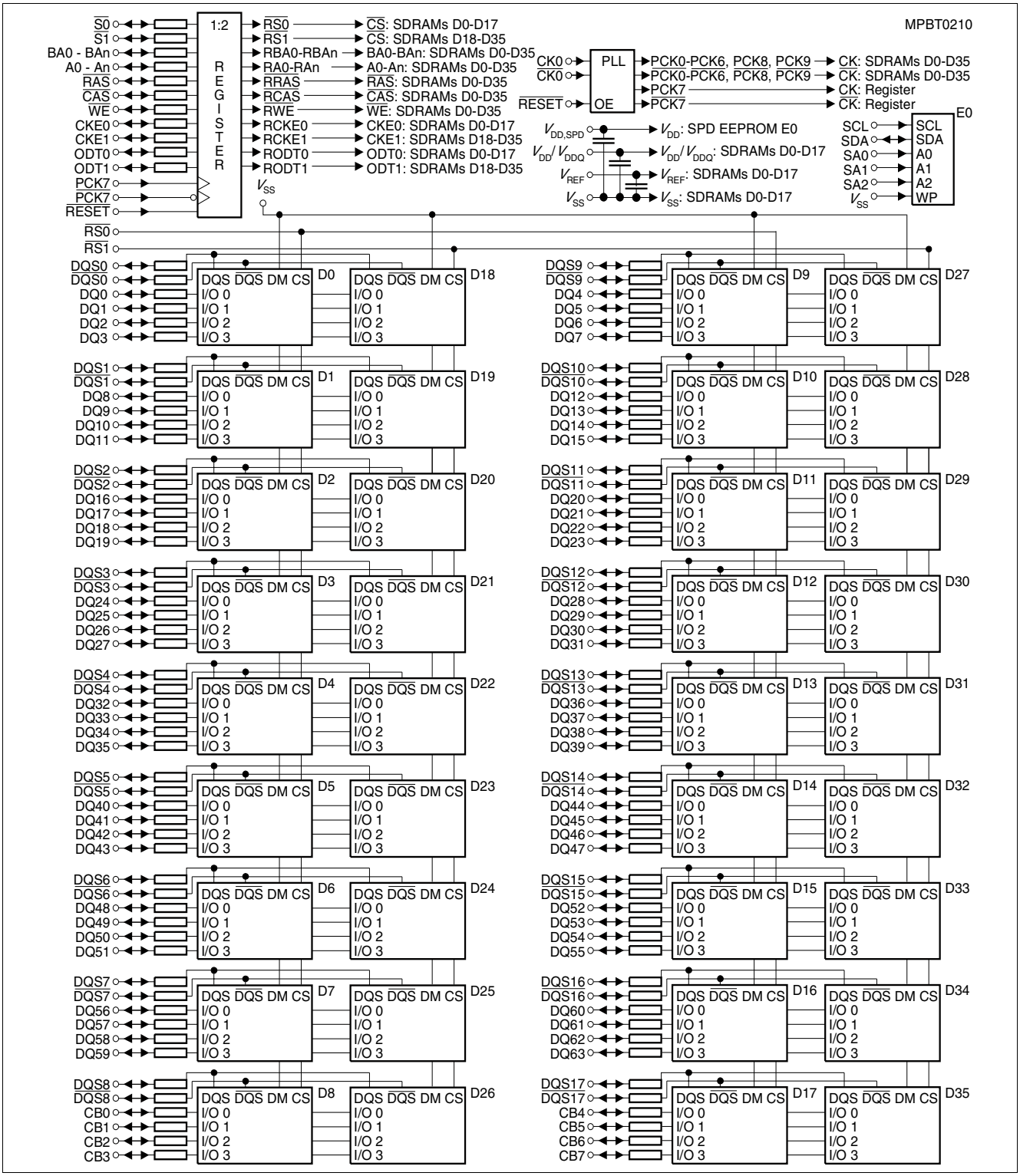

Figure 7 Block Diagram Raw Card L RDIMM (x72, 2Ranks, x4)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *$\overline{RS0}$ and $\overline{RS1}$ alternate between the bottom and surface sides of the DIMM.*
3. *$\overline{S0}$ connects to $\overline{DCS}$ and $\overline{S1}$ Connects to $\overline{CSR}$ on a pair of registers. $\overline{S1}$ connects to $\overline{DCS}$ and $\overline{S0}$ connects to $\overline{CSR}$ on another pair of registers.*
4. *$\overline{RESET}$, PCK7 and $\overline{PCK7}$ connect to all registers.*

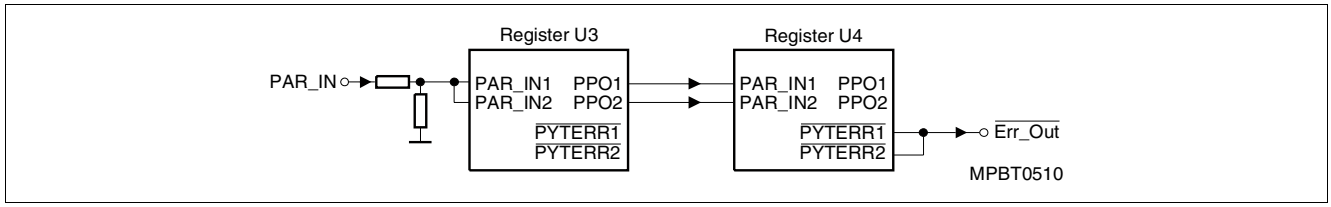

Figure 8 Block Diagram Raw Card L Signal for Address and Command Parity Function

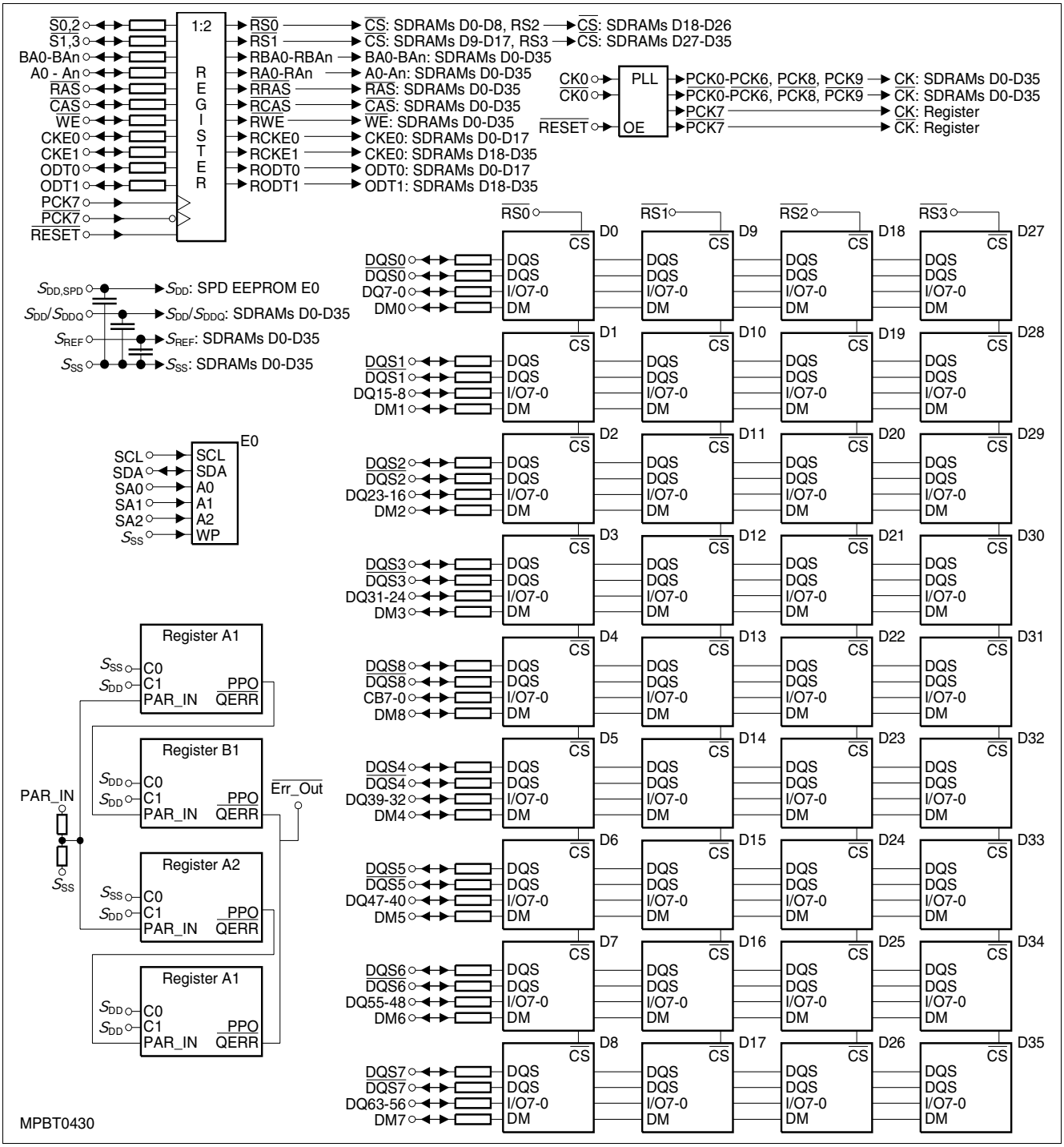

Figure 9 Block Diagram Raw Card N RDIMM (x72, 4Ranks, x8)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *$\overline{S0}$ and $\overline{S2}$ connects to $\overline{DCS0}$, $\overline{S1}$ and $\overline{S3}$ to $\overline{DCS1}$ on a Register A. $\overline{S1}$ and $\overline{S3}$ connects to $\overline{DCS}$ and $\overline{S0}$ and $\overline{S2}$ connects to $\overline{CSR}$ on another pair of Register.*
3. *$\overline{S2}$ and $\overline{S3}$ have required pull up resistors (100K Ω), not indicated here.*
4. *A13-An have optional pull down resistors (100K Ω), not indicated here.*
5. *RESET, PCK7 and $\overline{PCK7}$ connect to all Registers. Other signals connect to two of four Registers.*

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	
Voltage on V_{DD} relative to V_{SS}	V_{DD}	–1.0	2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	–0.5	2.3	V	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values maycause irreversible damage to the integrated circuit.

3.2 DC Operating Conditions

Table 11 Operating Conditions

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+55	°C	
DRAM Component Case Temperature Range	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	–50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3) Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.
4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.
5) Up to 3000 m

Table 12 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Notes
		Min.	Nom.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	–0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	–5		5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 AC Characteristics

3.3.1 Speed Grades Definitions

Table 13 Speed Grade Definition Speed Bins for DDR2–667

Speed Grade			DDR2–667		Unit	Notes
IFX Sort Name			–3S			
CAS-RCD-RP latencies			5–5–5		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 14 Speed Grade Definition Speed Bins for DDR2-533

Speed Grade			DDR2–533C		Unit	Note
IFX Sort Name			–3.7			
CAS-RCD-RP latencies			4–4–4		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 15 Speed Grade Definition Speed Bins for DDR2–400B

Speed Grade			DDR2–400B		Unit	Note
IFX Sort Name			–5			
CAS-RCD-RP latencies			3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 AC Timing Parameters

List of AC Timing Tables

- Table 16 “Timing Parameter by Speed Grade - DDR2–667” on Page 29
- Table 17 “Timing Parameter by Speed Grade - DDR2-533” on Page 31
- Table 18 “Timing Parameter by Speed Grade - DDR2-400” on Page 33

Table 16 Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	175	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	—	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	240	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	—	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	275	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	200	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	

Table 16 Timing Parameter by Speed Grade - DDR2–667 (cont'd)

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HPQ} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	340	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	8)
		—	3.9	µs	9)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.35 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes [4)5)6)7)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) 0 °C≤ T_{CASE} ≤ 85 °C
9) 85 °C < T_{CASE} ≤ 95 °C

Table 17 Timing Parameter by Speed Grade - DDR2-533

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	375	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—		

Table 17 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	[8)]
		—	3.9	µs	[9)]
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes [4)5)6)7)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) 0 °C≤ T_{CASE} ≤ 85 °C
9) 85 °C < T_{CASE} ≤ 95 °C

Table 18 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	350	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—		

Table 18 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	[8)]
		—	3.9	µs	[9)]
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes [4)5)6)7)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) 0 °C≤ T_{CASE} ≤ 85 °C
9) 85 °C < T_{CASE} ≤ 95 °C

3.3.3 ODT AC Electrical Characteristics

Table 19 ODT AC Electrical Characteristics and Operating Conditions for DDR2-667

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

Table 20 ODT AC Electrical Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

3.4 Currents Specifications and Conditions

Table 21 I_{DD} Measurement Conditions [1)2)3)4)5)6)7)8)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = $CL_{.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CK.MIN}$., Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 21 I_{DD} Measurement Conditions (cont'd)[1)2)3)4)5)6)7)8)]

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET is LOW. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{OUT} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) IDD specifications are tested after the device is properly initialized and IDD parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 22**
4) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
6) RESET signal is HIGH for all currents, except for I_{DD6} (Self Refresh)
7) All current measurements includes Register and PLL current consumption
8) For details and notes see the relevant INFINEON component data sheet

Table 22 Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are V_{REF} = V_{DDQ}/2
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.

Table 23 I_{DD} Specification for HYS72T[64/128/256]xx0HP-3S-A

Product Type	HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A	Unit	Notes[1)]
Organization	**512MB**	**1GB**	**1GB**	**2GB**	**2GB**	**2GB**		
	1 Rank	**1 Rank**	**2 Ranks**	**2 Ranks**	**2 Ranks**	**4 Ranks**		
	×72	**×72**	**×72**	**×72**	**×72**	**×72**		
	-3S	**-3S**	**-3S**	**-3S**	**-3S**	**-3S**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	1020	1870	1070	1960	1960	1160	mA	2)
I_{DD1}	1150	2130	1200	2220	2220	1290	mA	2)
I_{DD2P}	430	690	480	780	780	570	mA	3)
I_{DD2N}	840	1500	1290	2400	2400	2190	mA	3)
I_{DD2Q}	750	1320	1110	2040	2040	1830	mA	3)
$I_{DD3P(MRS=0)}$	560	940	730	1280	1280	1070	mA	3)
$I_{DD3P(MRS=1)}$	440	700	490	810	810	600	mA	3)
I_{DD3N}	840	1500	1290	2400	2400	2190	mA	3)
I_{DD4R}	1560	2940	1600	3030	3030	1690	mA	2)
I_{DD4W}	1650	3120	1690	3210	3210	1780	mA	2)
I_{DD5B}	1650	3120	1690	3210	3210	1780	mA	2)
I_{DD5D}	440	700	490	810	810	600	mA	3)4)
I_{DD6}	45	90	90	180	180	180	mA	3)4)
I_{DD7}	1710	3240	1750	3330	3330	1840	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

Table 24 I_{DD} Specification for HYS72T[64/128/256]xx0HP-3.7-A

Product Type	HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A	Unit	Notes[1)]
Organization	**512MB**	**1GB**	**1GB**	**2GB**	**2GB**		
	1 Rank	**1 Rank**	**2 Ranks**	**2 Ranks**	**4 Ranks**		
	×72	**×72**	**×72**	**×72**	**×72**		
	-3.7	**-3.7**	**-3.7**	**-3.7**	**-3.7**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	920	1670	950	1740	1020	mA	2)
I_{DD1}	1010	1850	1040	1920	1110	mA	2)
I_{DD2P}	370	570	400	640	470	mA	3)
I_{DD2N}	690	1220	1050	1940	1770	mA	3)
I_{DD2Q}	600	1040	870	1580	1410	mA	3)
$I_{DD3P(MRS=0)}$	470	790	620	1080	910	mA	3)
$I_{DD3P(MRS=1)}$	380	590	420	680	510	mA	3)
I_{DD3N}	690	1220	1050	1940	1770	mA	3)
I_{DD4R}	1140	2120	1180	2190	1250	mA	3)
I_{DD4W}	1190	2210	1220	2280	1290	mA	2)
I_{DD5B}	1500	2840	1540	2920	1610	mA	2)
I_{DD5D}	380	610	440	720	550	mA	3)4)
I_{DD6}	36	72	72	144	144	mA	3)4)
I_{DD7}	1590	3030	1630	3100	1700	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

3.4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 25 I_{DD} Measurement Test Conditions for DDR2–667

Parameter		Symbol	–3S	Unit
			DDR2–667D	
CAS Latency		$CL_{(IDD)}$	5	t_{CK}
Clock Cycle Time		$t_{CK(IDD)}$	3.75	ns
Active to Read or Write delay		$t_{RCD(IDD)}$	15	ns
Active to Active / Auto-Refresh command period		$t_{RC(IDD)}$	60	ns
Active bank A to Active bank B command delay	×8[1)]	$t_{RRD(IDD)}$	7.5	ns
	×16[2)]	$t_{RRD(IDD)}$	10	ns
Active to Precharge Command		$t_{RAS.MIN(IDD)}$	45	ns
		$t_{RAS.MAX(IDD)}$	70000	ns
Precharge Command Period		$t_{RP(IDD)}$	15	ns
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC(IDD)}$	105	ns
Average periodic Refresh interval		t_{REFI}	7.8	µs

1) ×4 & ×8 (1 kB page size)

2) ×16 (2 kB page size), not on 256M components

Table 26 I_{DD} Measurement Test Conditions for DDR2–533

Parameter		Symbol	–3.7	Unit
			DDR2–533C	
CAS Latency		$CL_{(IDD)}$	4	t_{CK}
Clock Cycle Time		$t_{CK(IDD)}$	3.75	ns
Active to Read or Write delay		$t_{RCD(IDD)}$	15	ns
Active to Active / Auto-Refresh command period		$t_{RC(IDD)}$	60	ns
Active bank A to Active bank B command delay	×8[1)]	$t_{RRD(IDD)}$	7.5	ns
	×16[2)]	$t_{RRD(IDD)}$	10	ns
Active to Precharge Command		$t_{RAS.MIN(IDD)}$	45	ns
		$t_{RAS.MAX(IDD)}$	70000	ns
Precharge Command Period		$t_{RP(IDD)}$	15	ns
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC(IDD)}$	105	ns
Average periodic Refresh interval		t_{REFI}	7.8	µs

1) ×4 & ×8 (1 kB page size)

2) ×16 (2 kB page size), not on 256M components

3.4.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 27 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
		7.5	9	11.25	mA/DQ	A6 = 1, A2 = 1
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0
		15	18	22.5	mA/DQ	A6 = 1, A2 = 0

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 28 “SPD Codes for HYS72T[64/128]xxxHP–3S–A” on Page 42
- Table 29 “SPD Codes for HYS72T256xx0HP–3S–A” on Page 46
- Table 30 “SPD Codes for HYS72T[64/128/256]xx0HP–3.7–A” on Page 50

Table 28 SPD Codes for HYS72T[64/128]xxxHP–3S–A

Product Type		HYS72T64000HP–3S–A	HYS72T128000HP–3S–A	HYS72T128020HP–3S–A
Organization		512MB	1 GByte	1 GByte
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–555	PC2–5300R–555	PC2–5300R–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	06	06	06
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04

Table 28 SPD Codes for HYS72T[64/128]xxxHP–3S–A (cont'd)

Product Type		**HYS72T64000HP–3S–A**	**HYS72T128000HP–3S–A**	**HYS72T128020HP–3S–A**
Organization		**512MB**	**1 GByte**	**1 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	80	01	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18

Table 28 SPD Codes for HYS72T[64/128]xxxHP–3S–A (cont'd)

Product Type		HYS72T64000HP–3S–A	HYS72T128000HP–3S–A	HYS72T128020HP–3S–A
Organization		**512MB**	**1 GByte**	**1 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
48	Psi(T-A) DRAM	78	78	78
49	ΔT_0 (DT0)	4B	4B	4B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	2E	2E	2E
51	ΔT_{2P} (DT2P)	26	26	26
52	ΔT_{3N} (DT3N)	26	26	26
53	$\Delta T_{3P.fast}$ (DT3P fast)	2B	2B	2B
54	$\Delta T_{3P.slow}$ (DT3P slow)	1B	1B	1B
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4A	4A	4A
56	ΔT_{5B} (DT5B)	20	20	20
57	ΔT_7 (DT7)	22	22	22
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	68	68	68
61	ΔT_{REG} (DTREG) / Toggle Rate	94	94	94
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	47	C2	49
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00

Table 28 SPD Codes for HYS72T[64/128]xxxHP–3S–A (cont'd)

Product Type		**HYS72T64000HP–3S–A**	**HYS72T128000HP–3S–A**	**HYS72T128020HP–3S–A**
Organization		**512MB**	**1 GByte**	**1 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	36	31	31
77	Product Type, Char 5	34	32	32
78	Product Type, Char 6	30	38	38
79	Product Type, Char 7	30	30	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	30	30
82	Product Type, Char 10	50	48	48
83	Product Type, Char 11	33	50	50
84	Product Type, Char 12	53	33	33
85	Product Type, Char 13	41	53	53
86	Product Type, Char 14	20	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 29 SPD Codes for HYS72T256xx0HP–3S–A

Product Type		HYS72T256020HP–3S–A	HYS72T256220HP–3S–A	HYS72T256040HP–3S–A
Organization		**2 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0E	0E	0E
4	Number of Column Addresses	0B	0B	0A
5	DIMM Rank and Stacking Information	61	61	63
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	06	06	06
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	04	04	08
14	Error Checking SDRAM Width	04	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	07	07	07
22	Component Attributes	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60

Table 29 SPD Codes for HYS72T256xx0HP–3S–A (cont'd)

Product Type		**HYS72T256020HP–3S–A**	**HYS72T256220HP–3S–A**	**HYS72T256040HP–3S–A**
Organization		**2 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	01	01	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
48	Psi(T-A) DRAM	78	78	78
49	ΔT_0 (DT0)	4B	4B	4B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	2E	2E	2E
51	ΔT_{2P} (DT2P)	26	26	26
52	ΔT_{3N} (DT3N)	26	26	26
53	$\Delta T_{3P.fast}$ (DT3P fast)	2B	2B	2B

Table 29 SPD Codes for HYS72T256xx0HP–3S–A (cont'd)

Product Type		**HYS72T256020HP–3S–A**	**HYS72T256220HP–3S–A**	**HYS72T256040HP–3S–A**
Organization		**2 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
54	$\Delta T_{3P.slow}$ (DT3P slow)	1B	1B	1B
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4A	4A	4A
56	ΔT_{5B} (DT5B)	20	20	20
57	ΔT_{7} (DT7)	22	22	22
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	68	68	68
61	ΔT_{REG} (DTREG) / Toggle Rate	94	94	94
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	C5	C5	4D
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	32	32	32
77	Product Type, Char 5	35	35	35
78	Product Type, Char 6	36	36	36
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	32	32	34

Table 29 SPD Codes for HYS72T256xx0HP–3S–A (cont'd)

Product Type		**HYS72T256020HP–3S–A**	**HYS72T256220HP–3S–A**	**HYS72T256040HP–3S–A**
Organization		**2 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**
		2 Ranks (×4)	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
81	Product Type, Char 9	30	30	30
82	Product Type, Char 10	48	48	48
83	Product Type, Char 11	50	50	50
84	Product Type, Char 12	33	33	33
85	Product Type, Char 13	53	53	53
86	Product Type, Char 14	41	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 30 SPD Codes for HYS72T[64/128/256]xx0HP–3.7–A

Product Type		HYS72T64000HP–3.7–A	HYS72T128000HP–3.7–A	HYS72T128020HP–3.7–A	HYS72T256220HP–3.7–A	HYS72T256040HP–3.7–A
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61	61	63
6	Data Width	48	48	48	48	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	06	06	06	06	06
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	08	04	08	04	08
14	Error Checking SDRAM Width	08	04	08	04	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	01	01	01	01	01
21	DIMM Attributes	04	05	05	07	07
22	Component Attributes	03	03	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	50

Table 30 SPD Codes for HYS72T[64/128/256]xx0HP–3.7–A (cont'd)

Product Type		**HYS72T64000HP–3.7–A**	**HYS72T128000HP–3.7–A**	**HYS72T128020HP–3.7–A**	**HYS72T256220HP–3.7–A**	**HYS72T256040HP–3.7–A**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28	28	28
46	PLL Relock Time	0F	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	51	51	51	51	51
48	Psi(T-A) DRAM	78	78	78	78	78
49	ΔT_0 (DT0)	3F	3F	3F	3F	3F

Table 30 SPD Codes for HYS72T[64/128/256]xx0HP–3.7–A (cont'd)

Product Type		**HYS72T64000HP–3.7–A**	**HYS72T128000HP–3.7–A**	**HYS72T128020HP–3.7–A**	**HYS72T256220HP–3.7–A**	**HYS72T256040HP–3.7–A**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	22	22	22	22	22
51	ΔT_{2P} (DT2P)	1E	1E	1E	1E	1E
52	ΔT_{3N} (DT3N)	1E	1E	1E	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	24	24	24	24	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17	17	17	17
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	34	34	34	34	34
56	ΔT_{5B} (DT5B)	1E	1E	1E	1E	1E
57	ΔT_{7} (DT7)	20	20	20	20	20
58	Psi(ca) PLL	C4	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	61	61	61	61	61
61	ΔT_{REG} (DTREG) / Toggle Rate	78	78	78	78	78
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	19	94	1B	97	1F
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37	37
74	Product Type, Char 2	32	32	32	32	32

Table 30 SPD Codes for HYS72T[64/128/256]xx0HP–3.7–A (cont'd)

Product Type		HYS72T64000HP–3.7–A	HYS72T128000HP–3.7–A	HYS72T128020HP–3.7–A	HYS72T256220HP–3.7–A	HYS72T256040HP–3.7–A
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**	**4 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	36	31	31	32	32
77	Product Type, Char 5	34	32	32	35	35
78	Product Type, Char 6	30	38	38	36	36
79	Product Type, Char 7	30	30	30	32	30
80	Product Type, Char 8	30	30	32	32	34
81	Product Type, Char 9	48	30	30	30	30
82	Product Type, Char 10	50	48	48	48	48
83	Product Type, Char 11	33	50	50	50	50
84	Product Type, Char 12	2E	33	33	33	33
85	Product Type, Char 13	37	2E	2E	2E	2E
86	Product Type, Char 14	41	37	37	37	37
87	Product Type, Char 15	20	41	41	41	41
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

5 Package Outlines

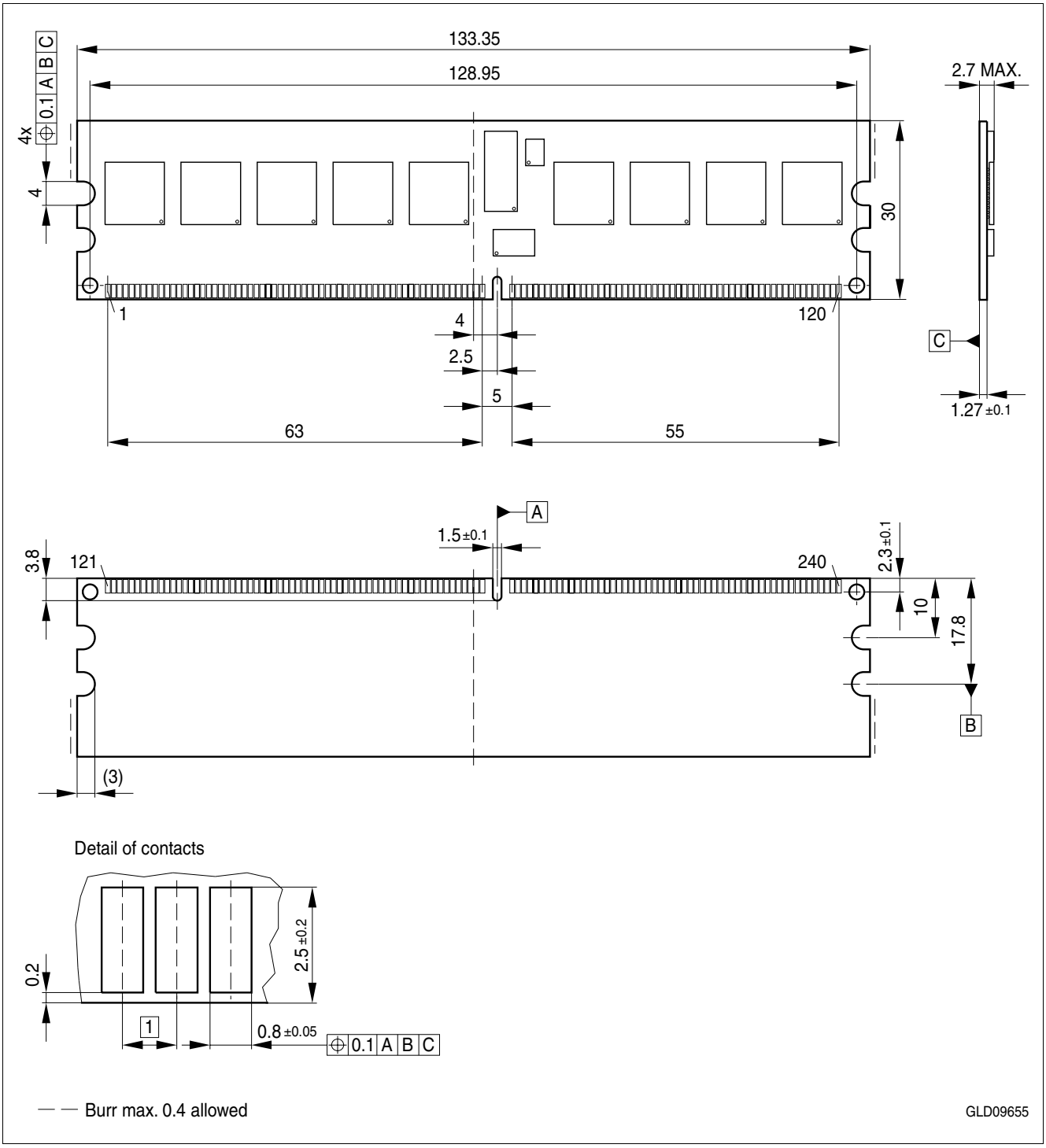

Figure 10 Package Outline Raw Card A-F L-DIM-240-11

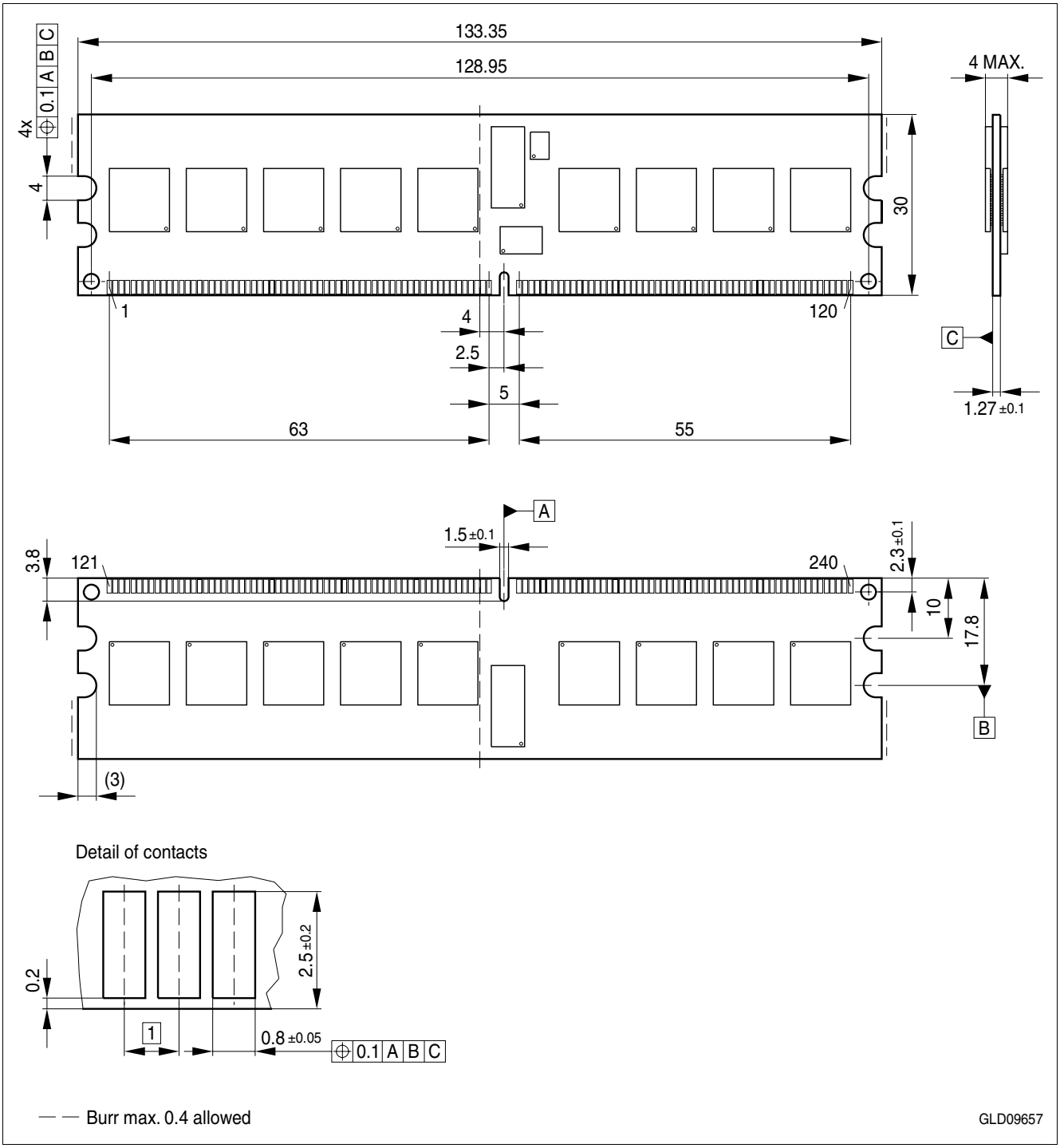

Figure 11 Package Outline Raw Card C-H L-DIM-240-13

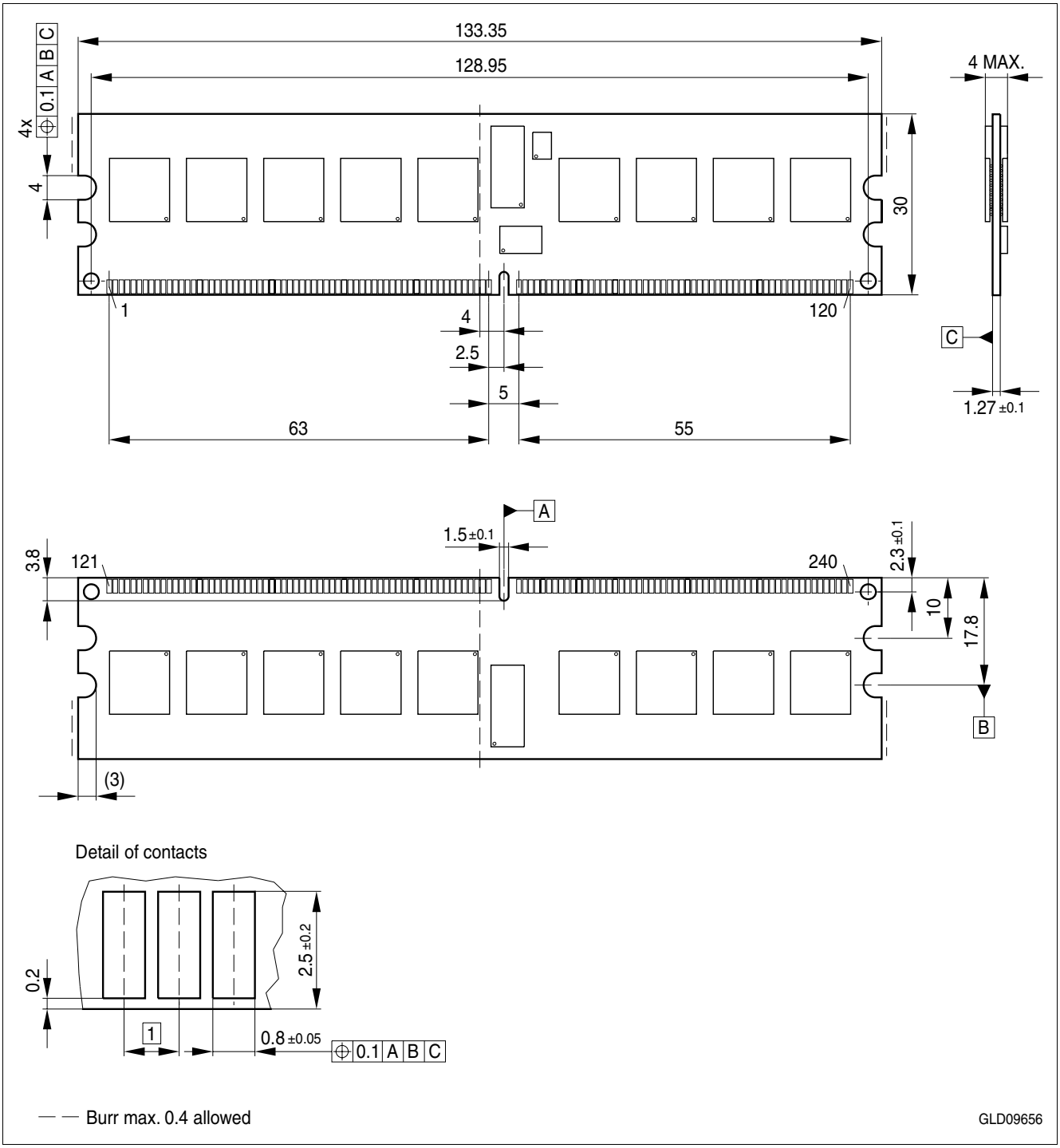

Figure 12 Package Outline Raw Card B-G L-DIM-240-12

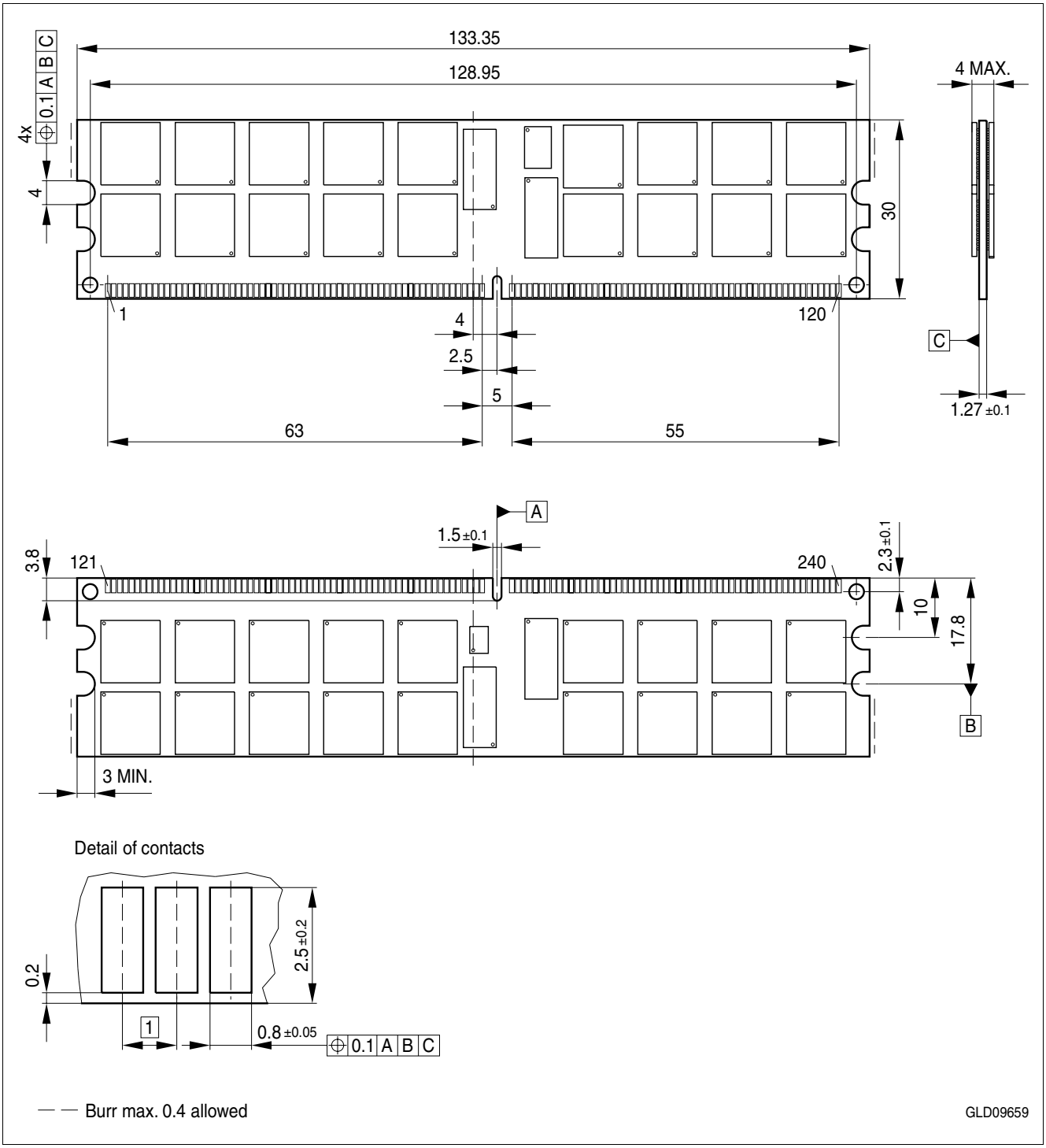

Figure 13 Package Outline Raw Card J L-DIM-240-20

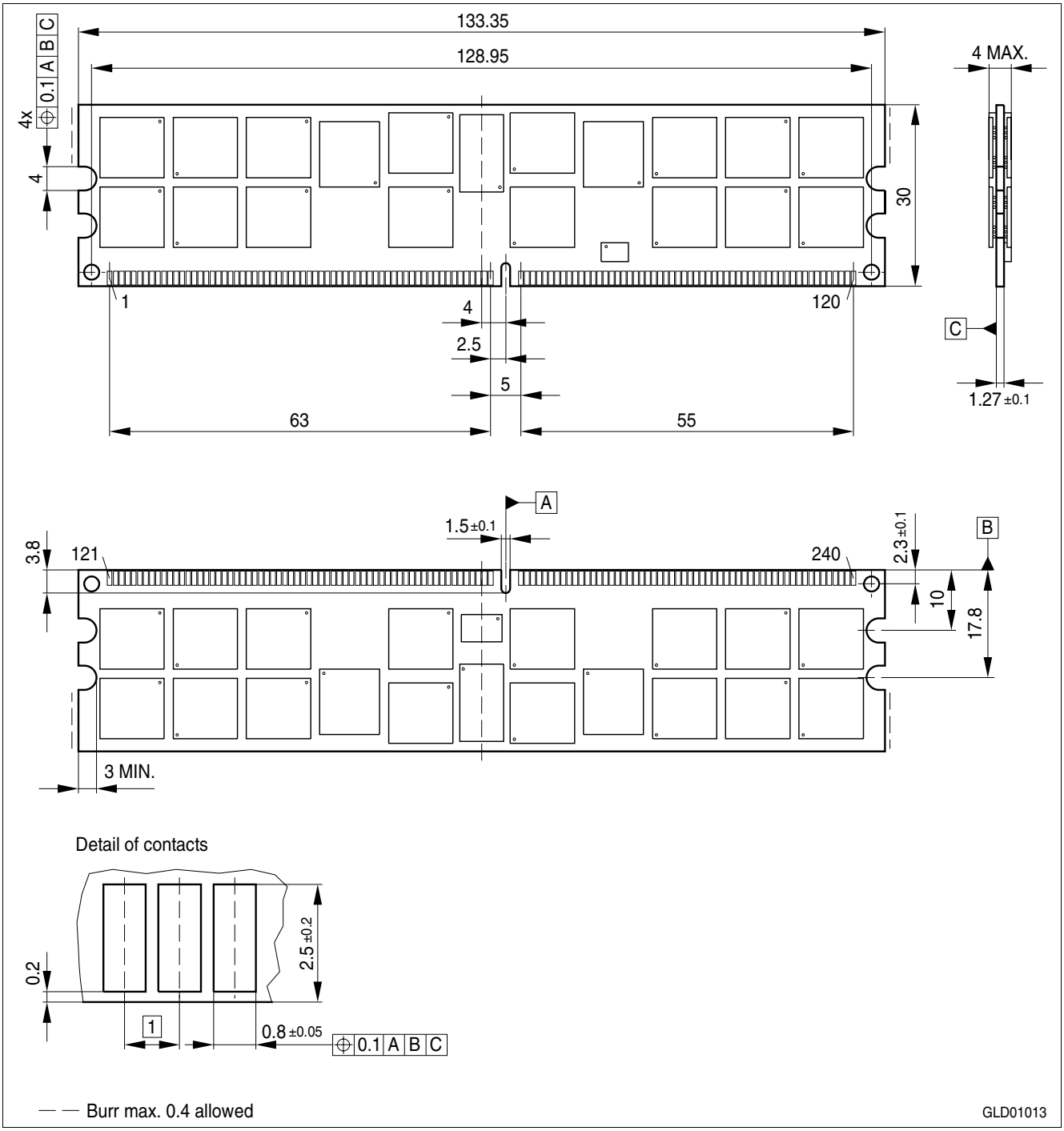

Figure 14 Package Outline Raw Card L L-DIM-240-40

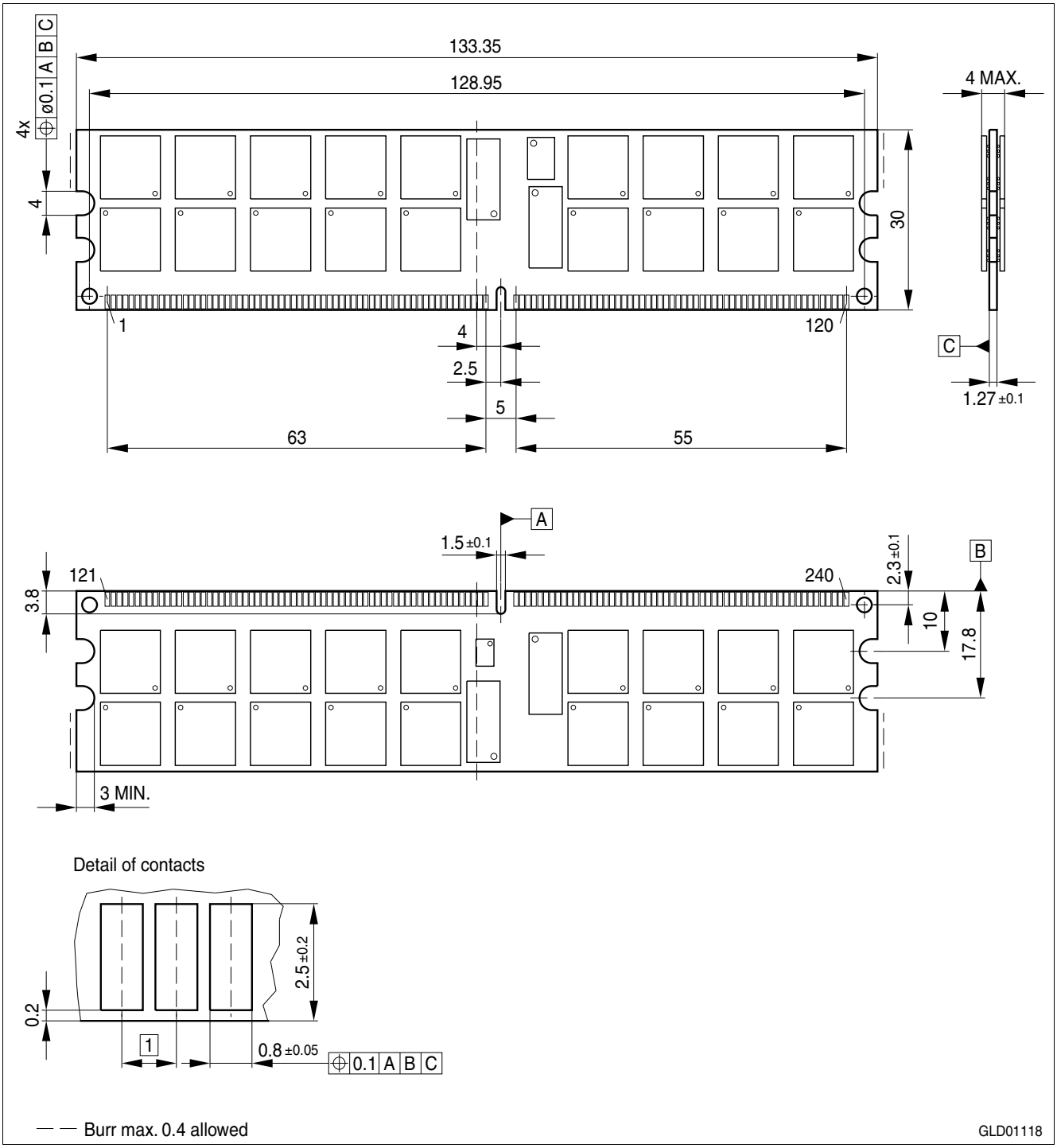

Figure 15 Package Outline Raw Card N L-DIM-240-44

6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some propriatory coding. Table 31 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 32 and for components in Table 33.

Table 31 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 32 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		P	Registered with parity
		U	**U**nbuffered
		F	**F**ully Buffered
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 33 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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